Semiconductor Devices for Telecommunications

Dec. '86

HITACHI

HITACHI SEMICONDUCTOR DEVICES FOR TELCOMMUNICATIONS

We are pleased to send along a copy of our newly published "Telecommunications Semiconductor Data Book."

We hope it will be of use to you, and that you will keep it close at hand along with our other data books, such as those on microprocessors, memories, and numerous other devices.

Telecommunications semiconductors have a wide diversity of applications, in telephones, switching equipment, and transmission lines. Hitachi has built up a full lineup of such products to match customers' needs, starting with CODECs and SLICs, and ranging from microprocessors at the core to opto devices and other discrete devices. Moreover, all of these have the high reliability required for actual use.

In addition to the devices included in this data book, many other types and models of telecommunications semiconductors are being developed, as part of Hitachi's continual effort to produce better products that satisfy our customers. To this end we depend on your opinions, your advice, and your encouragement in what is an increasingly challenging endeavor.

As always, we are grateful to you, our customer, for your patronage and cooperation. We hope this latest data book will be of help in the system design task.

Sincerely,

Masao Uchihashi
General Manager
Semiconductor & IC Div.
Hitachi, Ltd.

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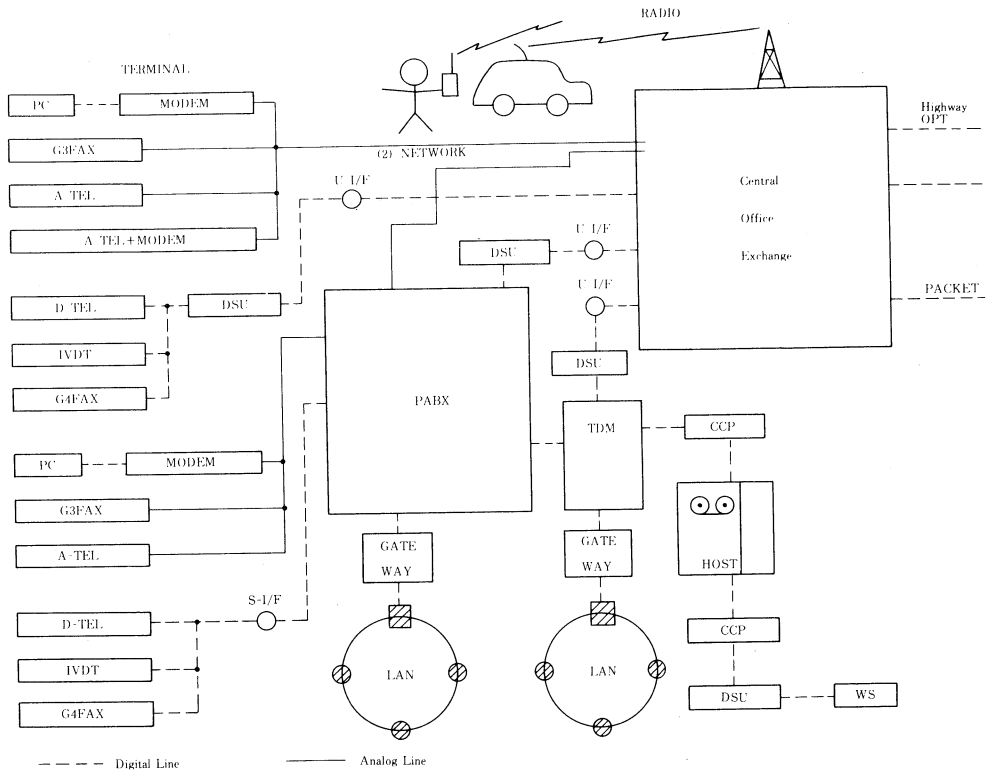
CONTENTS

SELECTION GUIDES FOR APPLICATIONS

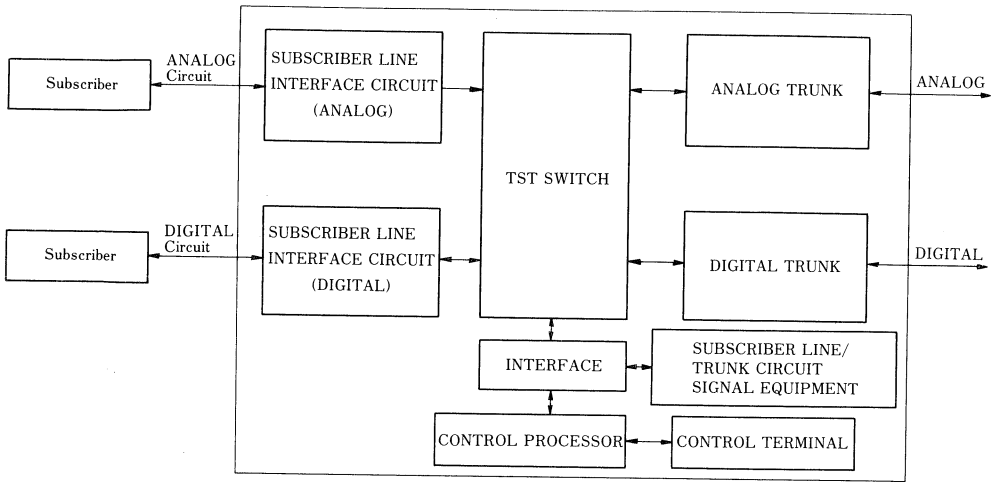
1. TELECOM NETWORK SYSTEM



DSU: DIGITAL SERVICE UNIT
IVDT: INTEGRATED MULTI FUNCTION TEL.
TDM: TIME DIVISION MULTIPLEXER
CCP: COMMUNICATION CONTROL PROCESSOR
SS: SWITCHING SYS.
WS: WORK STATION
PC: PERSONAL COMPUTER
LAN: LOCAL AREA NETWORK
I/F: INTERFACE
A-TEL: ANALOG TELEPHONE
D-TEL: DIGITAL TELEPHONE

2. FOR PABX (Private Auto Branch Exchange) APPLICATION

(1) For example structure of system

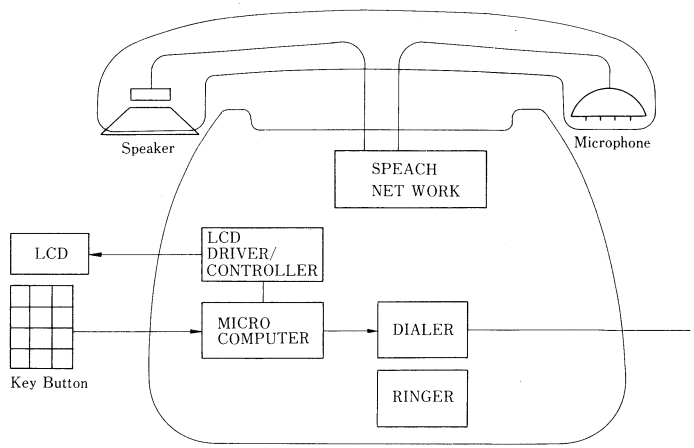


(2) Semiconductor lineup

	Used Semiconductor	Hitachi Product Lineup
Analog Subscriber	RT BSH CODEC MP GATE ARRAY	ECN 1200 HA16811 NT HD44230 SERIES HITACHI STANDARD IC
Digital Subscriber	FEED IC LAPD MP GATE ARRAY	HITACHI STANDARD IC
TST Switch	SWITCH MATRIX MP GATE ARRAY	HITACHI STANDARD IC
Analog Trunk	CODEC MP GATE ARRAY	HD44230 HITACHI STANDARD IC
Digital Trunk	X25 MP GATE ARRAY	HITACHI STANDARD IC
Subscriber Line/ Trunk Circuit Signal Equipment	MP DSP AD/DA	HITACHI STANDARD IC HD61810/811Y(HSP) HITACHI STANDARD IC
Control Processor	MP MEMORY GATE ARRAY	HITACHI STANDARD IC

3. FOR TELEPHONE SET APPLICATION

(1)-(A) For Example Structure of System (Analog Telephone)

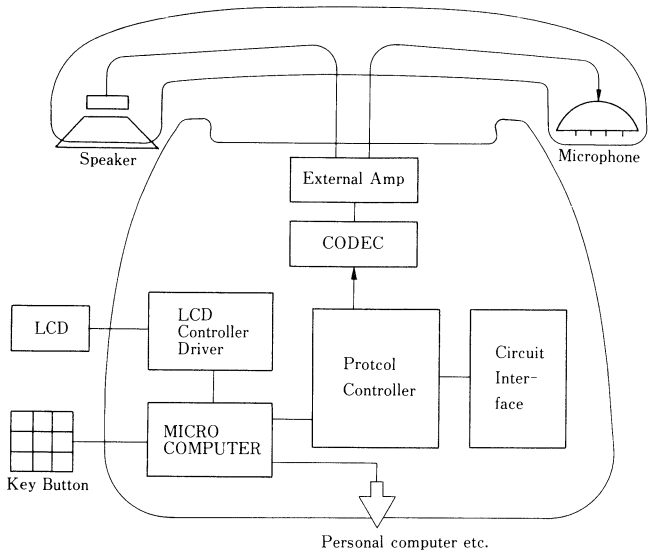


(2)-(A) Semiconductor line up

Function		Hitachi Product Line Up
		Standalone Function IC ⟷ Multi Function IC
LCD controller driver		LCD II / LCD III, IV / HD61827
Micro processor (MP)		STANDARD 4/8 bit MP / LCD III, IV / HD61827
Memory		HMCS4608*
Dailer	Pulse dialer	HD61825
	DTMF	HD61826
Tone receiver		HA16808
Speech network		HA16808
Tone ringer (Voice composite)		HA16802/4/5 / Voice composite HD61885/7
Mega control of automatic answering telephone set)		HA12089NT

*: Under development

(1)-(B) For example structure of system (Digital Telephone)



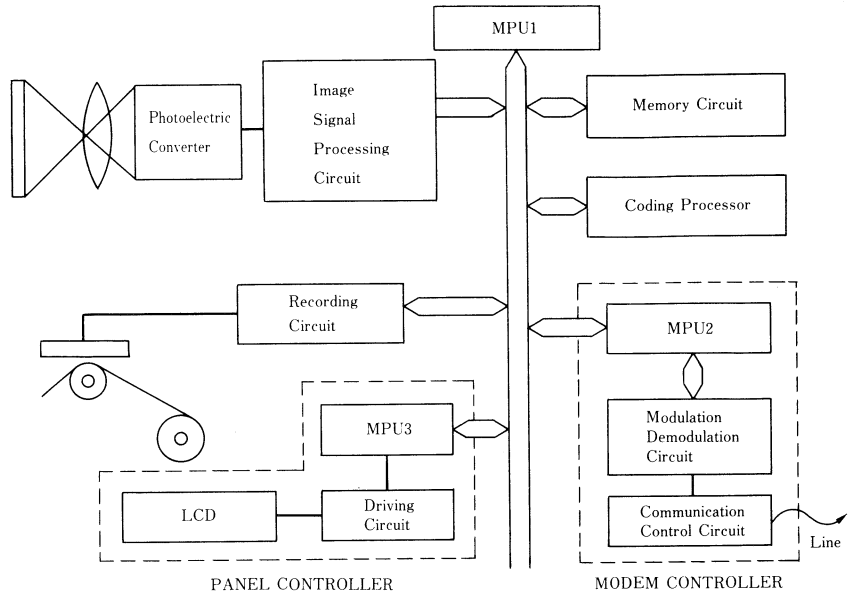
(2)-(B) Semiconductor line up

Function		Hitachi Product Line Up: Standalone Function IC ◄——► Multi Function IC
CODEC	Standard	HD44230 SERISE HD44240 SERISE HD44270 SERISE HD81AXXX *
	Side tone adjustable pin	
Loud speaker		Standard Linear IC
LCD controller driver		LCD II LCD III, IV
Micro processor (MP)		Standard 4/8 bit MP
Digital circuit interface		Standard gate array

*: Semi custom IC

4. FOR FACSIMILE SYSTEM APPLICATION

(1) For example structure of system



(2) Semiconductor line up

Function	Used Semiconductor	Hitachi Product Line Up
MPU 1.2	8 bit Microcomputer	Hitachi Standard IC
MPU 3	4 bit Microcomputer	Hitachi Standard IC
Memory Circuit	SRAM, EPROM	Hitachi Standard IC
Photoelectric Converter	CCD Photo Sensor	Hitachi Standard IC
Image Signal Processing Circuit	VPP, DIPP	HD63084
Modulator Demodulator Circuit	Signal Processor	HD61810
Coding Processor	DICEP	HD63085Y
Communication Controller	Gate Array	Hitachi Standard IC
LCD Driving Circuit	LCD Controller/Driver	Hitachi Standard IC
Recording Circuit	Hybrid IC	Hitachi Standard IC

5. APPLICATION FOR DATA COMMUNICATION SYSTEM

(1) APPLICATION SYSTEM

(a) Terminal
(b) Work Station
(c) Office Computer
(d) Personal Computer

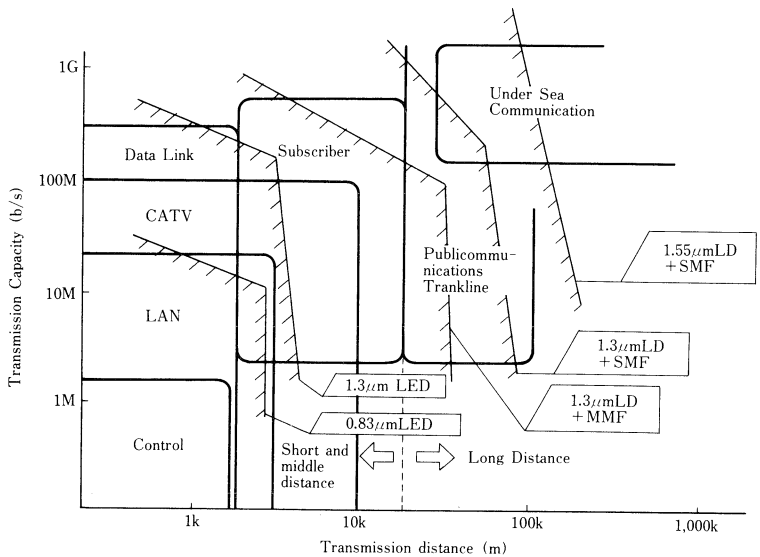
(2) Hitachi products line up

Serial I/O IC				Dual Port RAM
Bit Sync.		Character Sync.	Start-Stop System	
Network Layer	Link Layer			
	HD68562*			
		HD6852	HD6850 Series HD6350 Series HD64941*	HD63310 Series*

*: Preliminary

6. APPLICATION FOR OPTICAL FIBER COMMUNICATION SYSTEM

(1) Optical fiber communication system



(2) Hitach products line up

Transmission Rate (Mb/s)	Transmitter Device Number	Receiver Device Number
32	HE8402F (0.84 μm IRED) HE8403R1 HE8403ML (0.84 μm IRED)	HR8102 (SI-PIN) HS9605 (SI-APD)
140	HE1301R/ HE1301ML (1.3 μm IRED) HLP1400/ HLP1500 (0.84 μm LD)	HR1101 (InGaAsP-PIN) HR8102 (SI-PIN) HS9605 (SI-APD)
565	HXXXXX (1.3 μm LD DIL PKG) HL1321SP (1.3 μm LD with SMF)	HS9611 (InGaAs-PIN) HXXXXX (InGaAs-APD)
1000	HLP5400/ HL1321AC (1.3 μm LD) HL1521A (1.55 μm BH LD)	HXXXXX (InGaAs-APD)
1200	HL1341A (1.3 μm DFB LD)	HXXXXX (InGaAs-APD)
2000 or More	HL1541A (1.55 μm DFBLD)	HXXXXX (InGaAs-APD)

RELIABILITY

1. RELIABILITY

1.1 RELIABILITY CHARACTERISTICS FOR SEMICONDUCTOR DEVICES

Hitachi semiconductor devices are designed, manufactured and inspected so as to achieve a high level of reliability. Accordingly, system reliability can be improved by combining highly reliable components along proper emvironmental conditions. This section describes reliability characteristics, failure types and their mechanisms in terms of devices. First, semiconductor device characteristics are examined in light of their reliability.

(1) Semiconductor devices are essentially structure sensitive as seen in surface phenomenon. Fabricating the device requires precise control of a large number of process steps.

(2) Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.

(3) Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin film surfaces sometimes exhibit physically different characteristics from the bulks.

(4) Semiconductor device technology advances drastically: Many new devices have been developed using new processes over a short period of time. Thus, conventional device reliability data thus cannot be used in some cases.

(5) Semiconductor devices are characterized by volume production. Therefore, variations should be an important consideration.

(6) Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially operable semipermanently. However, wear failures caused by worn materials and migration should be also reviewed when electrode and package materials are not suited for particular environmental conditions.

(7) Component reliability may depend on device mounting, conditions for use, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength.

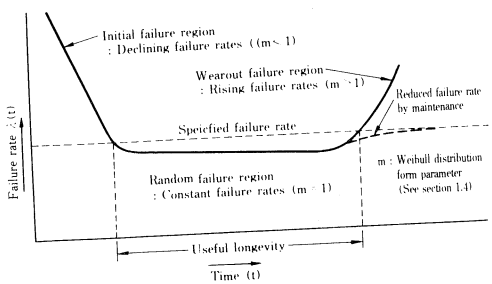


Fig. 1-1 Typical failure rate curve

Device reliability is generally represented by the failure rate. 'Failure' means that a device loses its function, including intermittent degradation as well as complete destruction. Failure criteria are defined in Chapter 3 Reliability Test. Under actual use, however, variations in failure detection sensitivity and operational margin should be considered.

Generally, the failure rate of electric components and equipment is represented by the bathtub curve shown in Fig. 1-1. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which means an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be physically represented as well as statistically. Both aspects of failures have been thoroughly analyzed to establish a high level of reliability.

1.2 FAILURE TYPES AND THEIR MECHANISMS

1.2.1 Failure physics

Failure physics is, in a broad sense, a basic technology of "physics + engineering". It is used to examine the physical mechanism of failures in terms of atoms and molecules to improve device reliability. This physical approach was introduced to the reliability field with the demand for minimized development cost and period, as technology rapidly developed and system performance increased, requiring more complex and higher levels of reliability. These conditions derived from the development of solid state physics (semiconductor physics) after World War II and associated device development.

Failure physics have been employed to:

1) Detect failed devices as soon as possible
2) Establish models and equations used for failure prediction
3) Evaluate reliability for short periods by accelerated life tests

The purpose of the failure physics approach is to contribute to reliability related fields such as product design, prediction, test, storage and usage by adding physics as a basic technology to conventional experimental and statistical approaches.

1.2.2 Failure types and their mechanisms

Device failures are physically discussed in this section. Semiconductor device failures are basically categorized as disconnection, short-circuit, deterioration and miscellaneous failures. These failures and their causes are summarized in Table 1-1. Actual failures are shown in Photos 1-7 to 1-16. Typical failure mechanisms are reviewed next.

(1) Surface Deterioration

The pn junction has a charge density of $10^{14} - 10^{20}/cm^3$. If charges exceeding the above density are accumulated on the pn junction surface, particularly adjacent to a depletion layer, electrical characteristics of the junction tend to be easily varied. Although the surface of such devices as

planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by surface channels still exists. Surface deterioration depends heavily on applied temperature and voltage and is often handled by the reaction model shown in section 3.3. One example of recent failures is surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage BV_{DS} by raising internal voltage and when a strong electric field is established near the MOS device's drain resulting from reduced device geometry from 5 μm to 2 μm. Generated hot carriers may affect surface boundary characteristics on a part of the gate oxide film, resulting in degradation of threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices have employed improved design and process techniques to prevent these problems. However, as processing becomes even finer, surface deterioration may possibly become a serious problem.

(2) Electrode-related Failures

Electrode-related failures have become increasingly important as multi-layer wiring has become more complicated. Noticable failures include electromigration and Al wiring corrosion in plastic sealed packages.

① Electromigration

This is a phenomenon in which metal atoms are moved by a large current of about 10^6 A/cm^2 supplied to the metal. When ionized atoms collide with current of about scattering electrons, an 'electron wind' is produced. This wind moves the metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at an opposite one. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause shortcircuits in multi-metal line.

② Multi-metal line related failures

Major failures associated with multi-metal line include increased leak currents, shortcircuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

③ Al line corrosion and disconnection

When Plastic encapsulated devices are subjected to high-temperatures, high-humidity or a bias-applied condition, Al electrodes in devices can cause corrosion or disconnection (Fig. 1-2). Under high-temperatures and high-humidity, corrosions are randomly generated over the element surface. However, after an extended period of time, the corrosions have not significantly increased. Accordingly, this failure is possibly due to an initial failure associated with manufacturing. It is also verified that this type of failure can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-applied, high-temperature, high-humidity condition, on the other hand, corrosions are generated in higher potential areas while in lower potential areas, grain corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Fig. 1-3.

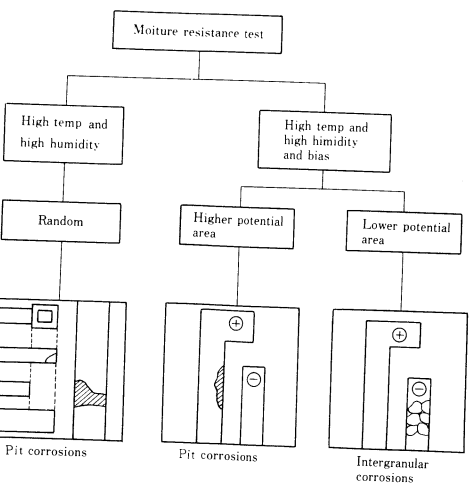


Fig. 1-2 Categorized Al corrosion mode

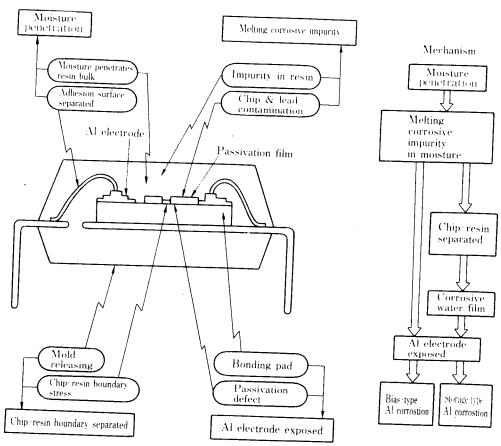


Fig. 1-3 Plastic package cross section and Al corrosion mechanism

(3) Bonding related failures

① Degradation caused by intermetallic formation

Bonding strength degradation and contact resistance increase are caused by compounds formed in connections between Au wire and Al film or between Au film and Al wire. These are the most serious problems in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

② Wire creep

Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introducing to the intergranular system. Bonding

under usual conditions with no loop configuration failures does not cause this failure unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

③ Chip crack

With the increase in chip size associated with the increased number of incorporated functions, more problems have been occurring during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element analysis and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. However, this is difficult due to the existence of a silicon oxide film on the silicon back surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

④ Reduced maximum power dissipations

For power devices, heat fatigue due to thermal expansion coefficient mismatch among different materials deteriorates thermal resistance. This results in decreased maximum power dissipations.

(4) Sealing related failures

Hermetic sealing packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

1. Al line corrosion on the chip surface due to slight moisture and reaction between the different ionized materials.
2. Intermittent moving foreign metals short
3. Al line corrosion due to extraneous H_2O caused by hermetic failure

Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parastic effects and metal shorts. The foreign matter detection method is specified by MIL-STD-883C, PIND (Particle Impact Noise Detection) Test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone, and then amplifying.

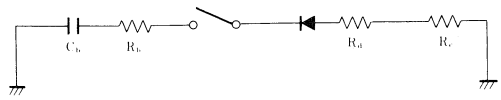
(5) Electrostatic discharge destruction

① Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure: the human body model, charged device model and field induced model.

The human body is easily charged. A person just walking across a carpet can be charged up to 15000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Fig. 1-4. The human body's capacitance Cb and resistance Rb are 100 to 200 pF and 1000 to 2000Ω, respectively. Assuming a body is charged with 2000V, the dissipated energy is obtained by:

With a time constant of 10^{-7} sec, the dissipated energy is 2 KW, which is enough to destroy a small area of a chip.

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of



Cb – Human body capacity
Rb – Human body resistance
Rd – Device resistance
Rc – Resistance between device and ground

$$E = \frac{1}{2} CbV^2 = 0.2 \times 10^{-3} \text{ J}$$

Fig. 1-4 Equivalent circuit of human body model

this model is shown in Fig. 1-5. Device size and device position relative to GND are important parameters in this model since the model depends on device capacity.

In the field induced model a device is left under a strong electric field or is affected by neighboring high voltage material. Since the capacitor of device or lead of device acts like an antenna, the following cases will possibly cause destruction. 1) a device is incorporated into a high electric field such as a CRT, 2) a device is left under a high-frequency electric field and 3) a device is moved with a container charged at high voltage, such as a tube.

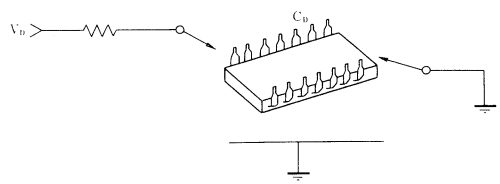


Fig. 1-5 Equivalent circuit of charging model

② Latch up

Latch up is a problem unique in CMOS devices. This problem is a thyristor phenomenon caused by a parastic PNP or NPN transistor formed in the CMOS configuration. Latch up occurs when an accidental surge voltage exceeding a maximum rating, a power supply ripple, an unregulated power supply and noise is applied, or when a device is operated from two sources having different set-up voltages. These cases can cause input or output current to flow in the opposite direction from usual flow, which triggers parastic thyristors. This results in excessive current flowing between a power supply and ground. This phenomenon continues until the power is off or the flowing current is forced to be reduced to a certain level. Once latch up occurs in an operating device, the device will be destroyed. Much effort should be made in designing circuits to prevent latch up. Latch up triggering input or output currents start to flow under the following conditions.

Vin > Vcc or Vin < GND for input level

Vout > Vcc or Vout < GND for input level

Therefore, circuits should be designed so that no forward current flows through the input protection diodes or output parastic diodes.

③ Soft errors

When α particles are generated from uranium or thorium in a package the silicon surface of an LSI chip, electron-hole pairs are formed which act as noise to data lines and other floating nodes, causing temporary soft errors. This pheno-

Table 1-1 Failure causes and mechanism

Failure related causes		Failure mechanisms	Failure modes	Example
Passivation	Surface oxide film, Insulating film between wires	Pin hole, Crack, Uneven thickness, Contamination, Surface inversion, Hot carrier injected	Withstanding voltage reduced, Short, Leak current increased, h_{FE} degraded, Threshold voltage variation, Noise	Fig. 1-7
Metallization	Interconnection, Contact, Through hole	Flaw, Void, Mechanical damage, Break due to uneven surface, Non-ohmic contact, Insufficient adhesion strength, Improper thickness, Electromigration, Corrosion	Open, Short, Resistance increased	Figs. 1-8, 1-16
Connection	Wire bonding, Ball bonding	Bonding runout, Compounds between metals, Bonding position mismatch, Bonding damaged	Open, Short Resistance increased	Fig. 1-9
Wire lead	Internal connection	Disconnection, Sagging, Short	Open, Short	Fig. 1-10
Diffusion, Junction	Junction diffusion, Isolation	Crystal defect, Crystallized impurity, Photo resist mismatching	Withstanding voltage reduced, Short	Fig. 1-11
Die bonding	Connection between die and package	Peeling chip, Crack	Open, Short, Unstable operation, Thermal resistance increased	Fig. 1-12
Package sheling	Packaging, Hermetic Seal, Lead plating, Hermetic package & plastic package, Filler gas	Integrity, moisture ingress, impurity gas, high temperature, surface contamination, lead rust, lead bend, break	Short, Leak current Increased, Open, Corrosion disconnection, Soldering failure	Fig. 1-13
Foreign matter	Foreign matter in package	Dirt, Conducting foreign matter, Organic carbide	Short, Leak current increased	Fig. 1-14
Input/output pin	Electrostatistics, Excessive Voltage, Surge	Electron destroyed	Short, Open, Fusing	Fig. 1-15
Disturbance	α particle	Electron hole generated	Soft error	
	High electric field	Surface inversion	Leak current increased	

menon is shown in Fig. 1-6. Only electrons from among the electron-hole pairs are only collected to a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases organic material, PIQ, is applied to the surface of the device.

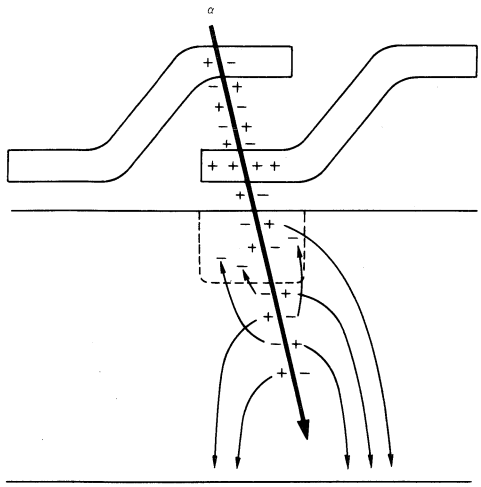


Fig. 1-6 **Soft error caused by α particles in dynamic memory**

(6) Fine geometry related problems

In response to higher integration requirements for memories and microcomputers, LSI geometry has been reduced in the way of 5 μm → 3 μm → 2 μm → 1.3 μm. However power supply has not been scaled down used for 5V, only line dimensions has been fined increasingly. Problems associated with finer geometry are shown in Table 1-2.

Table 1-2 Finer geometry related problems

Item	Problems	Countremasure
5V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Gettering ◦ Screening
Horizontal dimension reduction	• Soft errors by α particles • Al reliability reduced • CMOS latch up • Mask alignment margin reduced • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved ◦ Process improved
Vertical & horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

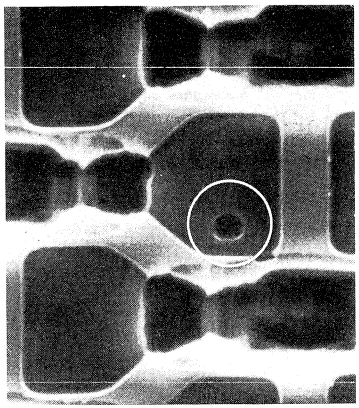


Fig. 1-7 Pin hole

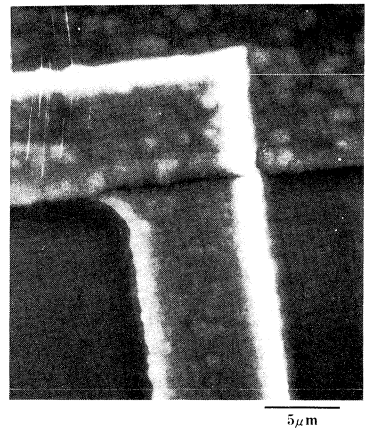


Fig. 1-8 Metallization break due to uneven surface

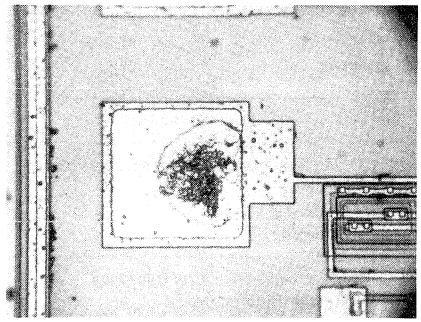


Fig. 1-9 Defect caused by bonding

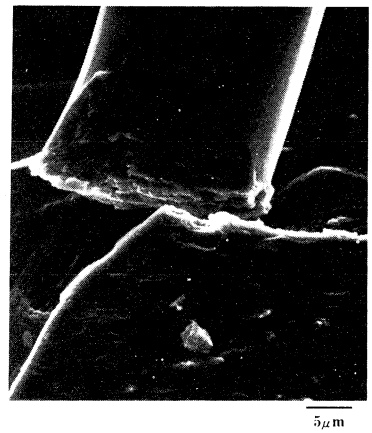


Fig. 1-10 Bonding wire destruction by ultrasonic fatigue

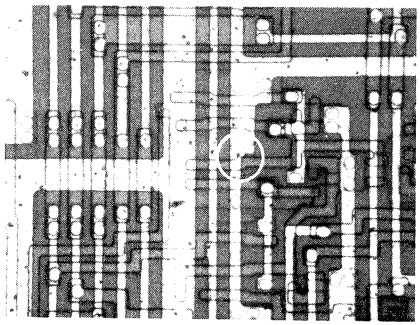


Fig. 1-11 Diffusion photo resist failure

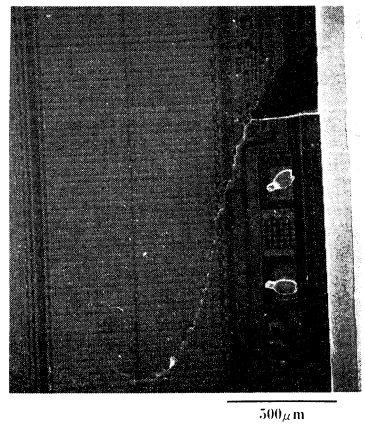


Fig. 1-12 Chip crack

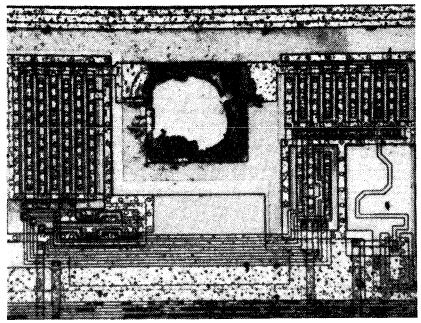


Fig. 1-13 Disconnection caused by bonding pad corrosion

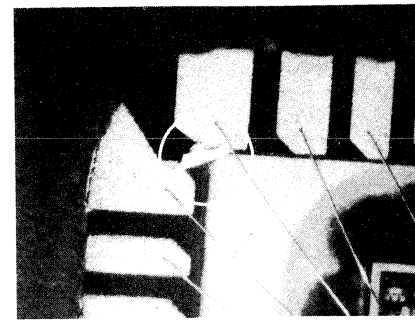


Fig. 1-14 Short caused by conducting foreign matter in a package

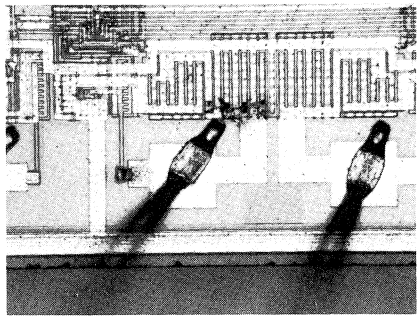
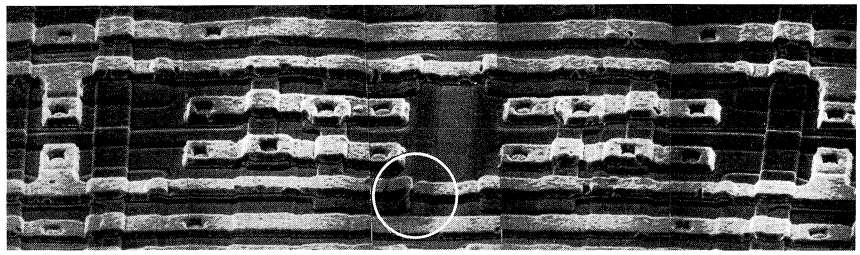
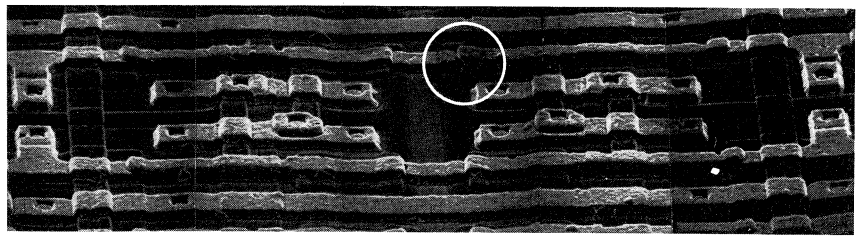


Fig. 1-15 Output pin destruction (open failure)



SEM photo of failure



The above part taken in opposite direction

Fig. 1-16 Al film break due to uneven surface

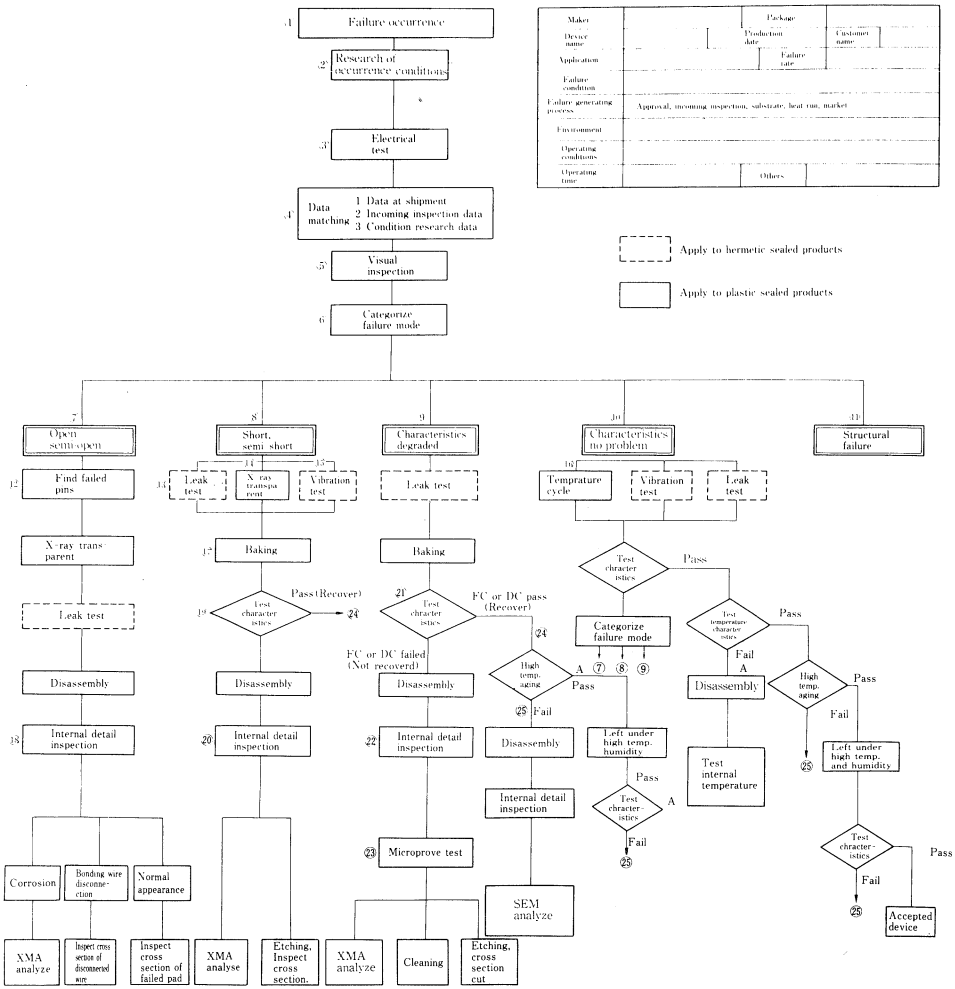


Fig. 1-17 Failure analysis flow

1.3 FAILURE ANALYSIS

Failures can occur during reliability testing or processing by users, or in the field. Analyzing the failures not only provides data on failure modes and failure mechanisms, but also contributes to device reliability improvement. Failure analysis should be carefully performed in a proper way. Please note the following failure analysis:

① Failure devices must be so analyzed as not to apply mechanical, electrical or thermal shocks. These shocks may alter the failure conditions.

② Equipment used for analysis should be suited for the purpose.

③ Proper failure analysis requires good knowledge of device design and manufacturing techniques.

④ Data concering stress applied under tests and use and failure histories are valuable for proper failure analysis.

⑤ Failure analysis results should be systematically recorded and accumulated.

A failure analysis procedure performed by semiconductor manufacturers is flowcharted in Fig. 1-17. Details of the procedure may vary depending on the failure mode and failure degree. Main equipment used for failure analysis are shown in Table 1-3.

Table 1-3 Equipment for failure analysis

For observation	Stereomicroscope Metal microscope Ultrasonic microscope Scanner electron microscope (SEM) Transparent electron microscope (TEM) Infrared microscope Scanner laser microscope X-ray transparent equipment Camera Scanner surface temperature measurement Others
For electrical characteristics measurement	Diode curve tracer Transistor curve tracer IC curve tracer Transistor tester IC tester LSI tester Function tester Oscilloscope Pulse generator DC power supply Ammeter, microammeter Voltmeter Noise measurement Small ohm-meter Insulating ohm-meter LCR meter Manipulator Others
For spectrum analyzing	Electron microscope X-ray microanalyzer (XMA) Fluorescence X-ray analyzer Auger electron spectral analyzer Auger electron microanalyzer
For analyzing	Ion microanalyzer (IMA) Laser microanalyzer Electron beam analyzer X-ray analyzer Infrared absorption spectral analyzer Emission spectral analyzer Atomic absorption photometer PH meter Electron spectral analyzer (ESCA) Nuclear magnetic resonance analyzer (NMR) He leak tester Bubble leak tester Ion chromatography Gas chromatography Mass spectrographer Differential thermal analyzer Others
For generating samples used for analyzing	Cutter Grinder Sander Epoxy mould Evaporation equipment Draft (foul solution, exhaust gas) Etchants Plastic decomposition Others
For various tests	PIND tester Thermostatic chamber Burn-in equipment Humidity generator Temperature cycling chamber Tension tester Others
Others	Chemical balance, Projector, Measuring micrometer, Micrometer, Caliper, Tarry step

Table 1-4 Screenings

Screening		Failure effective to screening	Effectivity	Remarks
Visual before sealing		Lead plating, wire bond metallization, contaminants, oxide film, corrosion, foreign material, substrate, die bond	Extremely effective	• Essential for highly reliable devices. • Cost depends on visual inspection.
Infrared-ray		Thermal resistance design	Very effective	• Used for design evaluation only.
X-ray		Die bond, sealing, lead, plating, package, foreign material, contaminants	Extremely effective for die bond, Effective for others	• Visual inspection after sealing. • X-ray can peneterate Al, Si, etc. • Cost is six times higher than visual before sealing.
High temp. storage		Electrical stability, Si (bulk), metallization, corrosion	Effective	• Highly recommended screening.
Thermal cycle		Package, wire bond, sealing, chip crack, die bond, thermally mismatching	Effective	• Effective for Al lead devices.
Thermal shock			Effective	• The same as for thermal cycling except for slightly larger stress level.
Constant acceleration		Lead plating, wire bond, die bond, chip crack	Effective	
Drop	No monitor	Wire bond, chip crack, die bond	Effective	• Inferior to constant acceleration screening.
	With monitor	Foreign materials, semi-short, semidisconnection	Inferior Slightly effective Slightly effective	• For foreign materials, inferior to visual and X-ray screenings.
Vibration fatigue		Lead plating, wire bond, package, substrate crack, die bond	Inferior	• Destruction possibility exists.
Variable frequency vibration	No monitor	Package, wire bond, die bond, substrate	Slightly effective	
	With monitor	Foreign materials, lead plating, semi-disconnection	Slightly effective Effective Effective	
Random vibration	No monitor	Package, wire bond, die bond, substrate	Effective	• More effective for space equipment than variable frequency vibration without monitor
	With monitor	Foreign materials, lead plating, semi-disconnection	Slightly effective	• Not recommended due to its high cost except for special cases.
He leak test		Package, sealing	Slightly effective	• Detect leak $10^{-6} \sim 10^{-10}$ atm cc/sec.
Radio isotope leak test		Package, sealing	Slightly effective	• Detect leak $10^{-8} \sim 10^{-12}$ atm cc/sec.
Phloro carbon leak test		Package, sealing	Slightly effective	• Detect leak 10^{-3} atm cc/sec on more.
Glycerol leak test		Package, sealing	Slightly effective	• Possibility of reliability deterioration.
High voltage test		Oxide film	Effective	
Insulating resistor		Lead plating, contaminants, metallization	Slightly effective	

(to be continued)

Screening	Failure effective to screening	Effectivity	Remarks
AC	Metallization, design, Si (bulk), parameter variation, oxide film, contaminants, inversion channel	Very effective	
DC	Metallization	Effective	
High temp. AC	AC operation	Extremely effective	• Temperature accelerates failures. • Most effective screening though most expensive.
High temp. inverse bias	Inversion channel	Effective	
Visual after sealing	Package crack, package sealing	Effective	
Power sequence	Parastic PNPN	Effective	Required for latch-up sensitive devices.

Table 1-5 Activation energy of deterioration in semiconductor devices

Area	Deterioration mechanism	Deterioration	Activation energy
Seal glass	Insulating resistance deteriorated (Pb^+ ion drift)	Conductivity	1.05 to 1.17 eV
Wire bonding	Au-Al alloy	Bonding tension strength	0.11
		Contact resistance	0.57, 1.04, 1.08
		Au-Al alloy film growth	0.69
Die bonding	Connection strength deteriorated	Au diffusion coefficient in Si	1.1
Contact	Contact disconnection (Si diffusion in Al)	Burn-out life (Pure Al)	0.55
		Burn-out life (Al containing Si)	0.31
		Contact resistance	0.89 (Tj > 210°C)
		Al diffusion in Si (Al bulk)	0.79
		Al diffusion in Si (1.8 Si-Al)	0.9
Metallization	Al electromigration	Burn-out life (small particle)	0.48
		Burn-out life (large particle)	0.84
		Burn-out life (SiO_2 coating)	1.2
		Al self-diffusion coeffecient	1.48
	Al moisture corrosion	Al surface film generation	1.17 (T > 60°C)
Resin	Al corrosion	Water diffusion coeffecient in resin	Approx. 0.4
Passivation	Surface resistance reduced	Conductivity (PSG)	0.8 0.5 (after moisture absorption)
		Conductivity (CVD SiO_2)	0.6
	Charge moving in PSG (Na^+ ion drift)	Na diffusion coefficient ([P] 4 mol %)	1.38
Field SiO_2	Surface resistance reduced (Adsorbed water film leak)	Surface conductivity	0.35 (> 80% RH) 0.65 (> 40% RH)
	Surface charge leak	Vth variation	1.0
	SiO_2 film alkaline moving	Na^+ diffusion constant	1.1 to 1.4
		Li^+ diffusion constant	1.0
		H^+ diffusion constant	0.31, 0.44
	SiO_2 NAPOX surface boundary resistance reduced	Surface boundary leak current	0.43 to 0.70
	SiO_2 film trap charge acquisition	Vth variation	1.3
	Hot electron SiO_2	Vth variation	1.06 0.97~2.0 (Actual device)
	Hot 'ectron SiO_2		1.0

Table 1-6 Typical acceleration life tests

Stress applied	Characteristics	Example of tests	Acceleration factors	Failure modes
Constant stress	Inspects how stress affects devices	High & low temp storage	Temp	Surface deteriorated
		Operational lifetime	Junction temp, voltage	Surface deteriorated
		High temp & humidity storage	Temp, humidity	Corrosion, breakdown voltage reduced
		High temp & humidity bias	Temp, humidity, voltage	Corrosion, bridge between pins
Cyclic stress	Inspects how cyclic stress affect devices	Temp cycling (thermal shock)	Temp difference, duty	Disconnection, shorted
		Power cycling	Temp difference, duty	Disconnection thermal resistance reduced
		Humidity & Temp cycling	Temp difference, duty, humidity difference	Disconnection, shorts, corrosion
Step stress	Inspects limits of devices to stress	Operational lifetime	Junction temp, voltage	Element deteriorated
		High temp inverse bias	Junction temp, voltage	Element deteriorated
		Surge destruction	Electricity, voltage	Electrostatic destruction, element deteriorated
		Soldering resistance	Temp, time	Chip crack, element deteriorated

2. QUALITY ASSURANCE

2.1 RELIABILITY DESIGN AND PROCESS FEATURES OF HITACHI SEMICONDUCTOR DEVICES

The technology for designing and processing individual semiconductor devices, ICs, and LSIs is remarkably progressing towards more refined processing and higher reliability. Beginning overall with the setting of target specifications for reliability design of circuits and devices, higher integration and higher reliability can be accomplished by upgrading processing technology such as crystal processing, epitaxial growth, impurity diffusion, ion implantation, photo-etching surface stabilization, terminal forming, bonding, and sealing, as well as manufacturing process control technology, inspection, reliability evaluation, failure analysis, and so on.

The following describes reliability design and process features of Hitachi semiconductor devices.

2.1.1 Surface stabilization technology

There are mainly two reasons for surface degradation, one of the primary failure modes of semiconductor devices, according to the degradation parameter and mechanism.

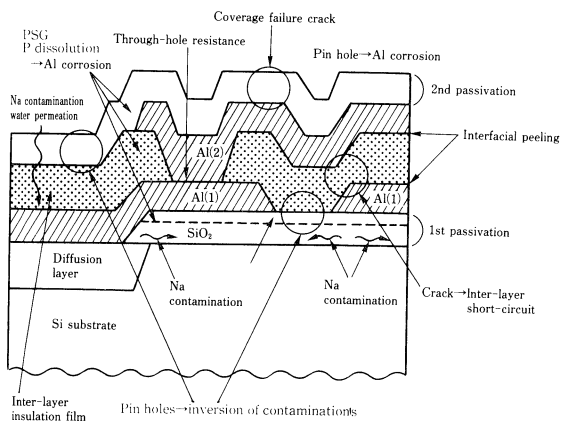


Fig. 2-1 Cross-section of surface protective films and the problems

One is due to the conductivity on the Si-SiO_2 surface layer such as backward pressure degradation at PN junction, threshold voltage (V_{TH}), a change on standing of mutual conductance, and the other is due to carrier reconnection on surface such as current amplification degradation and low-frequency noise degradation.

The following four factors are considered to cause surface degradation. (See Figure 2-1)

(1) Penetration of mobile ions (Na^+ etc.) into the first passivation film from manufacturing process and/or sealing material
(2) Surface charge (Qss) on surface level of the Si-SiO_2 surface layer
(3) Pin hole: failure of passivation film
(4) Leak charge onto the second passivation film from electrical fields

With the advances in device integration and performance, even a slight contamination of mobile ions can be a serious problem, and even a extremely partial contamination from passivation defects and the like can cause a fatal failure.

Therefore, to stabilize the Si surface, it is necessary to improve the "getter" effect for mobile ions in the first passivation film, to ensure surface stability by clean processes, to produce defect free films, and to have enough threshold voltage (V_{TH}) to resist leak charge. Additionally, to enhance the reliability of plastic sealing components (moisture resistance), the second passivation performs a significant role. The following features are required.

(1) Penetration prevention of external water molecules or contamination, and contaminated ions from the resin material itself
(2) Passivation film to resist thermal stress of the resin material
(3) Small defect density

From this point of view, Hitachi has enhanced reliability by developing and adopting first and second passivations, and a layer insulation film for various types of semiconductor devices. This section introduces a part of their development and adoption.

(1) Improve the second passivation to prevent external contamination, and to enhance moisture resistance
(2) Clean and defect free processes;
Cleanliness and defect free processes are particularly important for the first passivation. Hitachi is trying to achieve defect free processes by purifying process materials such as photoresist, cleaner, and evaporation Al, by cleaning oxidation furnace quartz pipes, by upgrading photomasks, by improving wafer handling methods, and by eliminating process dust. (See Figure 2-2)
(3) Leak charge countermeasure;
Threshold voltage (V_{TH}) can be made larger by forming a channel stopper layer using ion implantation technology, and by thickening passivation films.
(4) Process control;
For process control concerned with mobile ions, control of the implantation amount using specific MOS component, or automatic measurement of film thickness using optical methods at polysilicon film generation, is carried out as well as the BT (Bias-Temperature) method.

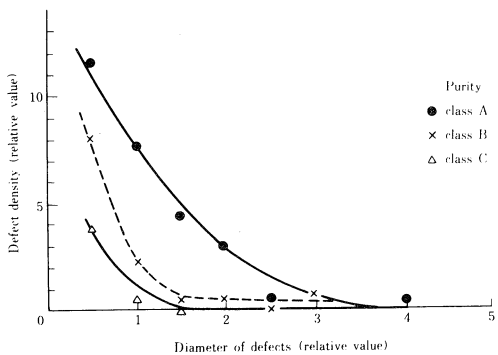


Fig. 2-2 Relationship between defect density in passivation films and the purity

Moreover, Hitachi has developed technology for refined, higher-density, and multilayer line, and has adopted this technology to various semiconductor devices. The following describes some of them.

(1) Anisotropic dry etching using special gas is adopted (Figure 2-3), since conventional wet etching using chemicals cannot ensure enough dimension precision for refined processes.

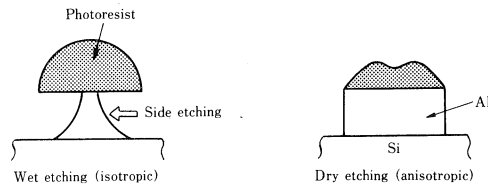


Fig. 2-3 Cross sections of devices during wiring process using the etching methods

(2) In the case of multilayer line, flow glass is applied or an etching method by sputtering is utilized.

2.1.2 Soft error

(1) Soft error mechanism

More and more refined IC memories are now being manufactured. This refinement implies a reduction in signal levels and accumulated charge in dynamic memories, as well as reduction of chip dimensions. The soft error problem interferes with this refinement. A "soft error" is a temporary failure which can be corrected by rewriting data into memory. The cause of it is α particle emitted by uranium and thorium (U, Th) which are slightly present in packaging material. A memory datum can be reversed when a memory chip is exposed to this α particle and subsequently many electron holes are generated on the Si substrate.

Figure 2-4 illustrates how an NMOS dynamic memory datum can be reversed by one of this α particle. In NMOS dynamic memory, only the electron cloud reverses information in a memory cell (data "1" → "0"), and the hole cloud is drawn by electric potential since a negative charge is formed onto the Si substrate. The failure mode shown in Figure 2-4 is defined as "memory cell mode" of a soft error and is distinguished from "bit line mode" to be described next.

Figure 2-5 illustrates "bit line mode" of a soft error. When

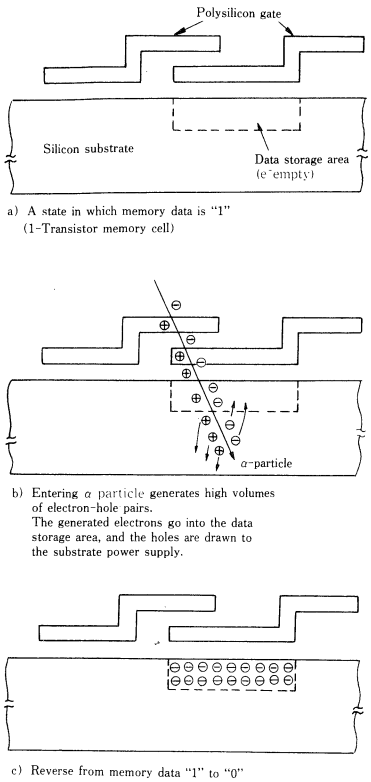


Fig. 2-4 Malfunction at the memory cell

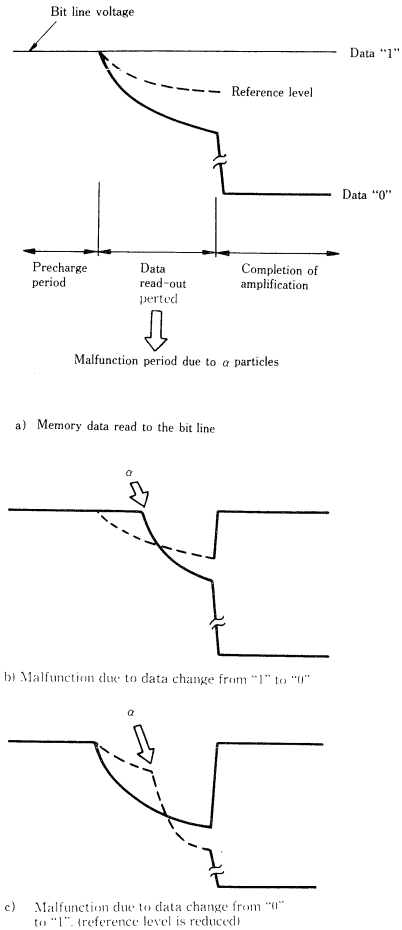


Fig. 2-5 Malfunction on the bit line

the information stored in a memory cell is placed on the bit line, the electric potential of the bit line is altered due to this bit of information.

This charge is very small (hundreds mV), and the electric, potential is amplified by a sense amplifier, compared with the basic electric potential (electric potential read from dummy cell).

Datum reverse from "1" to "0" occurs if the bit line electric potential is below the basic electric potential due to the emission of α particle during the short period from data reading to amplification. The datum reverse from "0" to "1", on the other hand, occurs if the basic electric potential is lowered.

These are designated as "bit line mode", since errors occur through the emission of α particle onto the bit line in both cases. Figure 2-6 shows the relation between soft error occurrence ratio and cycle time.

Actual products are characterized by either cell mode or bit line mode soft errors, or their mixed mode.

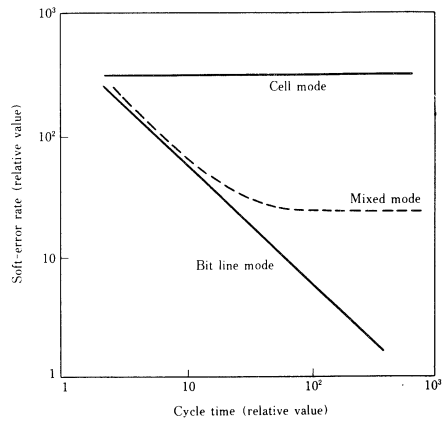


Fig. 2-6 The cycle-time dependency of soft error rate

(2) Countermeasures against soft errors

The error rate of 64 k DRAM is expected to exceed the target specification value according to forced irradiation test results. Consequently, the following countermeasures have been taken to reduce soft errors.

(a) Utilize package material emitting less α particle

(b) Utilize chip coating technology to prevent α particle peneteration

(c) Utilize circuit design and layout technology to withstand α particle penetration

Due to these countermeasures, soft errors in 64 k DRAM are not a problem any longer in practical use. Figure 2-7 shows an example of soft error reduction in 64 k DRAM. For masks 1 and 2, chip coating technology has been used to reduce soft errors. With the advance of layout technology (c), chip coating is not necessary for masks 3 and 4. The improved technology for 64 k DRAMs is also utilized for 256 k DRAMs to solve the soft error problem.

(3) Suggested countermeasures for system devices

As described so far, Hitachi has been taking various countermeasures against soft error to a satisfactory degree. The reliability of a system will be much more enhanced if the ECC function is added for large memory systems, and the parity bit for small systems.

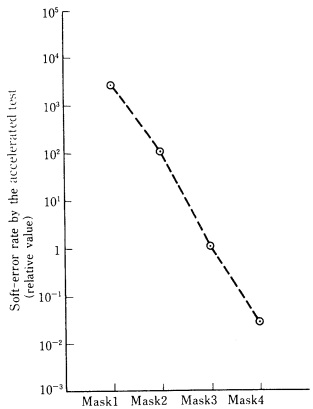


Fig. 2-7 Improvement in soft error rate of a 64K DRAM

2.1.3 Multilayer line technology using the resin insulation method

As one of the multilayer line technologies to raise the density of monolithic LSIs, Hitachi has developed a resin insulation method using polymeric resin for insulating material between line layers, and has been mass-producing LSIs for more than 10 years using this technology.

The process and materials used by this resin insulation method, particularly Polyimide Isoindro Quinazolinedione (PIQ), are originally Hitachi's technology.

Currently, LSIs with 3-layered line have been partially developed, but most LSIs still have 1- or 2-layered line. This structure, as shown in Figure 2-8, is configured by the repetition of 1-layered line processing. Using this method, the steps in the insulator layer and conductor layer are formed on top of each other, and these layers become thinner at either side of the steps. Consequently, short

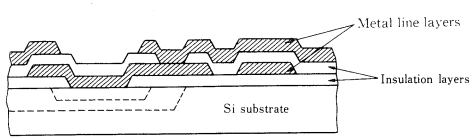


Fig. 2-8 A cross-section of the conventional 2-layer line structure

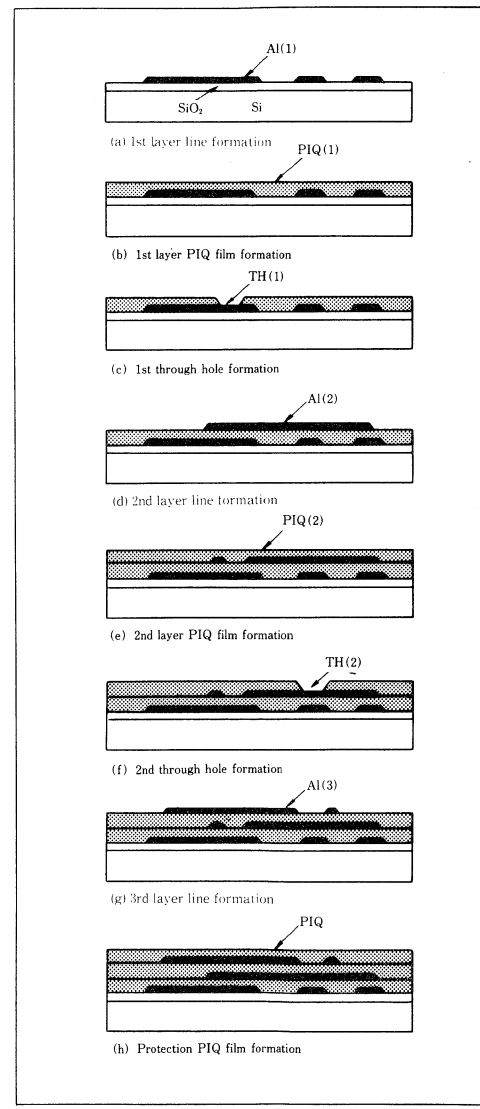


Fig. 2-9 PIQ layer process

circuits and disconnections in the conductor layer can easily occur at these points. Considering yield and reliability, up to 3-layered line can be allowed.

Accordingly, Hitachi, for the coming higher-integrated LSIs, has been trying to overcome failures in metal structure, and to develop new line technology to easily provide from 2- to 5-layered line. From among many trails for new metal line technology, Hitachi has developed a planar-type 2-layered line method, where thermosetting polymer resin is used for insulation film, and has mass produced LSIs using this method.

Additionally, for future VLSI devices, Hitachi has been developing ultra-fine processing and 3-layered line processing (Figure 2-9).

Scanning Electron Microscopy (SEM) photographs of the cross-section and surface of the 3-layered line structure are shown in Figures 2-10 and 2-11, respectively. These pictures show that the coverage of insulation film and metal line at the steps is extremely good and that there is no possibility of disconnection at these points.

Although the through hole is configured by ultra-fine processing, the taper is etched at an angle of 60° providing roundness. Disconnection, therefore, cannot occur since the coverage of Al line is satisfactory at this point.

Table 2-1 shows reliability test results of resin-sealed multilayer line LSIs using PIQ. The test results are satisfactory because of the stability of the component and corrosion protection effect for metal line, and the stability and higher reliability of the line structure itself.

The following describes the main features of PIQ.

(1) Good heat resistance: up to 450°C for 3 to 4 hrs.
(2) Good metal line coverage due to good flatness in multilayer line structure,
(3) Thick film formation on Si wafer: no cracks even at a film thickness of 10μ
(4) No cracks due to temperature change: no cracks from −196°C to +150°C of thermal shock.
(5) Good processability: processing by photoresist

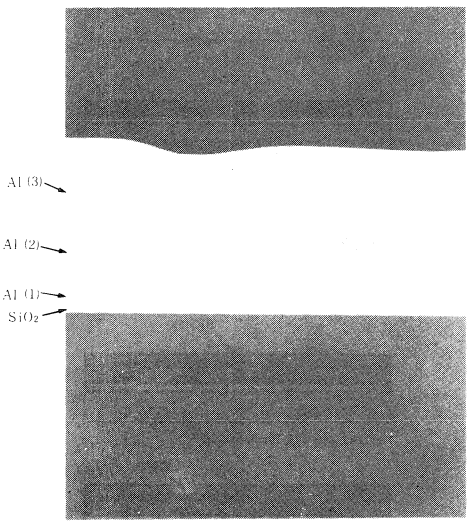


Fig. 2-10 A cross-section of three-layer lines

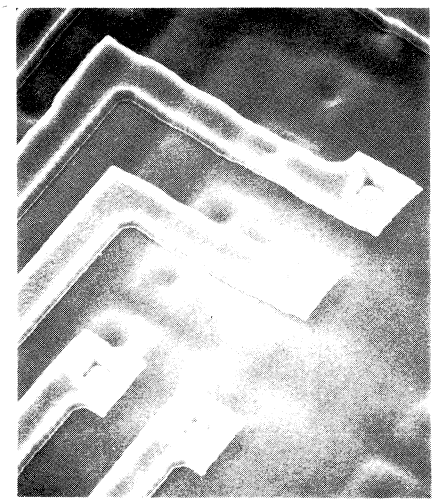


Fig. 2-11 The surface of a three-layer line LSI (by SEM)

2.1.4 Various types of breakdown protection circuits

Semiconductor devices may be damaged due to excessive stress caused by electrostatic discharge, surge, etc. Examples of improved circuits by installing protection circuits for electrostatic discharge, surge, and excessive load are described in the following.

2.1.4.1 Electrostatic breakdown protection circuit

Device breakdown by electrostatic discharge can generally be prevented by using the devices under moderate conditions following prescribed precautions. This is because a protection circuit is provided to strengthen the resistance against electrostatic breakdown as long as the performance of LSIs (operating speed, oscillation frequency, etc.) is not sacrificed. Figure 2-12 shows examples of electrostatic breakdown protection circuits; P-channel MOS IC (a), and bipolar IC (b). Each figure shows the equivalent circuit and cross-section. In the cross-section, the leak path of impressed electrostatic pulse is indicated by an arrow. Each protection circuit protects internal components from electrostatic damage by leaking static electricity to the IC board (GND) or power supply (Vcc) and by clamping the excessive input voltage at a constant voltage. Figure 2-13 shows electrostatic breakdown strength of typical Hitachi semiconductor devices.

Testing is carried out by the condenser discharge method, where a 200 pF condenser is used considering the capacitance of the human body. Generally, more than 200 V of breakdown strength is guaranteed except for ECL and the like, which require high-speed operation. Such types of LSIs cannot employ prevention circuit effectively.

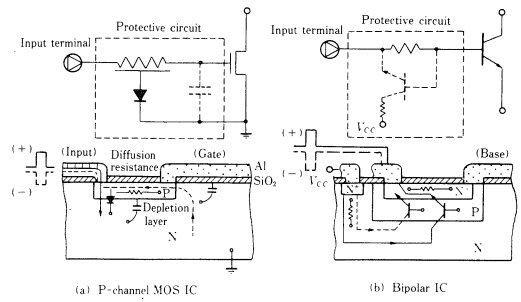


Fig. 2-12 Examples of protective circuits against electrostatic breakdown (Upper; Equivalent circuit, Lower; Cross-section)

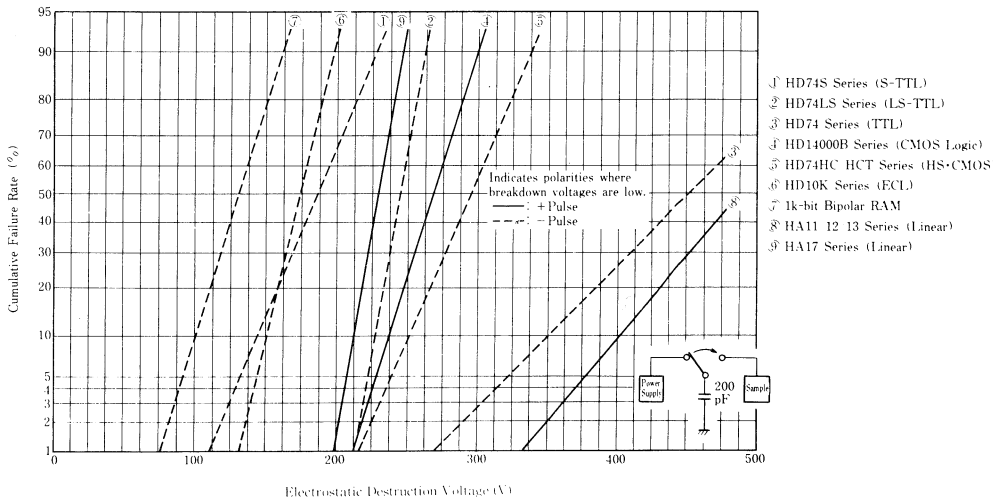


Fig. 2-13 An example of electrostatic breakdown voltages of ICs (1)

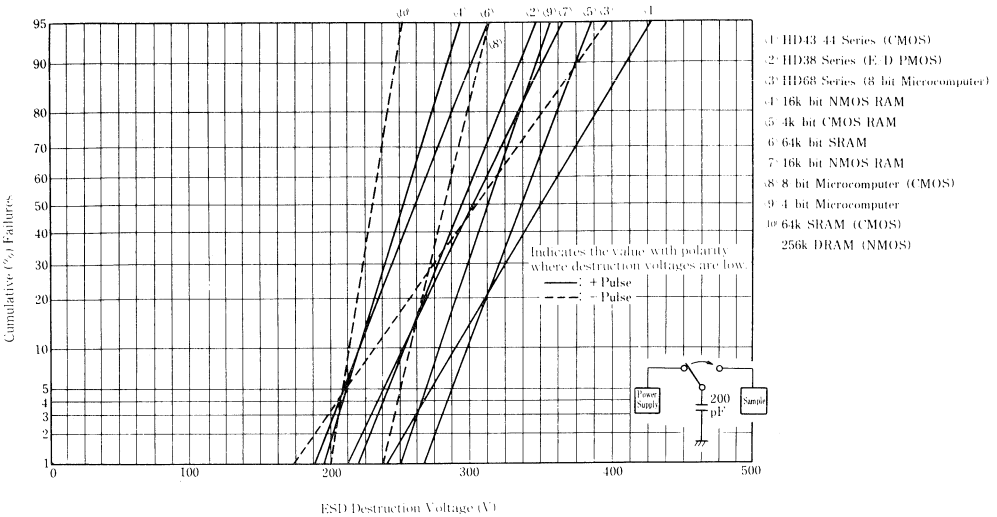


Fig 2-14 An example of electrostatic breakdown voltage of ICs (2)

2.1.4.2 Protection circuit for power IC

Power ICs for output amplification, which are mainly mounted ICs, incorporate a thermal shutdown circuit and surge protection circuit. If junction temperature reaches about 150°C, the thermal shutdown circuit begins operation. The thermal shutdown circuit protects ICs from damage by automatically controlling output, restraining heat, and keeping junction temperature below 150°C, in spite of a continuous short circuit load. Another problem is the destruction of mounted devices caused by overlapped surge onto the Vcc line. The surge protection circuit is provided to solve this problem. ICs are protected from surge destruction by inverse voltage of transistors and stopping amplifier operation, when surge voltage is applied to the power supply pin of the power IC. For example, the HA13108 has been improved so as not to be destroyed if 0.2 sec surge voltage is applied to the power supply pin at 50 V of peak voltage. Currently, new ICs containing ASO protection circuit are being developed. Hitachi is trying to enhance reliability by increasing the destruction margin.

2.1.5 Assembly technology

The assembly process refers mainly to the die bonding process to attach a chip onto a package, and the wire bonding process to connect terminals of a chip to leads. The reliability is greatly affected depending on the level of assembly technology. The following describes the main failure modes which are likely to occur during the assembly process.

(1) Bonding open, intermittent, short circuits
(2) Chip cracks
(3) Resistance increase and open due to Au-Al compound
(4) Bonding wire open due to repetitive thermal stress

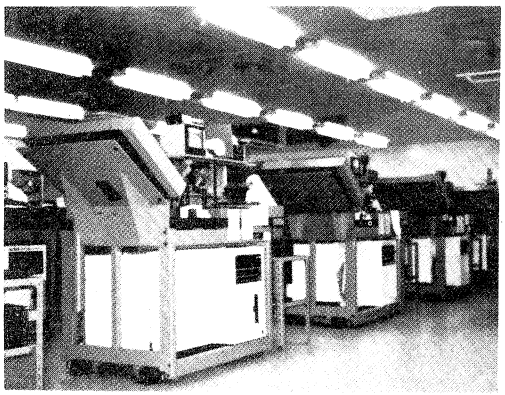


Fig. 2-15 Computerized automatic fabrication

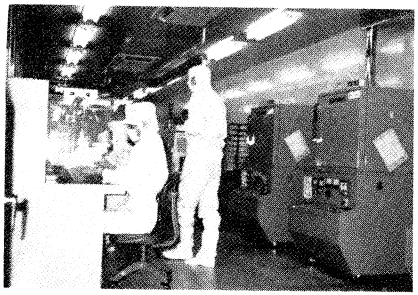


Fig. 2-16 Clean fabrication process

(5) Thermal resistance increase and chip peeling in soft solder type die bonding process

Hitachi is trying to enhance reliability by using appropriate designing and manufacturing technology to overcome these failures.

(1) Wafer dicing

Employing the diamond scribing method which has been widely used so far, cracks and chips on the pellet may occur. These failures are decreased by using the wafer dicing method where a wafer is diced by rapidly revolving a thin blade consisting of diamond powder congealed by a special metal.

(2) Automatic pellet bonding

There are several types of pellet bonding methods according to device characteristics.

(a) Au-Si eutectic alloying method

(b) Conductive adhesive method

(c) Soldering method

(d) Glass method, etc.

For each method, Hitachi adopts and automatic pellet bonding system on the mass-production line to upgrade quality and reliability of devices.

(3) Automatic wire bonding

Hitachi has developed and adopted an thermocompression automatic wire bonding system which can be controlled by computer (Figure 2-15). For quality control during processing, microwiring within a die is controlled by using SEM in addition to the usual visual inspection prior to sealing to upgrade device quality. Also, reliability is enhanced by keeping the assembly process clean (Figure 2-16).

2.1.6 Sealing technology

2.1.6.1 Plastic sealing technology

There are two types of sealing methods for semiconductor devices; one is an airtight sealing method using metal, ceramic or low fusion-point glass, and the other is a plastic sealing method using plastic material. As for airtight sealing, there is no peculiar problems concerning both material and technology. Airtightness is guaranteed through large and small leak tests. On the other hand, the plastic sealing method introduced to lower cost has enlarged the application field of semiconductor devices. Currently, devices completed by plastic sealing are very common among semiconductor products. This section describes reliability features of plastic-sealed devices.

There are mainly two types of failure modes for plastic-sealed devices; one is disconnection of electrode line due to aluminum line corrosion, and the other is wire bonding disconnection.

The former is caused by water molecules penetrating the boundary between plastic and lead frame or through the plastic material itself. These water molecules corrode electrode line and finally causes disconnection depending on impurity ions, voltage between electrode lines, and temperature.

The latter mode is caused by internal stress due to temperature change. Since the coefficient of thermal expansion and elastic modulus differs depending on component materials (Si chip, bonding wire, lead frame, plastic), the bonding wire, which is the weakest point, can be disconnected due to excessive internal stress caused by temperature change.

In addition to these failure modes, influence on electrical characteristics of other device types has been taken into

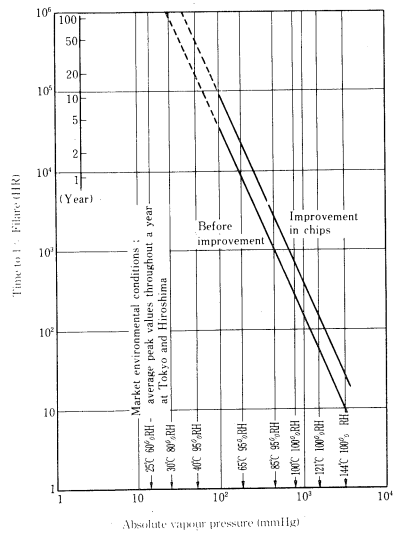


Fig. 2-17 Humidity dependency of a PIQ 2-layer metal line product and improvement

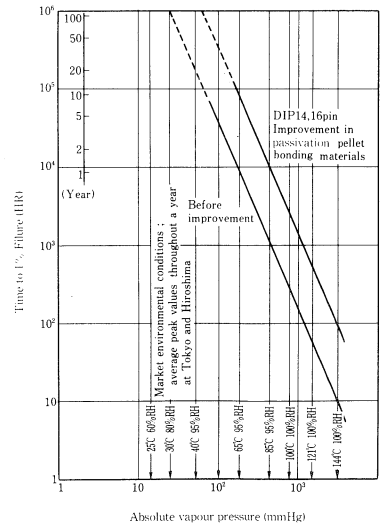


Fig. 2-18 Humidity dependency of a PIQ 1-layer line product and improvement

consideration. Considering all of these, Hitachi has systematically improved plastic material, molding technology, structure design, surface stabilization film of pellet bonding material, etc.
Figures 2-17 and 2-18 show improved moisture resistance of plastic-sealed ICs, taking PIQ 2-layered line products and 1-layered line products as examples.

2.1.6.2 Flameproofing of plastic-sealed devices

Resulting from the occurrence of TV fires, a UL (Underwriter's Lab. Inc.) standard has been established for plastic material in U.S.A. Hitachi finds flameproofing of plastic-sealed devices important to ensure product stability, and adopts the material with the highest flameproofing range V-0 defined by the UL94 standard. Table 2-2 shows flameproofing evaluation criteria of V-0 and HB (non-flameproofing).

2.1.7 Miscellaneous technology

Other than the technologies described above, Hitachi has improved such technologies as crystal processing, epitaxial growth, impurity diffusion, ion implantation, and photo etching.
Noise and leakage current of semiconductor devices result mainly from internal and surface defects or contamination of the crystal. Hitachi has tried various kinds of improved methods concerned with manufacturing, materials, equipment, and environment in the processes described above to eliminate these failures. For instance, product stability is ensured by adopting a method to decrease adverse effects due to surface polishing during crystal processing, a wafer rear face processing method to prevent lamination failure occurring at surface oxidation or diffusion, and an anneal method which is effective against lamination failure, and by improving materials used for photoresist and glassmask.
In addition, new automatic equipment for mask alignment or ion implantation has been utilized aiming at a full automation process. Hitachi has upgraded a variety of technologies pursuing cleanliness in the processing line, the first prerequisite in semiconductor manufacturing.

Table 2-2 UL94 Flameproofing Evaluation Criteria

V-0 (Vertical ignition 0 level)	HB (Horizontal ignition level)
A. Flaming within 10 sec after removing flame.	A. Burning rate below 1.5"/min when igniting the thickest specimen kept horizontally.
B. Flaming within 50 sec after applying flame to 1 set of 5 pieces 10 times.	
C. No flaming or glowing to pressure jig.	
D. No dropping of flaming grain ignition cotton below 12".	
E1. Glowing within 30 sec if removing flame ignited again after the procedure above.	
E2. Glowing but not igniting cotton after 10 sec have passed if removing flame ignited again after the procedure above.	

2.2 HITACHI'S PHILOSOPHY OF QUALITY AND RELIABILITY

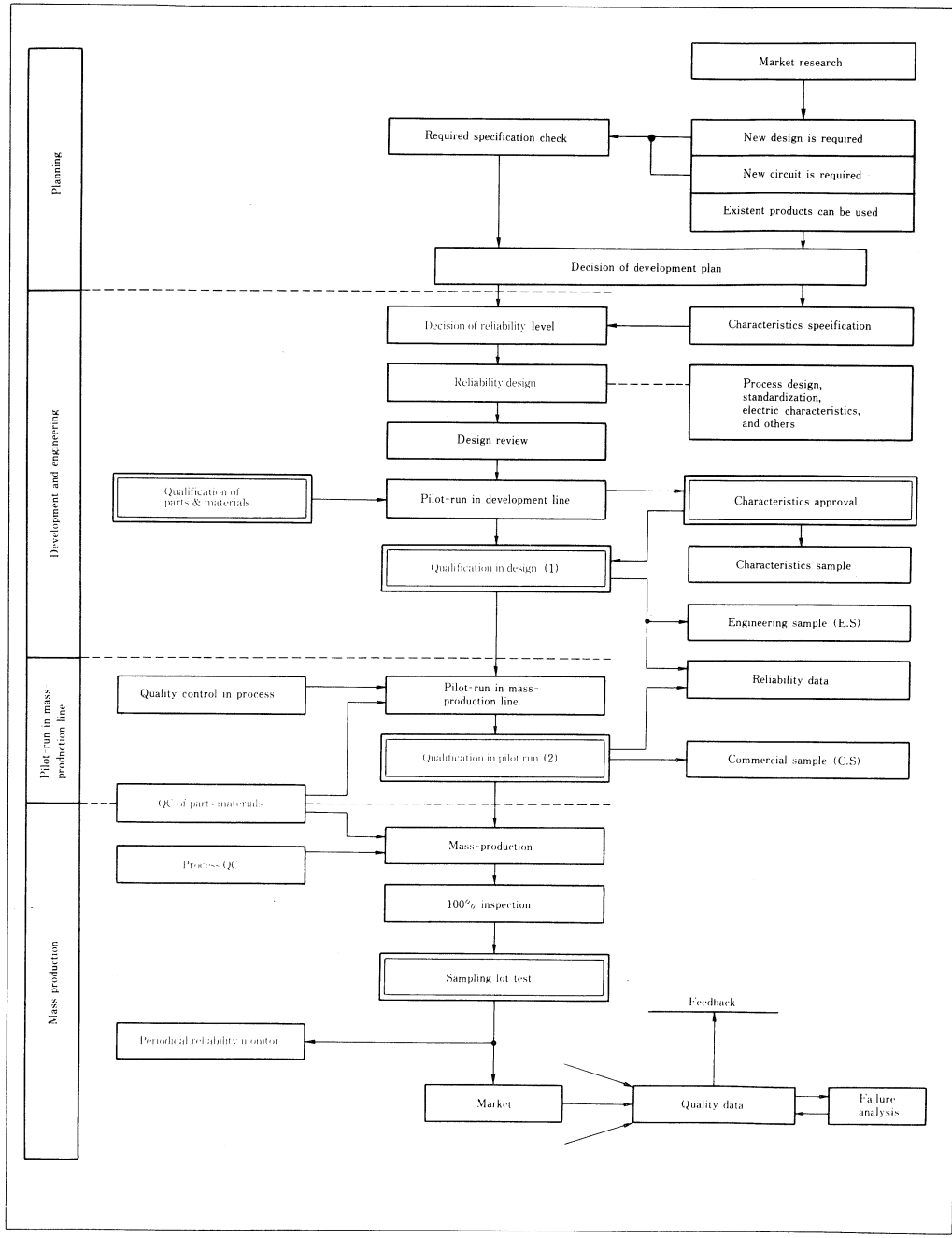
Hitachi is always pursuing higher quality to meet individual users' and markets needs. User requested quality is clearly specified by contract in some cases, but is not very clear in other cases. Nevertheless, Hitachi is constantly trying to upgrade reliability so that all devices fully demonstrate their high performance in practical use.
To ensure better quality, Hitachi finds it important to establish quality control systems and to enhance quality consciousness in the manufacturing process. With the advance of device performance and expansion of application fields, the quality level needed by users is rising every year. Hitachi defines the following strategy to ensure better product quality.
(1) Consider fully reliability when developing new products
(2) Specify product quality at the beginning of the manufacturing process
(3) Strengthen inspection and reliability test of finished products
(4) Satisfy PPM target value by intensively pursuing failure potential from field data and test data
Table 2-3 shows an example of a reliability program. In this way, Hitachi is always trying to enhance the quality level and reliability of devices so as to fully satisfy users' needs.

2.3 RELIABILITY DESIGN FOR SEMICONDUCTOR DEVICES

2.3.1 Reliability target

Reliability target is an important item along with function and price when fabricating and marketing products. It is not practical to define a reliability target according to the failure ratio under a specific test condition. Hitachi, therefore, defines quality control at engineering, manufacturing, and processing sections, for screening, testing method, etc, depending on characteristics of each device by collectively considering environment where the device is used, target reliability of a system, derating, operating condition, maintenance, etc.

Table 2-3 An example of reliability programs



2.3.2 Reliability design

To satisfy requested reliability according to a reliability target, the following should carefully be examined and executed.

(1) Design standardization

To standardize device design, design rules must be defined, and parts, material, and processes standardized. For design rules, Hitachi always gives critical consideration on quality and reliability when defining rules for circuits, component, layout design, etc. Therefore, even for newly developed products, reliability is hardly affected as long as the standardized processes and materials are utilized.

(2) Device design

Collective device design is necessary in terms of circuit, layout, process and structure design. Especially when utilizing new processes or materials, Hitachi fully examines design technology prior to device development.

(3) Reliability evaluation by TEG

TEG (Test Element Group), sometimes called a test pattern, is an effective method to evaluate reliability of complicated IC and LSI design methods, and their manufacturing processes. It is also effective for transistors to raise their failure detection probability when applying new processes. The following describes TEG.

(a) Purpose of TEG

- ○ Define basic failure modes
- ○ Define relation between failure mode and manufacturing process conditions
- ○ Analyze failure mechanisms
- ○ Define QC points for manufacturing, etc.

(b) Evaluation of TEG effectiveness

- ○ Can evaluate common basic failure modes and failure mechanisms
- ○ Can make comparisons with actual user operations by identifying factors causing failure modes
- ○ Easily understood relations between cause of failures and process factors
- ○ Easily executable tests

As specific examples, types and pattern examples of TEG used in MOS IC are shown in Table 2-4 and Figure 2-19, respectively.

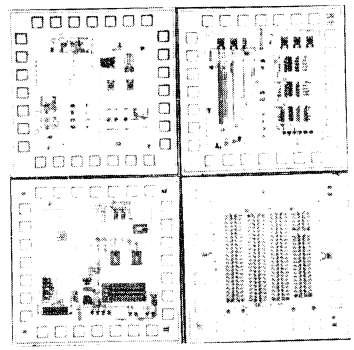


Fig. 2-19 An example of TEG pattern

Table 2-4 TEG types and check items

No.	Component		Check item
1	MOS transistor	Active MOS	Fluctuation in V_{TH}, and gm Fluctuation in junction voltage durability Fluctuation in leak current
2		Parasitic MOS	Fluctuation in field V_{TH} Fluctuation in junction voltage durability Fluctuation in leak current
3	Fundamental circuit	Unit cell	Fluctuation in operational margin Fluctuation in frequency characteristics Fluctuation in leak current
4	Contact		Degradation in ohmic characteristics Fluctuation in resistance value Fluctuation in leak current
5	Metal line		Fluctuation in resistance value

2.3.3 Design review

Design review is a systematic method to recognize whether or not the requested performance is fully satisfied, designing service is carried put in a specifies manner, technical improvement matters given by experiment data, field data, etc. are effectively taken into consideration. Also, design review is executed to enhance and ensure quality and reliability of products, in order to compete effectively with other developers.

Table 2-5 Design review standard

	Hitachi design review standard	NASA design review standard
Purpose	Reliability assurance required from the market	Guarantee for performance required by the space program
Definition	Promotion of systematic confirmation for various technical abilities	Systematic application of various technical abilities
Checking item	Correction of design failure	Correction of design failure
Checking subject	Specified products	Contracted projects
Period	Planning Intermediate design Final design	Preparation Before assembly Before issue
Organization Chairman of committee	Chief of designers	A person specified by the project manager
Members of committee	Manager in related dept., and a manager concerned with reliability	Manager or someone of upper rank and a manager concerned with reliability
Authorized limit of rights	Recommendation for improvement	Advise

Hitachi executes design review on new products as well as modified products from the stage of product planning.
This type of method is utilized in NASA. Table 2-5 shows comparison of design review criteria between Hitachi and NASA.
The items to be reviewed are as follows.

(1) Describe product according to design document
(2) Plan and execute subprograms such as calculations, experiments, or investigations, examining design document by specialists in various fields, if there is something unclear about design documents
(3) Determine reliability test contents and methods according to design document and drawings
(4) Check whether or not processability in the manufacturing workshop is sufficient to satisfy the design target
(5) Discuss production preparation
(6) Plan and execute subprograms such as tests, experiments, or calculations, to change device design following the suggestion of each specialist, or to determine such a change
(7) Review failure examples of similar products and determine preventive measures; plan and execute experimental programs to validate these measures

Hitachi performs the design review according to a check list specially defined for each product.

2.4 QUALITY ASSURANCE SYSTEM FOR SEMICONDUCTOR DEVICES

2.4.1 Quality assurance activity

This section describes Hitachi's general philosophy of quality assurance.

(1) Solve each process's problems; remove any potential failure factors in completed products
(2) Utilize feedback information to maintain good processability condition
(3) Ensure requested reliability and better quality by performing the above

The following sections describe quality control, reliability testing, etc.

2.4.2 Quality qualification

Hitachi executes quality qualification at sampling and mass-production to ensure requested quality and reliability, according to the reliability design described in section 2.3. The following shows the philosophy of quality qualification.

(1) Execute objective qualification from the customer's viewpoint
(2) Fully consider past failure specimens and field information
(3) Execute qualification also when design and process are changed
(4) Execute elaborate qualification for parts' materials and processes
(5) Determine control points at mass-production by examining processability and factors causing scatter

Hitachi executes the quality qualification shown in Figure 2-20, considering the above.

2.4.3 Quality and reliability control in mass-production

Hitachi controls product quality by effectively dividing the work between manufacturing section, inspection section, etc, as shown in Figure 2-21.

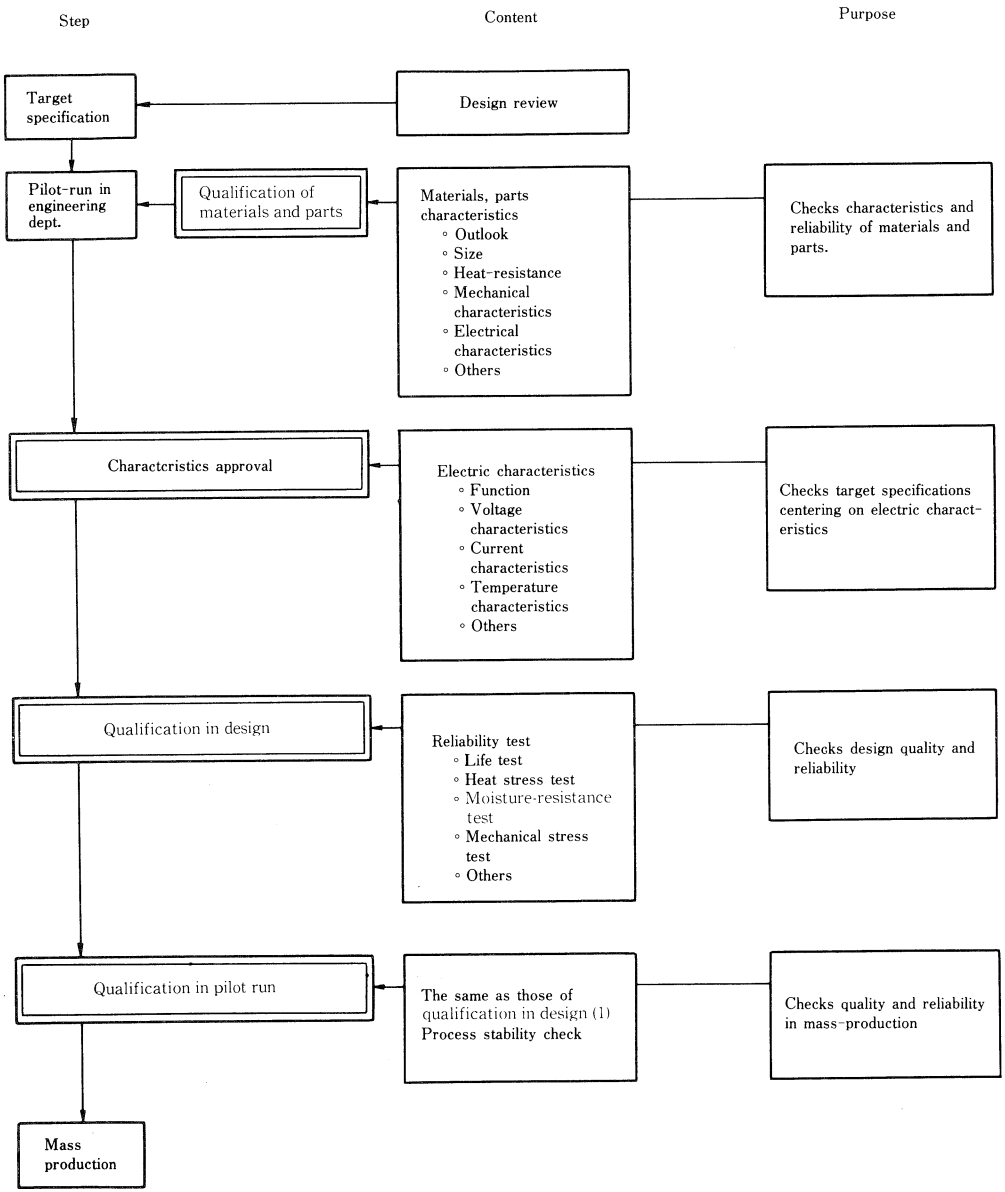


Fig. 2-20 Flowchart of quality authorization

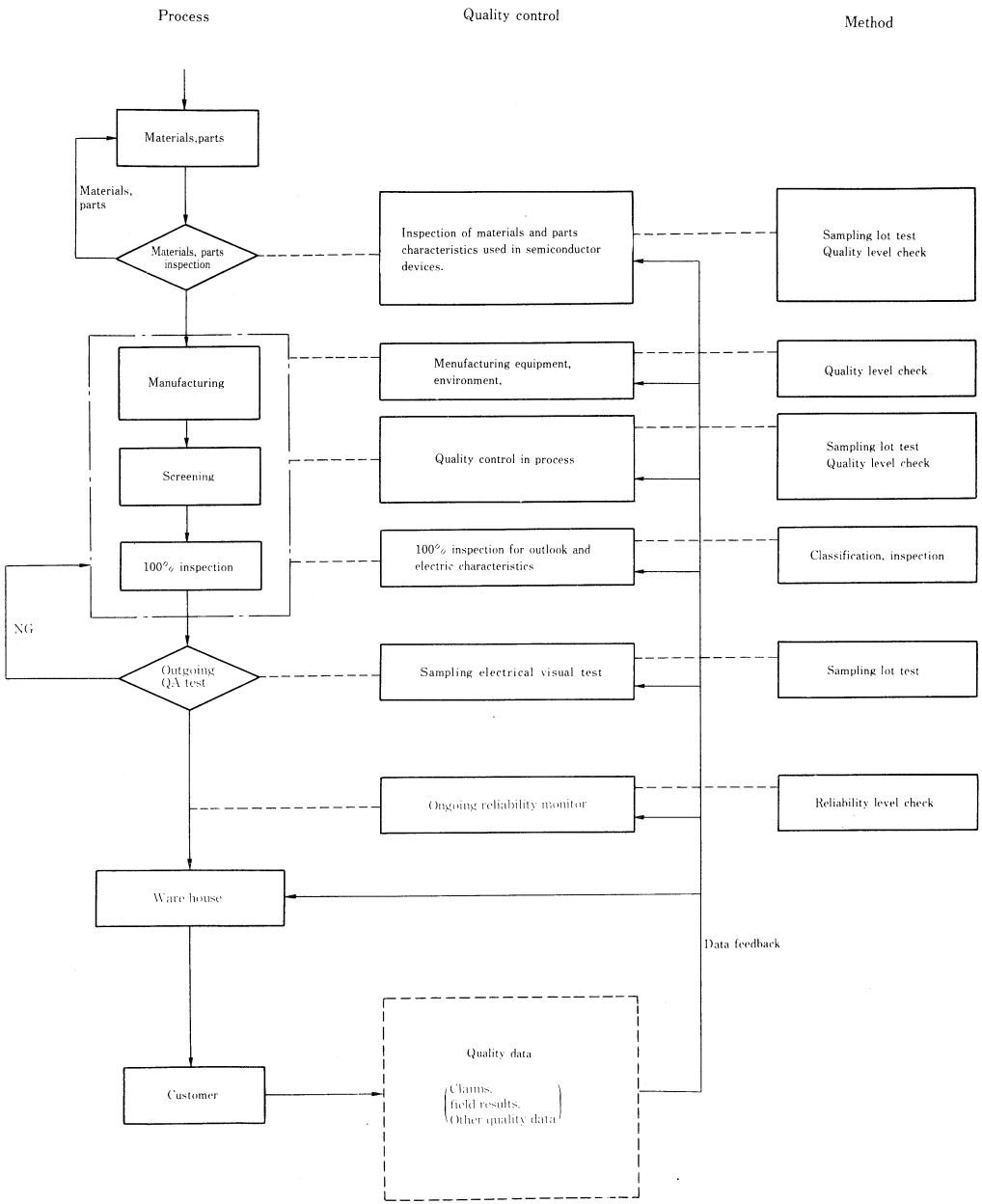


Fig. 2.21 Flowchart of product control in manufacturing process

2.4.3.1 Quality control of materials and parts

With the advance in performance and reliability of semiconductor devices, quality control of materials and parts which are necessary to fabricate products, such as crystal, lead frame, bonding wire, package, etc, and of materials which are necessary in the manufacturing process such as mask patterns, chemicals, etc. is becoming more and more important. For quality control of materials and parts, incoming inspection is executed in addition to qualification of materials and parts. Sampling inspection following MIL-STD-105D is carried out for incoming inspection according to the incoming inspection standard defined by purchase specifications and drawings.

The following items are also carried out for quality control.

(1) Liaison meeting for purchasing external technology

(2) External order qualification, external order guidelines

(3) Physical and chemical analysis and testing

Table 2-6 lists the primary check points for materials and parts.

2.4.3.2 Internal process quality control

Internal process quality control is extremely important to ensure better quality of devices. The following describes how to control partially fabricated products, finished products, manufacturing equipment, measuring instrument, manufacturing environment, and sub-materials. Figure 2-22 shows an example of Internal process quality control.

(1) Quality control of partially fabricated products and finished products

Potential failure factors must be removed in the manufacturing process. Hitachi defines check points in each process and never delivers a product with a failure factor to the following process. Especially for high-reliability semiconductor devices, the manufacturing line is carefully selected, and precise quality control is executed for internal processes. Hitachi carefully checks each product lot in each process, executes 100% inspection in appropriate process to remove failure factors due to scattered manufacturing, and

Table 2-6 Check points for controlling materials and parts quality

Material/parts	Items to be controlled	Check items
Wafer	Appearance	Surface damage and contamination
	Size	Flatness
	Specific resistance	Resistance value
	Defect density	Number of defects
	Crystalline axis	
Mask	Appearance	Number of defects and flaws
	Size	Dimensional level
	Registration	
	Shading	Deviation in shading
Thin wire for wire-bonding	Appearance	Contamination, flaws, deflection, and twisting
	Size	
	Purity	Purity level
	Elongation ratio	Mechanical durability
Frame	Appearance	Contamination and flaws
	Size	Dimensional level
	Processing accuracy	
	Plating	Bondability and solderability
	Assembly characteristics	Heat resistance
Ceramic package	Appearance	Contamination and flaws
	Size	Dimensional level
	Air-tight leakage	Air-tightness
	Plating	Bondability and solderability
	Assembly characteristics	Heat resistance
	Electric characteristics	
	Mechanical durability	Mechanical durability
Plastic	Composition	Characteristics of materials
	Electrical characteristics	
	Heat characteristics	
	Moldability	Moldability
	Assembly characteristics	Assembly characteristics

Process	Control Points		Purposes	
	Material purchase			
Wafer		Wafer	Characteristics, Visual	Eliminate flaw and crystal defect
	Surface oxidation	Oxidation		Ensure resistance value
	Surface oxidation inspection		Appearance, Oxidation film thickness	Recognize pin-hole and flaw
	Photoresist	Photoresist		
	Photoresist inspection		Dimension, Visual	Recognize dimension level
	◇PQC level check			Check photoresist condition
	Diffusion	Diffusion	Diffusion depth, Resistivity	Recognize diffusion condition
	Diffusion inspection		Base width	Control basic characteristics (h_{FE} etc.)
	◇PQC level check		Oxidation film characteristics	Check cleanliness and V_{TH}
			Breakdown voltage	Check breakdown voltage level
	Deposition			
	Deposition inspection	Deposition	Deposition film thickness Flaw, Contamination	Ensure standard film thickness
	◇PQC level check			
	Wafer inspection	Wafer	Wafer thickness	Reduction of voids, Scratches, discoloration
	Chip electrical inspection	Chip	Electrical characteristics	
	Chip scribing		Visual inspection	
	Chip visual inspection			
	◇PQC lot acceptance		Visual after bonding	Check die bonding quality
Frame				
Bonding wire	Die bonding	Die bonding	Visual after bonding	Check wire bonding quality
	Wire bonding	Wire bonding	Tensile strength, Application width shear strength	Prevent of wire short-circuit, Open-circuit
	◇PQC level check			
	Inspection after assembly		Inspection after assembly	
	◇PQC lot acceptance			
Package				
	Sealing	Sealing	Visual inspection after sealing	Ensure appearance and dimension
	Lead forming	Lead forming	Visual, Dimension	
	Marking	Marking	Marking strength	
	◇PQC level check			
	Final electrical inspection			
	◇Failure analysis		Failure analysis, Failure mode, mechanism	Feedback analysis information
	Visual inspection			
	Sampling inspection			
	Register			
	Delivery			

Figure 2-22 Example of Quality Control inside Process

Table 2-7 Reliability result for MOS memory

Test items	Testing conditions	Notes
Temperature Cycle test	−55°C–150°C 10 cycles	
High-temperature operation test	125°C, 48hrs	
	125°C, 1000hrs	
Humidity resistance	85°C 85%RH Bias 1000hrs	Plastic

performs necessary screening such as high-temperature aging, temperature cycle, etc.
The following lists the contents of internal process quality control.

- Control conditions for each piece of equipment and employee, and execute sampling inspection of partially fabricated products
- Propose and execute service improvement
- Educate employees
- Maintain and enhance yield
- Pick out problems on products and carry out countermeasures
- Communicate quality information

(2) Quality control of manufacturing equipment and measuring instruments

Manufacturing equipment is more and more advanced with higher-performance of devices and rationalization of production, and is extremely important to determine product quality and reliability. Hitachi promotes automation of manufacturing equipment to prevent manufacturing scatter, and controls each piece of high-performance equipment to operate and function appropriately.
Two types of checks are executed to control quality: daily check and periodic check. Every check point listed in the standard is thoroughly and carefully checked.
As for calibration of measuring instruments, calibration period is determined by defining custody no., specification, and calibration hysteresis. Measuring instruments are carefully checked according to the standard by using an officially qualified calibrator to ensure better quality.

(3) Quality control of manufacturing environment and submaterials

Quality and reliability of semiconductor devices greatly depends upon manufacturing processes. Hitachi fully controls the manufacturing environment such as temperature, moisture, dust, etc, and sub-materials such as gas and demineralized water. The following describes dust control.

Dust control is essential to realize higher-integration and higher-reliability. Hitachi maintains and promotes cleanliness in the workshop by periodically checking indoor floating dust, falling dust, floor soil, etc., paying attention to various points such as buildings, equipment, air-conditioning equipment, delivered goods, work clothes, service, etc.

(4) Control of changes

Hitachi defines procedures for any changes and determines product quality to maintain better quality and to prevent any failures after changes in manufacturing specification, working conditions, jigs, parts' materials, manufacturing section, etc.
For quality determination, Hitachi recognizes whether or not the requested quality and reliability is satisfied by executing qualification tests.
Depending on the contents of changes, customer's approval may be needed. In this case, Hitachi carries out discussions and coordinations between related sections prior to changes.

2.4.4 Failure management

If any failure is detected in a product after delivery, the product shall be returned to Hitachi by the request of customers or Hitachi. In this case, Hitachi's Marketing dept and Technical Marketing dept, together with Quality Assurance dept, should examine the product, conditions where it was used, period when it was used, conditions when the failure occurred, etc, and make appropriate response to the customers as soon as possible. Quality Assurance dept, in cooperation with engineering and manufacturing depts, should clarify the cause of failure and supply feedback to engineering and manufacturing depts, to prevent the failure from occurring again. Figure 2-23 shows how Hitachi manages failures.

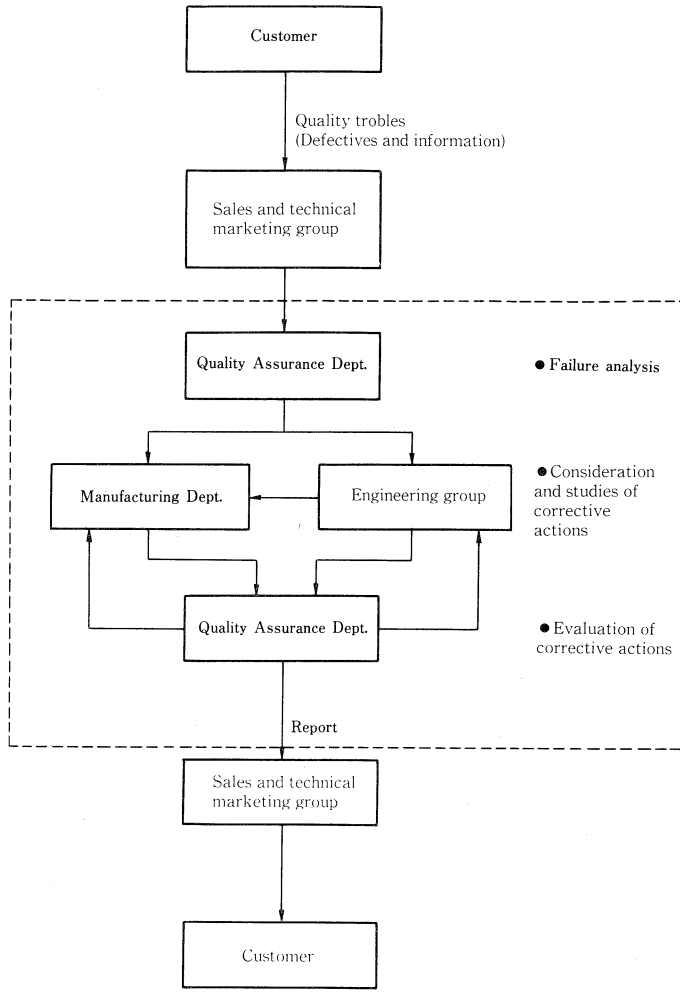


Fig. 2-23 A flowchart of transaction system for failures occurring customer sides

2.4.5 Reliability data collection

Hitachi estimates the field failure rate from process evaluation and reliability tests inside the company. This estimation is done by analyzing field data of similar products, or, in other words, quality information among users and markets. Figure 2-24 shows the failure rate trend of transistors, ICs, and LSIs used for components of large systems, as an example of field data. According to this figure, reliability of ICs and LSIs is being upgraded year by year. In this way, Hitachi pays careful attention to products after delivery, collects information from users, analyzes failures, and provides feedback quickly to engineering and manufacturing depts. The following describes field information and how it is used.

As for field data information,

- Early quality data on the device level
- Process data and early failure data on the sub-system level
- Debugging data such as burn-in on the system level
- Market data on the system level

are analyzed and effectively utilized to determine an attainable reliability target level, improve reliability design, process, acceleration tests, etc.

Field information is so important to ensure better reliability of products that it is directly collected from users through technical liaison meetings and the like.

In addition, Hitachi takes part in domestic and overseas data-exchange programs, and utilizes the obtained information to upgrade reliability.

As for data-exchange programs, the following are utilized.

- ? electronic parts reliability data-exchange program
- ? (RCJ) electronic parts reliability data-exchange program
- GIDEP (U.S.A.)
- EXACT (Europe)

Table 2-8 shows the RCJ field data sheet as an example.

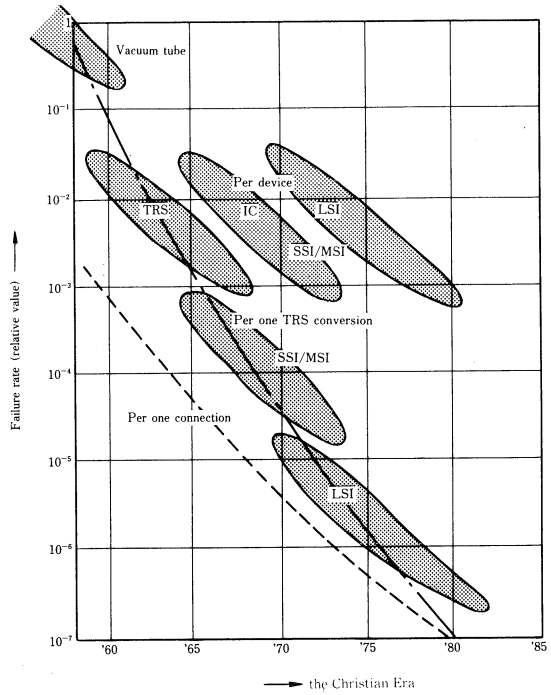


Fig. 2-24 The transition of the failure rate of semiconductor devices in a large-scale system

Table 2-8 Field Data Sheet

Prepared
Registered

① Company or Institute Name		Person in charge	Section
Address			Name Tel.

② Parts Code		⑤ Equipment Code	
Parts Name		Equipment Name	
STD No.		Parts structure, Ratings, Circuit Format, etc. (In case of no standard for similar products)	
Type No.			
③ Parts Supplier Name			
④ Installed Location	(a) Air-conditioned room (b) Ordinary room (c) Train (d) Automobile (e) Airplane (f) Ship (g) Portable (h) Outdoors (i)		

Conditions	⑥ (a) Used circuit	(1) Analog (2) Digital (3) Analog-Digital (4)
	⑦ (b) Ambient temperature Average (Max.)	(1) Below 0°C (2) 0 to 40°C (3) 40 to 60°C (4) 60 to 80°C (5) Above 80°C
	⑧ (c) Cooling method	(1) Natural cooling (2) Forced cooling (3) Other method ( )
	⑨ Ratings percentage (%)	(1) Below 20% (2) 20 to 50 (3) 50 to 80 (4) Above 80% of power , current, or voltage
	⑩ Operating Condition	(1) Continuous running (2) Average operating period/day (3) Average operating cycle
	⑪ Environment	(1) Heavy vibration (2) High dust (3) High moisture (4) Others ( )

⑫ Number of Units of Equipment		⑬ Number of Parts/ Equipment		⑭ Component Time T (10^4)	
Manufacturing Date		Running Start Date		Parts Component Time T (10^5) (Represented by numbers)	
⑮ Number of Failures	Breakdown maintenance		Total	⑯ Failure Rate fit (10^{-9} time) (Point estimation)	
	Preventive maintenance				

⑰ Number of Parts according to failure mode by breakdown maintenance.

Short circuit		Contamination	
Open circuit		Ambignous	
Breakage		Others	
Characteristics Value degradation			
Corrosion			

⑱ By preventive maintenance

(a) Individually check and exchange parts or sub-unit (Write change rate to nominal value, if checking characteristics value of parts)

Parameter	Number of parts	Change rate (%)

(b) Periodically change parts or sub-unit.
(After hrs. have passed)

Comments by Parts Supplier

Code column

①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬

⑭	⑮	⑯	⑰	⑱

(From RCJ)

3. RELIABILITY TEST METHODS AND TEST RESULTS

3.1 RELIABILITY TEST METHODS

3.1.1 For reliability testing, testing methods, testing conditions, and evaluation criteria should be appropriately selected depending on the product, its application, and test objectives. For example, the procedure for an endurance test is different from that of a test that checks whether or not device performance is passable under certain criterion.
Environmental factors (stress) are determined by taking device structures, processes, and operation conditions into account. There are many ways that stress can be applied; for example, single stress and combined stresses. Moreover, stress intensity and time-dependent stress should also be considered. In addition, we should check whether it is a screening or sampling test, and if a sampling test, sampling frequency should also be checked.
What is the most important factor in reliability testing is proper conjecture. At the same time, the test should contribute to improvement in device reliability. Accordingly, accumulation of actual reliability test results, failure analysis, and research on reliability improvement are required.

3.1.2 Reliability test methods

Standardized testing methods are required so as to obtain testing reappearance. These testing methods are determined by JIS standard, EIAJ standard, IEC standard, U.S. MIL standard, German DIN standard, and European CENELEC standard. Besides these, there are also standards registered by domestic government offices such as the Defence Agency, National Space Development Agency, NHK, JNR, and Japan Institute of Automobile Standards. From among these, generalized standards are shown in Table 3-1.
Among these standards, JIS C7021 and C7022 are registered with the JIS standard based on EIAJ standards SD-121 and IC-121. Their summary is shown in Tables 3-2 and 3-3. ① Test objectives, ② Equipment and materials necessary for testing, ③ Testing method, and ④ Failure check method are described in the summary column of these tables. Notes from actual testing are described in the testing-points column. In the related-standard column, ⓐ to ⓓ indicates JIS C7021, IEC Pub. MIL-STD-750B, and MIL-STD-883C, respectively.

Table 3-1 Reliability testing standard

JIS standards
- JIS C 7030: Testing Methods for Transistors
- JIS C 7031: Testing Methods for Small Signal Diodes
- JIS C 7033: Testing Methods for Semiconductor Rectifier
- JIS C 7021: Environmental Testing Methods and Endurance Testing Methods for Discrete Semiconductor Devices
- JIS C 7210: General Rules for Reliability Assured Discrete Semiconductor Devices
- JIS C 5700: General Rules for Reliability Assured Electric Components
- JIS C 5020 General Rules of Basic Environmental Testing Procedure for Electronic Components
- JIS C 5003: General Test Procedure of Failure Rate for Electronic Components
- JIS C 7022: Environmental Testing Methods and Entrance Testing Methods for Semiconductor Integrated Circuits.
- JIS C 7310: General Rules for Reliability Assured Digital Semiconductor Integrated Circuit.

IEC standards:
- Publication 68: Basic Environmental Testing Procedures.

CECC standards:
- CECC 50000: Generic Specification: Discrete Semiconductor Devices
- CECC 90000: Generic Specification: Monolithic Integrated Circuit

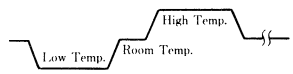
U S. MIL standards:
- MIL-STD-202E: Test Methods for Electronic and Electrical Component Parts
- MIL-STD-750B: Test Methods for Semiconductor Devices
- MIL-STD-883C: Test Methods and Procedures for Micro Electronics
- MIL-S-19500E: Semiconductor Devices, General Specification for
- MIL-M-38510C: Microcircuits General Specification for

Table 3-2 Summary of environment and weather resistance testing methods (JIS C 7022)

	Testing item	Summary	Notes on testing	Related standard (Note)
A-1	Soldering heat resistance test	① Checks heat resistance during soldering process. ② Solder component is Pb: Sn = 4:6 (H63A) ③ Dips device leads into solder of 260±5°C for 10±1 sec. as far as 1-1.5mm from the sample body. ④ Electrical characteristics	Dipping is performed one time	ⓐ A-1 ⓑ T ⓒ 2031.1

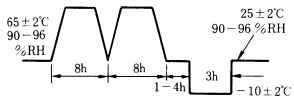
(Note) ⓐ JIS C 7021 ⓑ IEC Pub. 68. ⓒ MIL-STD-750B
ⓓ indicates the testing method number of MIL-STD-883C.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
A-2	Solderability test	① Checks the solderability of pins to be soldered. ② Solder component is Pb:Sn = 4:6 (H63A) Rosin isopropyl alcohol solution (25%) is used for flux. ③ Dips pins into solder bath of 230±5°C for 5±1 sec. after dipping them into flux. ④ Solder should be applied to more than 95% of the dipped portion. Pin holes or openings should not be concentrated on a certain portion, and their area should not exceed 5% of the total area.	Since a microscope of 10 to 20 magnification is used for this inspection and differences among individuals must be considered, it is recommended to prepare a limit sample.	ⓐ A-2 ⓑ 2-20 ⓒ 2026.2 ⓓ 2003
A-3	Thermal shock test	① Check device resistance against sudden temperature change. ② Two water baths of 100°C and 0°C. Pure water or supplied water (Condition A) ③ Method I: Devices are dipped in the hot bath for 15 sec. Next, they are transferred within 3 sec. and dipped in the cool bath. They are then transferred to the hot bath within 3 sec. after being dipped in the cool bath for at least 5 sec. This procedure is repeated 5 times. Method II: Devices are dipped in both baths alternately for 15 min., and the time for transfer is 10 sec, or less. ④ Electrical characteristics.	A temperature gradient is observed in a device, and stress strain occurs evenly with a uniform material. Measurement should be performed paying attention to bonding wire disconnections and pellet cracks. Fluorocarbon (FC-40, FC-77) is used in conditions B and C.	ⓐ A-3 ⓑ 2-14 ⓒ 1056.1 ⓓ 1011
	Temperature cycle test	① Checks device resistance against high and low temperatures and intermediate temperature changes. ② A high temperature bath and a low temperature bath having an air circulation system. ③ Example: low-temperature bath: 30 min. normal-temperature bath: 10 min. high-temperature bath: 30 min. normal temperature bath: 10 min. This procedure is repeated 5 times. ④ Wire breaks, short circuits, and electrical characteristics. 	Normally, Tstg max-min is selected. Since stress strain is generated in materials having different thermal expansion coefficients, care should be taken on the same points as the thermal shock test. Temperature change in each device differs depending on thermal capacity, thermal conductivity, and the number of devices. However, no special problem arises if the temperature changes in devices are within the range of Tstg max-min.	ⓐ A-4 ⓑ N ⓒ 1051.1 ⓓ 1010

(Note) ⓐ JIS C 7021 ⓑ IEC Pub. 68. ⓒ MIL-STD-750B
ⓓ indicates the testing method number of MIL-STD-883C.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
A-5	Temperature-humidity cycle	① Checks stability in a high-temperature high-humidity condition. ② A bath in which temperature and humidity are controllable by programming.  ③ 1 cycle: 24 hr. 10 cycles are carried out. 5 cycles of the low-temperature (−10°C) should be carried out before 9-cycle. ④ Electrical characteristics	Temperature must be controlled so that the temperature does not reach 100%RH. Opening/closing of the door should be performed when the temperature in the bath is normal. Distilled water or deionized water. pH: 6.0 ~ 7.2 ρ: 50 kΩ•cm	ⓐ A-5 ⓑ D ⓒ 1021.1 ⓓ 1004
A-6	Air-tightness test I (by He)	① Detection of slight leakage from a package. ② Puts a device in a closed vessel, and ③ He is pressurized at a prescribed time and pressure. Leakage detection is carried out by a mass analysis type leakage detector. Measurement is performed within 30 min. after the pressurization.	When leakage is great, a measurement error occurs because He escapes before the leak detection. It is recommended to check major leakage by performing the air-tightness test III (The reverse order is not possible).	ⓐ A-6 ⓑ Q_K ⓒ 1071.1 ⓓ 1014
	Air-tightness test II (by Kr^{35})	① Detection of minor leakage. ② Puts a device in a closed vessel, and ③ Measures the amount of Kr35 entering the device by pressurization using a scintillation counter.	Since this method involves a radioactive pollution problem, it has become less and less used.	
	Air-tightness test III (Test for major leakage by checking bubbles)	① Detection of major leakage in a package. ② Fluorocarbon (FC-48), silicon oil, or ethylene glycol. ③ Puts a device in the above solution heated at 125±5°C, and checks for bubbles appearing continuously from it. ④ If bubbles appear continuously from the same spot, it is considered that the device has a problem in air-tightness.	Since fluorocarbon evaporates at normal temperature, no washing is required after testing; however, it is quite expensive. In some cases, bubbles might be obserbed merely from an opening, strain, or surface absorption. Accordingly, this method requires some experience.	
A-7	Shock test	① Checks that devices can endure intense shock during transportation or actual use. ② A shock tester is used, whereby a prescribed half-sine wave acceleration can be applied. Normally, the prescribed acceleration can be obtained by raising a carriage (a device is fixed thereto) to a certain height, and then dropping it. ③ Selects among 100, 500, 1000, and 1500G. 3 shocks are applied per one direction to a device in the prescribed direction.	The acceleration should be selected by taking device materials and shapes into account. (Particular attention should be paid to ceramic packages).	ⓐ A-7 ⓑ Ea ⓒ 2016.2 ⓓ 2002

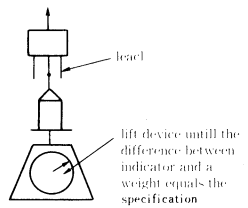
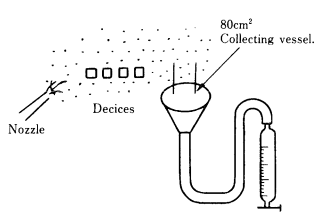
(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B
ⓓ Indicates the testing method number of MIL-STD-883C.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
	Natural drop test	① Checks that a device is durable against irregular shocks that might occur in normal handling. ② A flat maple board or equivalent (such as from a cherry) of 3cm or more thickness and 15 x 15 cm or more in size. ③ Drop a device naturally from a hight of 75 cm onto the maple board.	Care should be taken as to the drop direction according to the materials and shapes of devices. For example, when a large device is dropped leads first, the stem glass may sometimes break. This test is not applied for ceramic package.	ⓐ A-8 ⓑ Ed
A-9	Constant acceleration test	① Tests device durability against acceleration. ② A centrifugal accelerator. ③ Either 5000, 10000, or 20000G is applied in each X, Y, Z direction for one minute. ④ Electrical characteristics.	Tests mechanical durability of internal structures. Use a proper jig in which a package can be tightly fixed to the jig so that package deformity or destruction does not occur. Wire breaks are the main problem.	ⓐ A-9 ⓑ Ga ⓒ 2006 ⓓ 2001
A-10	Vibration test	① Tests how a device is influenced by vibration occurring during transportation and use. ② A vibration tester that can vary frequency. Wave shape: Sine wave ③ Fixes a package tightly to the vibrator using a jig. Vibration is applied to XYZ directions with equal testing times. 5 types of testing conditions are available. Two examples that are mainly used are shown below. Condition E: Freq. 60±20 Hz, Acceleration 20G, 96 Hr Condition D: Freq. 10-2000 Hz, 4 min./∞, 20G, 48 Hr ④ Electrical characteristics.	Since the size of semiconductor parts is small, the resonance frequency is high. Accordingly, condition D is more effective than condition E.	ⓐ A-10 ⓑ Fc ⓒ 2046.1 ⓓ 2005
A-11	Lead toughness test I (tensile test)	① Tests if a device is sufficiently durable against stress during attachment, wiring, or use. ② A tester, whereby a lead is pulled and the load can be measured. ③ Prescribed load is applied in the lead direction for 10±1 sec. Nominal cross-section area (mm^2) / Weight (kg) $0.05 < A \leqq 0.07$ — 0.25 $0.07 < A \leqq 0.2$ — 0.5 $0.2 < A \leqq 0.5$ — 1.0	Load should be applied gradually. When the tester is not provided, a prescribed weight may be hung at a lead. Another method can be employed in which a heavier weight is hung at the lead, and the weight is then put on an weighing machine. Adjust by lifting the device so that the difference between the pointer value of the machine and the weight becomes the prescribed value.	ⓐ A-11 ⓑ Ua ⓒ 2036.3 ⓓ 2004

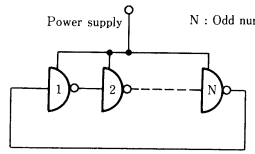
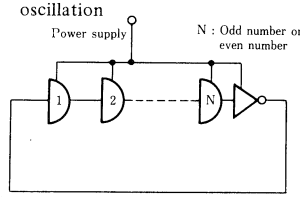
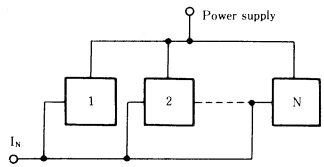
(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B
ⓓ Indicates the testing method number of MIL-STD-883C.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
		$0.5 < A \leqq 1.2$ 2.0 $1.2 < A$ 4.0	 Lifts a device so that the difference between load weight and the indicated value becomes the prescribed value.	
A-11	II	① ② Same as above. ③ A weight is hung at the tip of a lead. Next, the lead is bent 90° for within 5 sec., and then restored to its original position. Besides this test, torsion test and torque test for screw pins are available as pin toughness tests. (not described) Nominal cross-sectional area (mm^2) — Weight (kg) $0.05 < A \leqq 0.07$ 0.125 $0.07 < A \leqq 0.2$ 0.25 $0.2 < A \leqq 0.5$ 0.5 $0.5 < A \leqq 1$ 1.0 $1.2 < A$ 2.0 ④ Relative shifts between leads and main body. Damage, and loosening.		ⓐ A-11 ⓑ Ub ⓒ 2036.3 ⓓ 2004
A-12	Salt test	① Checks corrosion resistance and uniformity of a device surface. ② A temperature-controllable bath, whereby salt water is sprayed from a nozzle. ③ NaCl solution: 5% ± 1% (by weight) Temperature of salt water and bath is 35 ± 2°C. With respect to the spray amount, adjusts from 10-50 $g/m^2/d$. Unless specified, testing time is 24 ± 2 hr. Samples are washed by water at normal temperature after testing. ④ Unclear markings, peels, or pits on the surface are not acceptable. In addition, corrosion that results in a defective device is of course not acceptable.	 A bath from which no water drops form on devices should be prepared. In spite of such a bath, water drops are sometimes formed naturally, and can cause corrosion, making it difficult to judge. Accordingly, it is recommended to prepare a defective limit sample.	ⓐ A-12 ⓑ Ka ⓒ 1046.2 ⓓ 1009
A-13	Dip test	① Checks sealing effects. ② A hot water bath and a cold water bath. ③ One cycle is as follows: Dips into pure water at 65 ± 5°C for the specified time, and then dips		

(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B ⓓ Indicates the testing method number of MIL-STD-883C.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
A-13		into pure water or saturated salt water at 25 ± 10°C for the specified time. 2 cycles are carried out. The dip time is 15 min. ④ Electrical characteristics.		
A-14	Solvent durability test	① Checks marking durability against solvent used for the removal of solder flux. ② A vessel made of materials non-reactive with the solvent. ③ A sample is dipped into a solvent selected from among isopropyl alcohol, trichloro ethylene, acetate-n-butyl, acetone, and tetrachloro-carbon at 25°C for 30 ± 5 sec. ④ Visual inspection to check markings.		ⓐ A-13
B-1	High-temperature ring oscillating operation test	(a) Inverter gate circuit ring oscillation.  (b) Non-inverter gate circuit ring oscillation  Ta = Topr max. 1000 times Applicable examples: Bipolar gate circuits and MOS gate circuits.	Check operation periodically or occasionally.	ⓐ 1015
	Hith-temperature alternate operating test	 A specified pulse is applied to the input; a specified load is connected to the output terminal. Ta = Topr max. 1000 times. Applicable example: Bipolar gate circuits MOS gate circuits Flip-flop circuits Bipolar memory circuits MOS shift register circuits	Check operation periodically or occasionally.	ⓓ 1015

(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B
ⓓ Indicates the testing method number of MIL-STD-883C.

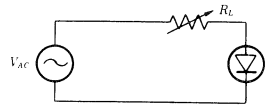
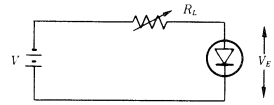
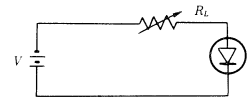
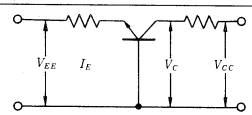
(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
B-1	High-temperature direct current operation test	1) A specified voltage is supplied to the power supply terminal, and a specified voltage is supplied to the input, making the output either H or L. Applicable example: Bipolar and gate circuits, Flip-flop circuits, MOS gate circuits, and MOS memories. 2) Supply a specified voltage to the power supply terminal. Input voltage including application sequence is supplied so that a particular bit (only one) goes into a read out state. Applicable examples: Bipolar memories 3) A specified voltage is supplied to the power supply terminal. Connects the input to ground, and the output is left open. Applicable example: Operational amplifiers and comparators.		ⓓ 1015
B-2	Intermittent operation test	① Checks durability against change in electric or thermal stress when power is periodically applied in the way of ON-OFF. ②,③,④ The same as those of B-1 except for the method in which ON-OFF is periodically applied entirely or partially to input or power supply.		ⓐ B-6 B-7
B-3	High-temperature storage test	① Checks durability when a sample is stored at a high temperature for a long period of time. ② 1000 hr. at a maximum rated storage temperature. (Tstg Max) Under 125°C $^{+5°C}_{-3°C}$ More 125°C ±5°C	Oxidation on account of surface finish should be excluded from the evaluation. Remove stains using sandpaper when necessary so as to avoid contact failure due to oxidization of the terminals.	ⓐ B-10 ⓑ B ⓒ 1031.4 ⓓ 1008
B-4	Low-temperature storage test	① Checks durability when a sample is stored at a low-temperature for a long period of time. ③ Storage temperature: Maximum rated storage Tstg	If frost or water drops are present, remove them in advance.	ⓐ B-12 ⓑ C ⓒ 1021.1
B-5	Moisture proof test	① Checks durability when a sample is used or stored in a highly humid atmosphere for a long period of time. ③ Conditions A 40 ± 2°C, 90 ± 5%RH B 60 ± 2°C, 90 ± 5%RH C 85 ± 2°C, 85 ± 5%RH	Deionized water is used. pH = 6.0-7 2 Temp.: 23°C Specific resistance: 50kohm·cm Care should be taken so that no water drops form on the device. In particular, apply bias after the inside of the bath becomes stable, and also after formed drops completely disappear.	ⓐ B-11 ⓑ A

(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B
ⓓ Indicates the testing method number of MIL-STD-883C.

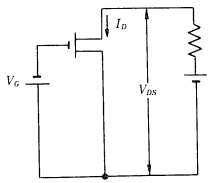
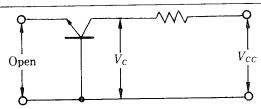
(to be continued)

Table 3-3 Summary of weather resistance testing method for transistors (JIS C 7021 except overlap of JIS C 7022)

	Testing item	Summary	Notes on testing	Related standard (Note)
B-1	Small-signal diode continuous operation test	 V_{AC} max = V_R max (50 or 60Hz) ±10% $R_L = V_{AC}(peak)/I_F$ (peak) Ta = 25 ± 5°C, 1000 hr		Ⓒ 1038
B-2	Zener diode, continuous operation test	 In the above circuit, an electric power of Pc max ± 5% is supplied. Ta = 25 ± 5°C 1000 hr	R_L should be such set so that the voltage drop at R_L is larger than V_Z.	Ⓒ 1038
B-3	Voltage variable capacitance diode, High-temp reverse bias test	 $V < V_R$ max. ±5% of the specific value Ta = Tj max 1000 hr	Monitoring method is recommended.	Ⓒ 1038
B-4	Transistor continuous operation test	 V_C = 0.4 to 0.6 x V_{CEO} max I_E is determined so that Pc = Pc max or Tj = Tj max. Both Vc and I_E should be within ±5% of the specified values. Ta = 25°C, 1000 hr	It's recommended to insert capacitances of 0.01 μF into E-B, C-B, and C-E to avoid oscillation.	Ⓒ 1039

(Note) Ⓒ Indicates the testing method number of MIL-STD-750B.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
B-5	Field effect transistor continuous operation test	 V_{DS} = 0.4 to 0.6 x V_{DS} max. I_D is determined so that P_T = P_T max. Both V_{DS} and I_D should be within ±5% of the specified value. Ta = 25°C, 1000 hr	If the gate turns on, in some cases, a large current may flow, destroying the device	Ⓒ 1036
B-6	Transistor intermittent operation test	Checks electrical-mechanical durability of a transistor against temperature change caused by ON-OFF.	Pay attention that no abnormal surge voltage is applied during the ON-OFF period.	Ⓒ 1036
B-7	Transistor intermittent operation test	The ON-OFF period is specified by the individual standards. Other conditions are the same as those of transistors and FET continuous operation test.		
B-8	Transistor high-temperature reverse bias test	 V_C = 0.7 to 0.8 x V_{CBO} max. V_C should be within ±5% of the specified value. Ta < Tj max, 1000 hr	When generated heat due to leak current is not negligible, decrease Ta or Vc so that Tj < Tj max.	Ⓒ 1036

(Note) Ⓒ Indicates the testing method number of MIL-STD-750B.

3.2 ACCELERATED LIFE TEST METHOD

The reliability of semiconductor devices are markedly influenced by the operational environment (e.g. junction temperature, temperature, humidity, voltage, and current conditions). Accordingly, the accelerated life test method has been normally employed as a means for estimating failure rate on the market.

The method of the accelerated life test is as follows:

Selecting a particular stress (e.g., voltage or junction stress) from actual stresses, a failure is investigated using the stress condition as a parameter, making it possible to estimate the failure ratio for actual operational conditions. This method is commonly used when new processes or devices are developed. In this section, the basic ideas of the accelerated life test are described.

3.2.1 Basic idea of the accelerated life test

When the accelerated test keeps a close relationship with failure physics, the test become effective. In other words, the test has been validated based on reaction kinetics; device failures occur as a result of physical-chemical reactions (crack generation, diffusion, or corrosion), and the reaction rate is determined by the stress factors.

An Arrhenius model, which is the most popular accelerated life model for semiconductor devices, and the Iring model, which is a modified model of the Arrhenius model, are described as follows:

(1) Arrhenius model

This model is commonly used when the accelerated test based on absolute temperature is carried out.

$$\ln L = A + E/R \cdot T$$

Where L is life time, A is a constant, E is activated energy [eV], T is absolute temperature [°K], and R is a gas constant.

Lifetimes L1 and L2 at temperatures of T1 and T2 can be represented as follows:

$$\log(L_1/L_2) = 5.009\,(1000/T_1 - 1000/T_2) \cdot E$$

The active energy of reaction, which is a scale of acceleration, can be determined using this formula. A conceptual figure of this model is shown in Fig. 3-4.

(2) Iring model

This model is commonly used when an acceleration based on stress is carried out, and is expressed as follows:

$$\ell n L = A - \alpha \ell n S$$

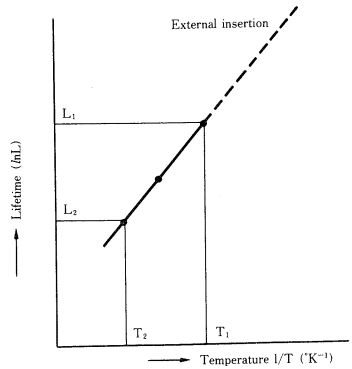


Fig. 3-1 A conceptual figure of Arrhenius model

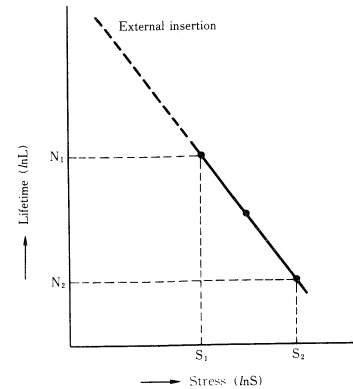


Fig. 3-2 A conceptual figure of Iring model

where L is lifetime, A and α are constants, and S is stress. In the case of material fatigue, alternating stress, and the number of repeated lifetimes N are employed. The relationship between repeated lifetimes N1 and N2 at the alternation stresses S1 and S2 is given by:

$$\ell n(N_1/N_2) = \alpha \ell n(S_1/S_2)$$

α, which represents the acceleration of this reaction, can be obtained using this formula. The conceptual drawing of this model is shown in Fig. 3-2. In JIS Z8115 (reliability terminology), the above acceleration life test is defined as "a test which is carried out in severer conditions than standard, and the object is to shorten testing time," and further defined as "failure mode and the cause should not be varied by acceleration so that the evaluation is valid."

Accordingly, the selection of acceleration factors and condition settings are key points.

When the accelerated life test is carried out, stress factors and conditions should be determined by assuming device manufacturing processes and the corresponding failure mechanism. Accordingly, the failure mechanism should be studied in advance through failure analysis of corresponding or similar devices. The accelerated life test can be classified according to stress application as shown in Table 3-4. The constant stress method is a technique in which the distribution of failure times is checked. On the other hand, the step stress method checks for the stress step where failure occurs by increasing stress step by step at constant time intervals (t_s).

Table 3-4 Classification of typical accelerated lifetime tests

Stress application method	Characteristics	Examples of accelerated test	Acceleration factor	Major failure mode
Constant stress application	Checks influence of stress on semiconductor device	High-temperature shelf test (Low-temperature shelf test)	Temperature	Surface degradation
		Operational lifetime	Junction temperature, Voltage	
		High-temperature high-humidity shelf test	Temperature, Humidity	Voltage durability degradation, Corrosion
		High-temperature high-humidity shelf test bias	Temperature, Humidity, Voltage	Corrosion, Inter-pin bridge
Cyclic stress application	Checks influence of repeated stress on semiconductor devices	Temperature cycle (Heat shock)	Temperature difference, duty	Wire break, short-circuit
		Power cycle	Temperature difference, duty	Wire break, Heat resistance degradation
		Temperature Humidity cycle	Temperature difference, Humidity difference	Wire break, short-circuit, Corrosion
Step stress application	Checks endurance limit of semiconductor device against stress	Operational lifetime	Junction temperature, Voltage	Device degradation
		High-temperature reverse bias	Junction temperature, Voltage	Device degradation
		Surge breakdown	Electricity amount, Voltage	Electrostatic breakdown, Device degradation
		Soldering heat resistance	Temperature, Time	Pellet cracks, Device degradation

3.3 RELIABILITY DATA FOR SEMICONDUCTOR DEVICES

Reliability data for Hitachi communication devices is described. Although current data is used, additional new data may be added because semiconductor devices are being developed in an innovative background. Since some devices are not mentioned in this section, refer to Hitachi's reliability data sheet for individual devices.

3.3.1 Reliability data for CODEC LSIs

Reliability test data for CODEC LSIs according to the reliability test methods described in the previous section are shown in this section. The results of high-temperature operation tests and high-temperature shelf tests are shown in Tables 3-5 and 3-6, and Table 3-7.

Thermal and mechanical environmental test results are shown in Table 3-8. Time-dependent fluctuation data of electrical characteristic parameters for CODEC LSIs obtained by high temperature operation tests are shown in Table 3-9.

Table 3-5 Reliability test result for CODEC LSI (1)

Testing item: High-temperature operation
Test condition: Ta = 125°C, V_{DD} = 5.5V, V_{SS} = −5.5V

Product name	Number of samples (pcs)	Total test time (hrs)	Number of defects	Failure rate* (1/hr)	Note
HD44231	294	3.60×10^4	0	2.5×10^{-5}	
HD44234	180	1.80×10^5	0	5.1×10^{-6}	
Total	474	2.16×10^5	0	4.3×10^{-6}	

* Confidence level: 60%

Table 3-6 Reliability test result for CODEC LSI (2)

Testing item: High-temperature operation
Test condition: Ta = 150°C V_{DD} = 5 5V, V_{SS} = −5.5V

Product name	Number of samples (pcs)	Total test time (hrs)	Number of defects	Failure rate* (1/hr)	Note
HD44231	503	5.30×10^5	2	5.8×10^{-6}	Oxidized film degradation
HD44232	48	8.40×10^4	0	1.1×10^{-5}	
HD44233	88	1.20×10^5	0	7.7×10^{-6}	
HD44234	268	1.50×10^5	0	6.1×10^{-6}	
HD44235	23	4.60×10^4	0	2.0×10^{-5}	
HD44236	24	4.80×10^4	0	1.9×10^{-5}	
HD44237	24	4.80×10^4	0	1.9×10^{-5}	
HD44238	109	2.20×10^5	0	4.2×10^{-6}	
Total	1087	1.25×10^6	2	2.5×10^{-6}	

* Confidence level: 60%

Table 3-7 Reliability test result for CODEC LSI (3)

Testing item: High-temperature operation
Test condition: Ta = 295°C

Product name	Number of samples (pcs)	Total test time (hrs)	Number of defects	Failure rate* (1/hr)	Note
HD44231	40	40000	0	2.3×10^{-5}	
HD44233	15	15000	0	6.1×10^{-5}	
HD44234	15	15000	0	6.1×10^{-5}	
HD44238	19	19000	0	4.8×10^{-5}	
Total	89	–	0	1.0×10^{-5}	

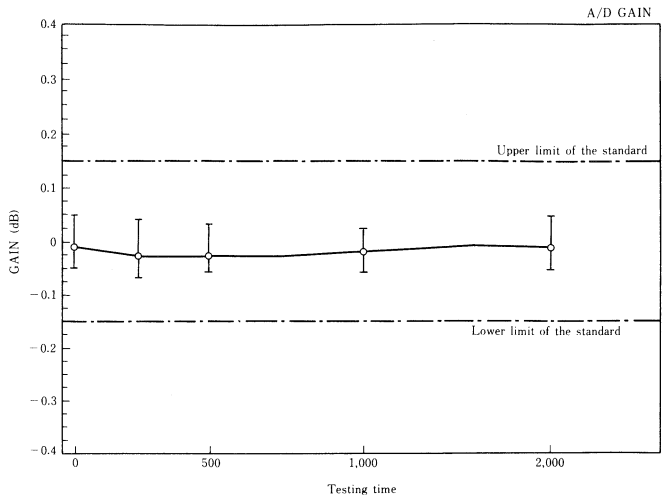
* Confidence level: 60%

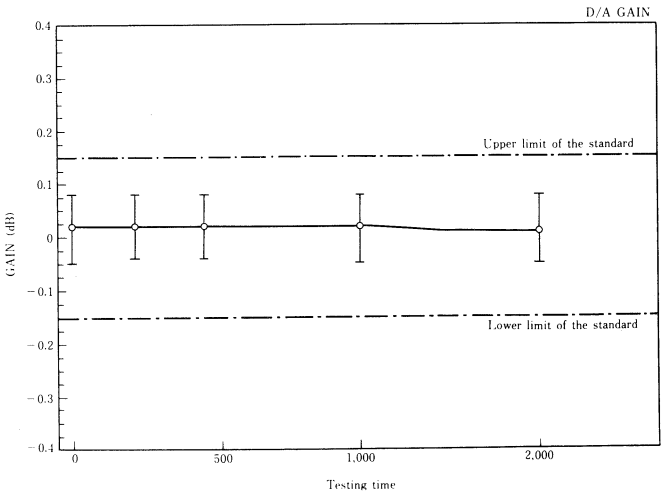
Table 3-8 Reliability test result for CODEC LSI (4)

Testing items	Test condition	Product name	Testing times	Number of samples	Number of defects
Temperature cycle (1)	−55°C to 150°C	HD44231	10 cycle	275	0
		HD44232		25	0
		HD44233		25	0
		HD44234		71	0
Temperature cycle (2)	−55°C to 150°C	HD44231	500 cycle	87	0
		HD44234		240	0
Heat shock	−65°C to 150°C	HD44231	30 cycle	30	0
		HD44234	15 cycle	15	0
Soldering heat resistance	260°C 10 sec	HD44231	–	13	0
		HD44234		44	0
Shock	1500G, 0.5msec, in each of X, Y and Z planes 3 times	HD44231		20	0
		HD44234		44	0
Variable frequency vibration	20 to 2000Hz, 20G, in each of X, Y and Z planes, 4 times	HD44231	–	20	0
		HD44234		44	0
Constant acceleration	20000G, in each of X, Y and Z planes, 1 minute	HD44231	–	20	0
		HD44234		44	0

Table 3-9 Fluctuation in characteristic for CODEC LSI

Fluctuation in characteristics		Time-dependent fluctuation in A/D and D/A gains according to lifetime testing for CODEC LSIs
Product name	HD44234B	
Testing condition	Ta = 150°C V_{DD} = +5.5V V_{SS} = −5.5V	
Number of samples	30 pieces	
Failure checking standard	A/D side Gain ±0.15dB D/A side Gain ±0.15dB	
Failure factor	V_{TH} shift due to such as surface degradation or contamination of gate oxidized films	





3.3.2 Reliability data for microcomputer LSIs

Reliability test data according to the reliability test methods described in the previous section are given in this section. Test data of 4-bit PMOS, 4-bit CMOS, 8-bit, and 16-bit NMOS LSIs are shown in Tables 3-10, 3-11, and 3-12.

(1) The distribution and fluctuation of both the A/D and D/A gains are within the standard with sufficient margin. No test results exceed the failure evaluation criterion.

Table 3-10 Reliability test results for microcomputer LSIs (1)

Test items	Test condition	4-bit microcomputer LSI Si-gate P channel plastic seal				4-bit microcomputer LSI Si-gate CMOS plastic seal			
		Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate
High-temperature operation lifetest	Ta = 125°C V_{DD} max	546	C.H. 5.6×10^5	1	3.6×10^{-6}	80	C.H. 0.8×10^5	0	1.2×10^{-5}
High-temperature shelf test	Ta = 150°C	43	0.2×10^5	0	–	53	0.2×10^5	0	–
Low-temperature shelf test	Ta = −55°C	90	0.4×10^5	0	–	–	–	–	–
High-temperature high-humidity lifetest	Ta = 65°C RH = 95%	1418	1.0×10^6	0	0.9×10^{-6}	80	0.6×10^5	0	–
	Ta = 85°C RH = 85% Bias application	45	0.2×10^5	0	–	–	–	–	–

* Confidence level: 60%

Table 3-11 Reliability test results for microcomputer LSIs (1)

Test item	Test condition	8-bit microcomputer LSI Si-gate N-channel ceramic seal				8-bit microcomputer LSI Si-gate CMOS plastic seal				16-bit microcomputer LSI Si-gate N-channel ceramic seal			
		Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate
High-temperature operation lifetest	Ta=125°C V_{DD} max	Pieces 1027	C.H. 9.4×10^5	1	2.1×10^{-6}	Pieces 331	C.H. 3.31×10^5	0	2.8×10^{-6}	Pieces 62	C.H. 0.62×10^5	0	1.5×10^{-5}
High-temperature shelf test	Ta=150°C	343	3.1×10^5	0	3.0×10^{-6}	–	–	–	–	42	0.42×10^5	0	–
Low-temperature shelf test	Ta=−55°C	66	0.7×10^5	0	–	–	–	–	–	42	0.42×10^5	0	–
High-temperature high-humidity lifetest	Ta=65°C RH=95%	90	0.9×10^5	0	–	176	1.39×10^5	0	6.6×10^{-6}	42	0.42×10^5	0	–
	Ta=85°C RH=85% Bias application	90 90	0.9×10^5 0.9	0	–	875	8.75×10^5	0	1.1×10^{-6}	42	0.42×10^5	0	–

* Confidence level: 60%

Table 3-12 Reliability test results for microcomputer LSIs (2)

Test item	Test condition	DIL plastic seal		FPP plastic seal		Ceramic seal (8-bit microcomputer LSI)		Ceramic seal (16-bit microcomputer LSI)	
		Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects
Heat shock	0°C to 100°C 10 cycles	150	0	100	0	76	0	44	0
Temperature cycle	−55°C to 150°C 10 cycles	1,637	0	1,514	0	397	0	42	0
Soldering heat resistance	260°C 10 sec.	140	0	160	0	88	0	22	0
Salt water spray	35°C NaCl 5% 24hr	20	0	20	0	22	0	22	0
Solderability	230°C 5 sec. Rosin flux	34	0	34	0	66	0	22	0
Natural drop	Used maple board 75cm, 3 times	24	0	20	0	76	0	44	0
Impact drop	1,500G, 0.5ms in each of X, Y and Z planes, 3 times	–	–	–	–	66	0	44	0
Vibration fatigue	60Hz, 20G in each of X, Y and Z planes 32hr.	120	0	20	0	66	0	44	0
Variable frequency vibration	100 to 2,000Hz, 20G, in each of X, Y and Z planes, 4 times	–	–	–	–	66	0	44	0
Constant acceleration	20,000G, in each of X, Y and Z planes, 1 minute	–	–	–	–	66	0	44	0
Pin toughness	225g, 90°C bending test, 3 times for both sides	20	0	20	0	66	0	20	0

3.3.3 Reliability data for MOS memories

3.3.3.1 Reliability data of MOS dynamic and static RAMs

Lifetime test results for 256K DRAM (HM50256), 64K DRAM (HM4864AP), 64K SRAM (HM6264P), and 16K SRAM (HM6116P) are shown in Tables 3-13 and 14. High-temperature and high-voltage lifetime tests are implemented so as to evaluate product reliability with few samples. Every failure occurring in the testing is due to faults in fabrication processes. These test results are reflected in the fabrication processes, enabling quality and reliability to be improved.

3.3.3.2 Reliability data for EPROMs

There are two types of EPROMs: one is the conventional type (a package with a window) in which written data is erasable by irradiating ultra-violet rays, and the other is the one-time writing type (OTP: one time EPROM). The latter is sealed into a plastic package.
Lifetime test results for 64K EPROMs (HN482764, HN482764P) and a 128K EPROM (HN4827128) are shown in Table 3-15.

The cause of the defects shown in Table 3-15 is data dissipation caused by a phenomenon in which charges (electrons) stored in memory cells escape from the floating gates out of a device by obtaining thermal energy. In this data dissipation phenomenon, although quite evident temperature dependency (activated energy: approximately 1.0 eV) is observed, no problems arise in actual use. The moisture resistance of plastic-sealed OTPs is quite favourable.

3.3.3.3 Reliability data for mask ROMs

Unlike EPROM/EEPROMs, since patterning is performed on mask ROMs in the manufacturing process according to the ROM data, no data dissipation occurs. The lifetime test results for 256K and 1M-bit mask ROMs are shown in Table 3-16.

3.3.3.4 Reliability data for MOS memories (environmental test results)

An example of environmental test results is shown in Table 3-17. Desirable results can be obtained without causing a failure even under severe environmental conditions.

Table 3-13 Reliability result for 256K DRAM, 64K DRAM

Test item	Test condition	HM50256 (CERDIP)				HM4864AP (PLASTIC)				Notes
		Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	
High-temperature pulse operation	150°C/8V	525	1.02×10^{6}	10*1	1.13×10^{-5}	500	1.0×10^{6}	1*4	2.02×10^{-6}	* 1 ~ 3 Oxidized film defect x 17 Foreign material x 1 *4 Oxidized film defect x 1
	150°C/7V	448	0.81×10^{6}	4*2	6.47×10^{-6}	69	0.35×10^{6}	0	2.63×10^{-6}	
	125°C/8V	336	0.67×10^{6}	4*3	7.82×10^{-6}	300	0.60×10^{6}	0	1.53×10^{-6}	
	125°C/7V	2834	0.95×10^{6}	0	9.68×10^{-7}	429	1.04×10^{6}	0	8.85×10^{-7}	
High-temperature high-humidity bias	85°C 85%RH 5.5V	160	0.36×10^{6}	0	2.56×10^{-6}	650	1.23×10^{6}	0	7.48×10^{-7}	
Pressure cooker	121°C/100%RH	–	–	–	–	100	5×10^{4}	0	1.84×10^{-5}	

* Confidence level: 60%

Table 3-14 Reliability test results for 64K SRAM, 16K SRAM

Test item	Test condition	HM6264P (PLASTIC)				HM6116P (PLASTIC)				Notes
		Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	
High-temperature pulse operation	150°C/7V	100	0.1×10^{6}	1*1	2.02×10^{-5}	–	–	–	–	*1 ~ 3 Foreign material x 2 PSG defect x 1 Crystalline defect x 1 Uncertain x 1 *4 Bit defect (Uncertain x 2
	125°C/8V	162	0.20×10^{6}	2*2	1.55×10^{-5}	–	–	–	–	
	125°C/7V	1014	1.16×10^{6}	2*3	2.67×10^{-5}	–	–	–	–	
	125°C/5.5V	–	–	–	–	9940	2.28×10^{6}	2*4	1.36×10^{-6}	
High-temperature high-humidity bias	85°C/85%RH 7V	304	0.30×10^{6}	0	3.07×10^{-6}	1430	2.35×10^{6}	4*5	2.23×10^{-6}	*5 Al corrosion x 2 Passivation defect x 2
Pressure cooker	121°C/100%RH	55	2.2×10^{4}	0	4.18×10^{-5}	250	4.4×10^{4}	0	2.09×10^{-5}	

* Confidence level: 60%

Table 3-15 Reliability test results for 64K EPROM, 128K EPROM

Test item	Test condition	HN482764 (CERDIP/PLASTIC)				HN4827128 (CERDIP)				Notes
		Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	
High-temperature pulse operation	125°C/5.5V	131	0.43×10^{6}	0	2.14×10^{-6}	100	0.1×10^{6}	0	9.2×10^{-6}	*1 Data dissipation
	125°C/7V	760	0.61×10^{6}	0	1.51×10^{-6}	–	–	–	–	
High-temperature shelf test	200°C	117	1.17×10^{5}	1*1	1.73×10^{-5}	80	0.4×10^{5}	0	2.3×10^{-5}	
	250°C	106	1.06×10^{5}	5*1	5.94×10^{-5}	65	0.33×10^{5}	1*1	6.12×10^{-5}	
	300°C	67	0.67×10^{5}	25*1	3.73×10^{-4}	50	0.25×10^{5}	6*1	2.93×10^{-4}	
High-temperature high-humidity bias	85°C/85%RH 5V	200	0.2×10^{6}	0	4.60×10^{-6}	–	–	–	–	OTPdata of 64K EPROM
Pressure cooker	121°C/100%RH	78	0.16×10^{5}	0	5.75×10^{-5}	–	–	–	–	

* Confidence level: 60%

Table 3-16 Reliability test result for 256K MASKROM, IM MASKROM

Test item	Test condition	HN613256P (PLASTIC)				HN62301P (PLASTIC)				Notes
		Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	
High-temperature pulse operation	125°C/5.5V	90	0.9×10^{5}	0	1.02×10^{-5}	–	–	–	–	
	125°C/7V	50	0.5×10^{5}	0	1.84×10^{-5}	246	2.46×10^{5}	0	3.74×10^{-6}	
High-temperature high-humidity bias	85°C/85%RH V_{CC} = 5.5V	120	1.2×10^{5}	0	7.67×10^{-6}	120	1.2×10^{5}	0	7.67×10^{-6}	
Pressure cooker	121°C/100%RH	80	0.8×10^{4}	0	1.15×10^{-4}	78	1.56×10^{4}	0	5.90×10^{-5}	

* Confidence level: 60%

Table 17 Reliability test result for MOS MEMORY

Testing item	Test condition	HM50256 (CERDIP)		EPROM (CERDIP)		HM4864AP (PLASTIC)		HM6264P (PLASTIC		LCC		Notes
		No. of samples	No. of defects	No. of samples	No. of defects	No. of samples	No. of defects	No. of samples	No. of defects	No. of samples	No. of defects	
Temperature cycle	−55°C to 150°C 10 cycles	1486	0	775	0	887	0	3315	0	860	0	
Temperature cycle	−55°C to 150°C 1000 cycles	316	0	250	0	277	0	150	0	445	0	
Heat shock	−65°C to 150°C 15 cycles	145	0	146	0	38	0	76	0	498	0	
Soldering heat resistance	260°C 10 sec.	50	0	90	0	38	0	76	0	82	0	
Impact drop	1,500G, 0.5ms	38	0	90	0	–	–	–	–	82	0	
Variable frequency vibration	20 to 2,000Hz 20G	38	0	90	0	–	–	–	–	82	0	
Centrifugal acceleration	20,000G	38	0	90	0*	–	–	–	–	82	0	*6,000G

3.3.4 Reliability data for linear ICs

Reliability test data of an linear IC obtained according to the test method for semiconductor devices described in the previous section is shown in Table 3-18. As an example of characteristics fluctuation, input offset of an operation amplifier is shown in Table 3-19.

3.3.5 Reliability data for bipolar digital ICs

Test results according to the reliability evaluation test for semiconductor devices described in the previous section are described in this section. As an example of reliability test results for TTLs, a summary of standard TTL HD74 series is described in Tables 3-20 and 21. They are classified into plastic seal type and air-tight seal type. For more details on HD74 series products and reliability test results of other series products, refer to the reliability data book.

Table 3-18 Reliability test result for Linear IC

Test items	Test condition	Plastic seal				Airtigh seal (Glass seal)			
		Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	Number of samples	Total test time	Number of defects	Failure rate (1/hr)*
High-temperature operation	Ta = 125°C V_{CC} = V_{CC} max. (V_{CC} = V_{EE} max)	1,660	1,190,000	5	5.3×10^{-6}	2,345	2,424,600	0	3.8×10^{-7}
High-temperature shelf test Low-temperature shelf test	Ta = 150°C Ta = −55°C Ta = −65°C	829 509 –	793,000 509,000 –	0 0 –	1.2×10^{-6} 1.8×10^{-6} –	485 – 376	463,700 – 376,000	0 – 0	2.0×10^{-6} – 2.4×10^{-6}
High-temperature high-humidity shelf test	Ta=65°C, 95%RH Ta=85°C, 85%RH	3,110	2,727,000	0	3.4×10^{-7}	–	–	–	–
High-temperature high-humidity operation	V_{CC}=V_{CC} max.	443	443,000	0	2.0×10^{-6}	–	–	–	–
Temperature cycle	−55°C to +150°C 10 cycles	10,043	–	0	–	2,198	–	0	–
Temperature cycle life-time	−55°C to +150°C 200 cycles	4,280	–	0	–	900	–	0	–
Heat shock	0°C to 100°C 10 cycles	398	–	0	–	311	–	0	–
Soldering heat resistance	260°C, 10 sec	404	–	0	–	305	–	0	–
Impact drop	1500G, 0.5ms., in each of X, Y and Z directions, 3 times	160	–	0	–	260	–	0	–
Vibration fatigue	60Hz, 20G, in each of X, Y and Z directions 32hrs.	160	–	0	–	260	–	0	–
Variable frequency vibration	100 to 2,000Hz, 20G, in each of X, Y and Z directions, 3 times	160	–	0	–	260	–	0	–
Constant acceleration	20,000G, in each of X, Y and Z directions, 1 minute	160	–	0	–	260	–	0	–
PCT	Ta = 121°C, 2 atmospheric pressure, 60hrs	360	–	0	–	–	–	–	–
Solderability	230°C, 5 sec Rodin flux	160	–	0	–	300	–	0	–
Pin toughness	225g, 90° bending test, 3 times for both sides	90	–	0	–	45	–	0	–

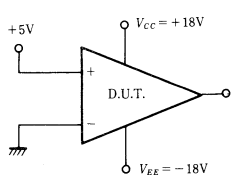
* Reliability level 60%

Table 3-19 Fluctuation in characteristics of Op-Amp. ICs

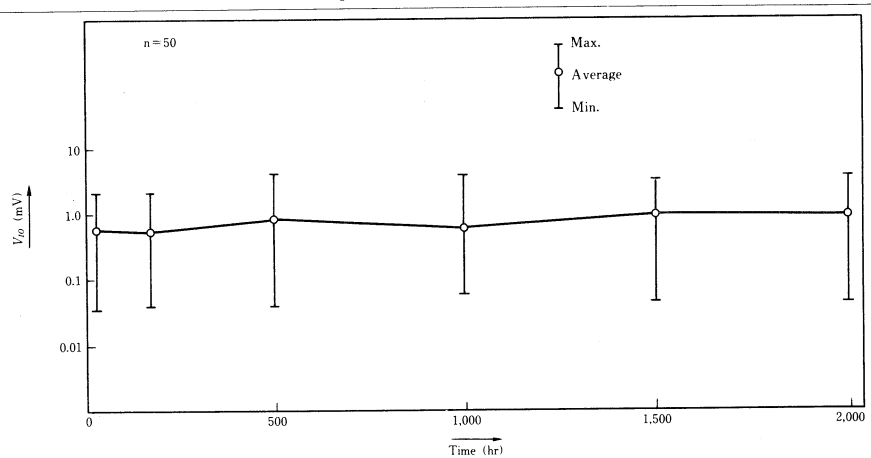
Fluctuation in characteristics	
Product	HA17747P (Plastic seal)
Testing condition	Ta = 125°C, $V_{CC} = -V_{EE}$ = 18V continuous operation
Failure checking standard	V_{IO} = 9mV (Rs ≦ 10kΩ) V_{IO} = 300nA
Failure mechanism	Surface degradation, V_{BE} balance

Results:
1) Both V_{IO} and I_{IO} vary stably.
2) Both V_{IO} and I_{IO} are within the initial standard; neither exceeds the failure checking standard.

Note: Circuit diagram of operation test



Fluctuation in input offset voltage and current of Op-Amp. ICs.



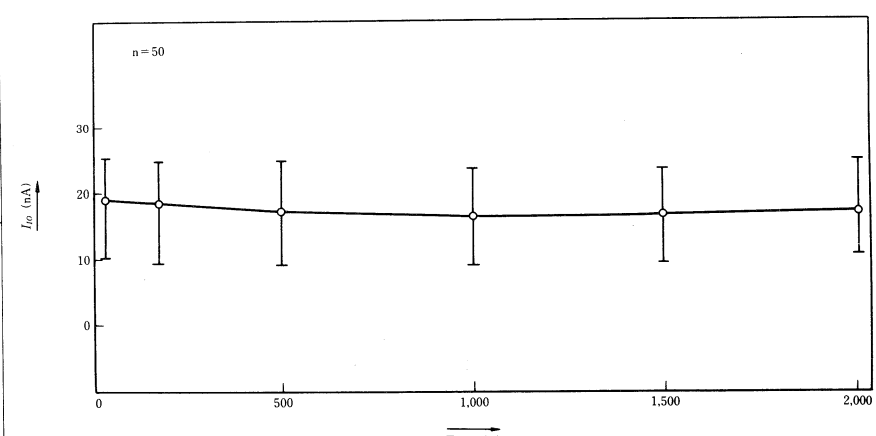


Table 3-20 Reliability test result for HD74 SERIES (1)

Test items	Test condition	Plastic seal				Ceramic seal			
		Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	Number of samples	Total test time	Number of defects	Failure rate (1/hr)*
High-temperature operation lifetime	Ta = 125°C V_{CC} = 5.5V	7,852	C.H. 7.3×10^6	2**	4.3×10^{-7}	3,390	C.H. 3.7×10^6	0	2.5×10^{-7}
	Ta = 150°C V_{CC} = 5.5V	–	–	–	–	3,771	3.3×10^6	0	2.8×10^{-7}
High-temperature shelf test lifetime	Ta = 150°C	1,488	6.4×10^6	0	1.4×10^{-7}	–	–	–	–
	Ta = 200°C	–	–	–	–	400	2.7×10^5	0	3.4×10^{-6}
Moisture-resistance lifetime	Stored at 65°C, 95%	11,312	1.1×10^7	1***	1.8×10^{-7}	600	6.0×10^5	0	1.5×10^{-6}
	Biased at 85°C, 85%	14,150	1.4×10^7	2***	2.2×10^{-7}	180	1.2×10^5	0	7.7×10^{-6}

* Reliability level 60% ** I_{IH} Large *** Al corrosion

Table 3-21 Reliability test results for HD74 SERIES (2)

Test item	Test condition	Plastic seal		Ceramic seal	
		Number of samples	Number of defects	Number of samples	Number of defects
Nutural drop	Use maple board 75cm	Piece 334	Pieces 0	Pieces 480	Pieces 0
Impact drop	1500G, 0.5ms in each of X, Y and Z planes, 3 times	311	0	540	0
Vibration fatigue	60Hz, 20G, in each of X, Y and Z planes 32hr.	90	0	547	0
Variable frequency vibration	100 to 200Hz, 20G in each of X, Y and Z planes, 4 times	90	0	409	0
Constant acceleration	20,000G in each of X, Y and Z planes once	160	0	480	0
Temperature cycle	–55°C to +150°C, 10 cycles	180,000	0	4,630	0
Heat shock	0°C to 100°C, 10 cycles	1,582	0	850	0
Soldering heat resistance	260°C, 10 sec.	653	0	835	0
Solderbility	230°C, 5 sec., Rosin flax	1,333	0	950	0
Pin toughness	225g 90° bending, 3 times	99	0	60	0
Temperature cycle lifetime	–55°C to +150°C, 500 cycles	68,000	0	4,552	0

3.3.6 Reliability data for small signal transistors

Examples of lifetime and environmental test results are shown in Tables 3-22 and 23. For individual reliability test results, refer to reliability data for each product.

Table 3-22 Reliability test result for small signal transistors (1)

Testing item	2SC1707 Ⓗ type (NPN metal seal)					2SA537 Ⓗ type (PNP metal seal)					2SA1084 type (PNP plastic seal)				
	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate
		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr
Operation life-time	P_C= 200mW V_{CB}= 40V	1,000	1.0×10^6	0	0.92×10^{-6}	P_C= 0.75W V_{CB}= −50V	1,000	1.0×10^6	0	0.92×10^{-6}	Ta=25°C P_C= 400mW V_{CB}= −72V	200	2.0×10^5	0	0.46×10^{-5}
High-temperature reverse bias	Ta= 150°C V_{CES}= 400V	300	3.0×10^5	0	3.1×10^{-6}	Ta= 150°C V_{CES}= −50V	300	3.0×10^5	0	3.1×10^{-6}	Ta= 125°C V_{CES}= −90V	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 175°C	500	5.0×10^5	0	1.8×10^{-6}	Ta= 175°C	500	5.0×10^5	0	1.8×10^{-6}	–	–	–	–	–
High-temperature shelf test	–	–	–	–	–	–	–	–	–	–	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}

Testing item	2SC2468 type (FPAK)					3SK83 type (FPAK)					2SC2462 type (MPAK)				
	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate
		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr
Operation life-time	P_C= 200mW V_{CA}= 24V	200	2.0×10^5	0	0.46×10^{-5}	P_C= 200mW V_{DS}= 15V	200	2.0×10^5	0	0.46×10^{-5}	P_C= 150mW V_{CB}= 40V	200	2.0×10^5	0	0.46×10^{-5}
High-temperature reverse bias	Ta= 125°C V_{CES}= 30V	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C V_{DS}= 15V V_{G1S}= V_{G2S}= −5V	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C V_{CES}= 50V	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}

Testing item	2SD1368 type (UPAK)					3SK136 type (MPAK-4)					2SA1374 type (SPAK)				
	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate
	**	Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr
Operation life-time	P_C=1W V_{CB}= 100V	200	2.0×10^5	0	0.46×10^{-5}	Pch= 150mW V_{DS}= 20V	200	2.0×10^5	0	0.46×10^{-5}	P_C= 300mW V_{CB}= −55V	200	2.0×10^5	0	0.46×10^{-5}
High-temperature reverse bias	Ta= 150°C V_{CES}= 50V	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C V_{DS}= 20V V_{G1S}= V_{G2S}= −5V	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C V_{CES}= −55V	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 150°C	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}

* Reliability level 60% ** Used specified heat sink

Table 3-23 Reliability test results for small signal transistors (2)

Test item	Test condition	2SC1775 (Plastic seal)		2SC2468 (FPAK)		2SC2462 (MPAK)	
		Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects
Soldering heat resistance	260°C, 10 sec. 1.3mm from root	Pieces 120	Pieces 0	Pieces 120	Pieces 0	Pieces 120	Pieces 0
Heat shock	−196°C to +150°C, 5 minutes, 100 cycles	775	0	775	0	775	0
Temperature cycle	−55°C to 25°C to 125°C 10 cycles	3,900	0	3,900	0	3,900	0
MIL humidity resistance	−10°C to +65°C, RH≧90% 10 cycles	200	0	200	0	200	0
Impact drop	1,500G, 0.5msec. in each X, Y and Z directions, 3 times	80	0	80	0	80	0
Variable frequency vibration	100 to 2,000Hz, 20G, in each of X, Y and Z planes, 4 minutes x 4 times	80	0	80	0	80	0
Vibration fatigue	60Hz, 20G in each of X, Y and Z planes 32hr.	80	0	80	0	80	0
Pin toughness (1)	450g, 90°C bending test, 3 times for both sides	80	0	–	–	–	–
	225g, 90°C bending test, once for both sides	–	–	80	0	80	0
Pin toughness (2)	450g, 10 sec.	80	0	80	0	80	0
Salt water spray	35°C, 5% salt water spraying test 48hr.	110	0	110	0	110	0

Test item	Test condition	3SK136 (MPAK-4)		2SD1368 (UPAK)		2SA1374 (SPAK)	
		Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects
Soldering heat resistance	260°C, 10 sec. 1.3mm from root	Pieces 120	Pieces 0	Pieces 120	Pieces 0	Pieces 120	Pieces 0
Heat shock	−196°C to +150°C, 5 minutes, 100 cycles	775	0	775	0	775	0
Temperature cycle	−55°C to 25°C to 125°C 10 cycles	3,900	0	3,900	0	3,900	0
MIL humidity resistance	−10°C to +65°C, RH≧90% 10 cycles	200	0	200	0	200	0
Impact drop	1,500G, 0.5msec. in each X, Y and Z directions, 3 times	80	0	80	0	80	0
Variable frequency vibration	100 to 2,000Hz, 20G, in each of X, Y and Z planes, 4 minutes x 4 times	80	0	80	0	80	0
Vibration fatigue	60Hz, 20G in each of X, Y and Z planes 32hr.	80	0	80	0	80	0
Pin toughness (1)	450g, 90°C bending test, 3 times for both sides	80	0	–	–	–	–
	225g, 90°C bending test, once for both sides	–	–	80	0	80	0
Pin toughness (2)	450g, 10 sec.	80	0	80	0	80	0
Salt water spray	35°C, 5% salt water spraying test 48hr.	110	0	110	0	110	0

Table 3-24 Fluctuation in characteristics of small signal transistors (1)

Fluctuation in characteristics (1)	
Product	2SC1707 Ⓗ
Test condition	Ta = 125°C, V_{CES} = 50V
Failure checking standard	h_{FE} fluctuation ratio ± 10%
Failure mechanism	Surface degradation

Result:
The fluctuation of h_{FE} which is highly sensitive to surface degradation of the emitter-base conjunction is evaluated. No or less fluctuation is observed as shown in the right figure.

Note
Air-tight seal

h_{FE} Fluctuation (I_C = 100μA)

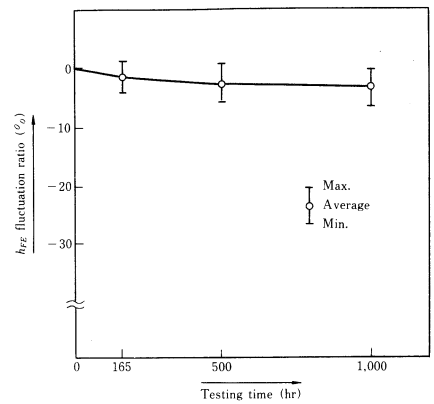


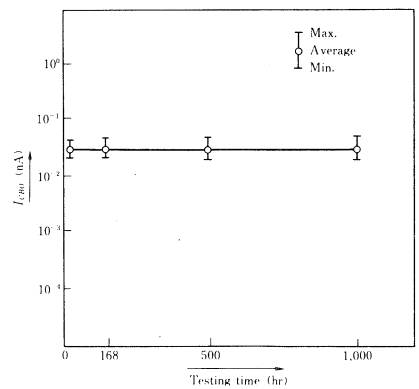
Table 3-25 Fluctuation in characteristics of small signal transistors (2)

Fluctuation in characteristics (2)	
Product	2SA1084
Test condition	High-temperature and high-humidity bias Ta=85°C RH=85% V_{CES}=−90V
Failure checking standard	I_{CBO} initial standard valuex2
Failure mechanism	Surface degradation due to water permeation

Result:
The fluctuation of I_{CBO} which is highly sensitive to surface degradation of the collector-base junction is evaluated. No device has current leakage of 0.1 nA or more even after 100 hr. of testing.

Note
Plastic seal

I_{CBO} fluctuation (V_{CB} = −60V)



3.3.7 Reliability data for power transistors

Examples of reliability test results for power transistors are shown in Tables 3-26 and 27. For individual reliability test results, refer to the reliability data for each product.
Checking characteristic fluctuation by the reliability test is very effective to grasp the reliability and quality level of products. In particular, with respect to characteristic items having no margin in circuit design, study of the characteristic fluctuation is required by taking operational conditions into account. In particular, with respect to high output device applications, this is very important since heat radiation design greatly influences the reliability. Examples of characteristic fluctuations are shown in Tables 3-28 to 30. During attachment, care should be taken that excessive force is not applied to devices. (tightening torque, foreign material between devices and heat sink plates, etc.)

Table 3-26 Reliability test result for Power transistors (1)

Test item	Test condition	2SB638Ⓗ/2SD628Ⓗ(TO-3)				2SK135(TO-3) power MOS FET				2SC3336 (TO-3P)			
		Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate
Operation lifetime	Tj=150°C	Piece 44	C.H. 4.4×10^4	Piece 0	1/hr 2.1×10^{-5}	Piece 80	C.H. 1.6×10^5	Piece 0	1/hr 5.8×10^{-6}	Piece 50	C.H. 5.0×10^4	Piece 0	1/hr 1.8×10^{-5}
High-temperature contrary bias	Ta=150°C $V_{CB}=V_{CB}$ max	50 V_{CB}=100V	5.0×10^4	0	1.8×10^{-5}	125 V_{DS}=160V V_{GS}=−10V	2.5×10^3	0	3.7×10^{-6}	50 V_{CB}=500V	5.0×10^4	0	1.8×10^{-5}
High-temperature shelf test	Ta=150°C	50	5.0×10^4	0	1.8×10^{-5}	80	1.6×10^5	0	5.8×10^{-6}	50	5.0×10^4	0	1.8×10^{-5}
High-temperature high-humidity shelf test	Ta=65°C RH≧95%	–	–	–	–	–	–	–	–	50	5.0×10^4	0	1.8×10^{-5}
Power cycle	ΔTc=90°C	50	Cycle 5.0×10^5	0	1.8×10^{-6} /cycle	50	Cycle 5.0×10^5	0	1.8×10^{-6} /cycle	50	Cycle 5.0×10^5	0	1.8×10^{-6} /cycle

Test item	Test condition	2SD768Ⓚ(TO-220)				2SC1514(TO-202)				2SD1081(DPAK)			
		Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate
Operation lifetime	with heat sink Tj=150°C	Piece 40	C.H. 4.0×10^4	Piece 0	1/hr 2.3×10^{-5}	–		–	–	–	–	–	–
	Free air Tj=150°C	40	4.0×10^4	0	2.3×10^{-5}	Piece 150	C.H. 1.5×10^5	Piece 0	1/hr 6.1×10^{-6}	Piece 150	C.H. 1.5×10^5	Piece 0	1/hr 6.1×10^{-6}
High-temperature contrary bias	Ta=150°C $V_{CB}=V_{CB}$ max	60 V_{CB}=120V	6.0×10^4	0	1.5×10^{-5}	120 V_{CB}=300V	1.2×10^5	0	7.6×10^{-6}	120 V_{CB}=180V	1.2×10^5	0	7.6×10^{-6}
High-temperature shelf test	Ta=150°C	76	7.6×10^4	0	1.2×10^{-5}	120	1.2×10^5	0	7.6×10^{-6}	120	1.2×10^5	0	7.6×10^{-6}
High-temperature high-humidity lifetime	Ta=65°C RH≧95%	40	4.0×10^4	0	2.3×10^{-6}	120	1.2×10^5	0	7.6×10^{-6}	120	1.2×10^5	0	7.6×10^{-6}
Power cycle	ΔTc=90°C	80	Cycle 8.0×10^5	0	1.2×10^{-6} /cycle	80	Cycle 8.0×10^5	0	1.2×10^{-6} /cycle	80	Cycle 8.0×10^5	0	1.2×10^{-6} /cycle

* Reliability level. 60%

Table 3-27 Reliability test result for power transistors (2)

Test item	Test condition	2SD628 Ⓗ (TO-3)		2SC3336 (TO-3P)		2SD768 Ⓚ		2SC1514 (TO-202)		2SD1081 (DPAK)	
		Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects
Soldering heat resistance	260°C 1.6mm 10 sec.	Pieces 22	Pieces 0	Pieces 22	Pieces 0	Pieces 20	Pieces 0	Pieces 75	Pieces 0	Pieces 22	Pieces 0
Heat shock	0 to 100°C 5 cycles	44	0	44	0	75	0	75	0	75	0
Temperature cycle	−45 to +150°C 10 cycles	510	0	1,152	0	800	0	76	0	1,152	0
Shock	1500G, 0.5msec 3 directions 3 times each	44	0	44	0	45	0	67	0	45	0
Natural drop	Used maple board 75cm×3times	400	0	1,152	0	800	0	350	0	800	0
Vibration fatigue	60Hz, 20G 3 direction, 96hr	22	0	45	0	45	0	67	0	45	0
Pin toughness	Stretch test 24hr	22	0	22	0	20	0	67	0	22	0
Salt water spray	5% saltwater spraying test 24Hr	22	0	22	0	20	0	–	–	22	0

Table 3-28 Fluctuation in characteristic of Power Transistors

Fluctuation in characteristics (1)	
Product	2SD628Ⓗ
Test condition	$\Delta Tj = 105°C$*
Failure checking standard	ΔV_{BE} initial standard value x 1.2
Failure mechanism	Material fatigue

Result:
The fluctuation of V_{BE} having an evident correlation with θ_{jc} through the power cycle is plotted in the right figure. No or less fluctuation is observed at a range up to 30,000 cycles.

Note
*ΔTj: Temperature differences in functions

Fluctuation in ΔV_{BE} through the power cycle

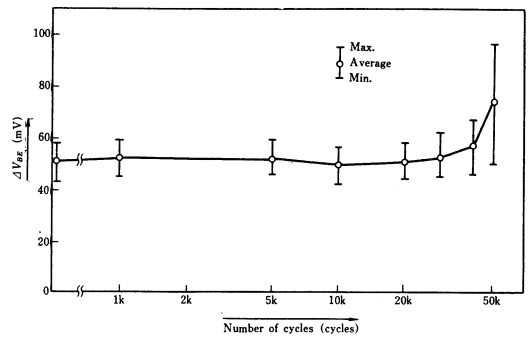


Table 3-29 Fluctuation characteristic of in Power-MOS FET

Fluctuation in characteristics (2)	
Product	2SK135
Test condition	Ta = 150°C V_{DS} = 160V, V_{GS} = −10V
Failure checking standard	V_{DSX} initial standard value × 0.8 $V_{DS(sat)}$ initial standard value × 1.2
Failure mechanism	Surface degradation
Result: 1. No or less fluctuation in voltage durability is observed even after 2,000 hr. 2. With respect to the saturation voltage change, a slight increase is observed at the initial stage; however, all are completely saturated after 2,000 hr.	
Note:	

Fluctuation in voltage durability and saturation voltage under high-temperature reverse bias conditions

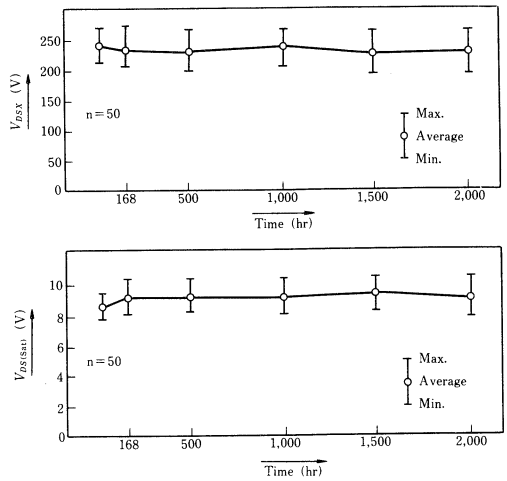
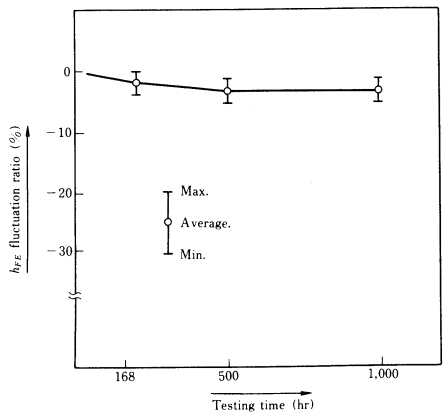


Table 3-30 Fluctuation in TO-3P transistors

Fluctuation in characteristics (3)	
Product	2SC3336
Test condition	Ta = 150°C, V_{CES} = 500V
Failure checking standard	h_{FE} fluctuation ratio ±20%
Failure mechanism	Surface degradation
Result: The fluctuation of h_{FE} which is highly sensitive to surface degradation of the emitter-base junction is evaluated. No or less fluctuation is observed as shown in the right figure.	
Note	Plastic seal

h_{FE} fluctuation (I_C = 1.0A)



3.3.8 Reliability data for infrared LEDs

Examples of reliability data for infrared LEDs are described. Reliability test results of RG-type devices of HLP series are shown in Table 3-31.

(3) Characteristic fluctuation

Time-dependent variational data examples of light emitting power by operation lifetime tests for RG type devices in HLP series are shown in Table 3-32.

3.3.9 Reliability data for laser diodes

Examples of reliability data for laser diodes are described. Reliability test results of HL and HLP series devices are shown in Table 3-33. For individual reliability test results, refer to reliability data for each product.

Time-dependent characteristic variational data examples from operational lifetime tests for HL and HLP series are shown in Table 3-34.

Table 3-31 Reliability test results for infrared LEDs

Test item	Test condition	RG type (Air-tight sealing)		
		Number of samples (Piece)	Test time (hr)	Number of defects (Piece)
Operational lifetime	Ta = 25°C, I_F = 200mA, RG type: Free air	22	1,000	0
Intermittent operation lifetime	2 min. for ON, and 1 min. for OFF under the same conditions as the above	22	1,000	0
Temperature shelf test	Ta = 100°C	11	1,000	0
High-temperature high-humidity shelf test	Ta = 60°C, RH ≧ 90%	15	1,000	0
Low-temperature shelf test	Ta = −40°C	15	1,000	0
Temperature cycle	−40 to +100°C, 30 minutes each, 10 cycles	22	1,000	0
Vibrational fatigue	60Hz, 20G, 2 directions each 32hr.	15	–	0
Variable frequency vibration	100 to 2000Hz, 20G 4 minutes for both sides, 2 directions, 3 times each			
Impact drop	1500G, 0.5msec, 2 directions, 3 times each			
Lead bending	225g, 90° 3 times	11	–	0
Soldering heat resistance	260°C, 10sec.	11	–	0
Solderability	230°C, 5sec.	11	–	0

Table 3-32 Fluctuation in infrared LEDs

Fluctuation in characteristics	
Product	HLP30
Test condition	Ta = 25°C, IF = 200mA RG type: Free air
Failure checking standard	Initial standard value of light emitting power × 0.7
Failure mechanism	Crystalline failure

Result:
The fluctuation in outputs from forward-direction continuous operational test is shown in the right figure.
Since heat radiating conditions are different, decrease in the light emitting output of the RG package is slightly greater than others.

Fluctuation in light emitting power (I_F = 200mA)

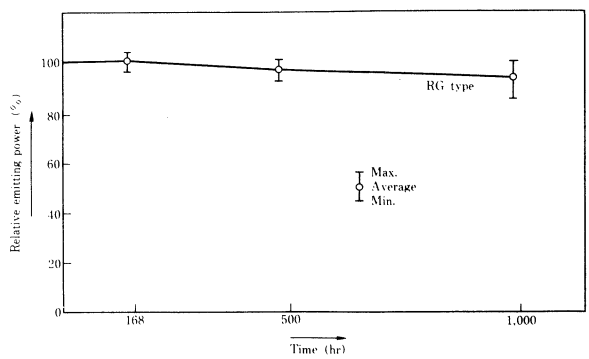


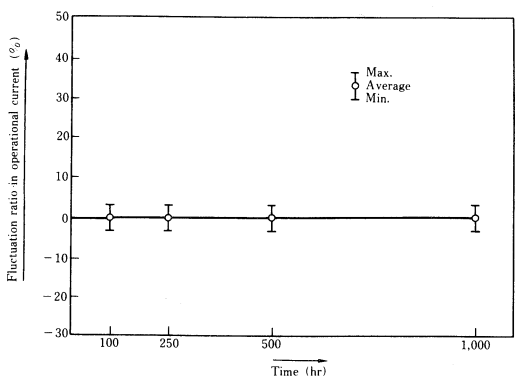
Table 33 Reliability test result for laser diodes

Test item	Test condition	Number of defects / Number of samples					
		HL7801E	HL7801G	HLP1500	HL8312E	HLP5400	HLP5500
Operation lifetime	50°C, N_2 atmosphere Po = 5mW, APC 1,000 times	0/100	0/100	0/20	0/50	0/50	0/20
Temperature cycle	−40 (30 min.) to 25(15 min.)to 70°C(30 min.) 10 cycles	0/50	0/50	0/45	0/50		0/20
Temperature cycle lifetime	−40 (30 min) to 25 (15 min.) to 70°C (30 min.), 100 cycles	0/20	0/20	0/10	0/20		0/10
Heat shock	0 to 100°C (5 min.) (5 min.) , 10 cycles	0/10	0/10	0/5	0/10	—	0/5
Soldering heat resistance	260°C, 10 sec.	0/10	0/10	0/5	0/10	—	0/5
High-temperature shelf test	Ta = 70°C, 1,000 times	0/10	0/10	0/5	0/10	0/10	0/5
High-temperature high-humidity shelf test	Ta = 60°C RH ≧ 90%, 1,000 times	0/50	0/50	0/10	0/50	—	0/20
Low-temperature shelf test	Ta = −40°C, 1,000 times	0/10	0/10	0/5	0/10	—	0/5
Shock	1,500G, 0.5msec XYZ directions 3 times each	0/10*	0/10*	0/5*	0/10*	0/5*	0/5*
Vibration fatigue	60Hz 20G XYZ directions 3 times each						
Vibration frequency vibration	100 to 2,000Hz, 20G XYZ directions 3 times each						
Lead toughness	Bending durability 225g, 90°, 3 times for both sides	0/5	0/5	0/5	0/5	0/10	0/10
Solderability	230°C, 5sec., Rosin flux	0/5	0/5	0/5	0/5	0/10	0/10
Air-tighting	(1) Bubble leak 100°C, Fluorinert (2) He leak 5×10^{-7} atm cc/sec	0/100	0/100	0/100	0/300	—	0/50

* Series test

Table 3-35 Reliability result for laser diode

Fluctuation in characteristics		Fluctuation in operational current (P_O = 5mW)
Product	HLP5400	
Test condition	Ta = 50°C, N_2 atmosphere with heatsink Po = 5mW APC	
Failure checking standard	Fluctuation ratio in operational current $^{+50\%}_{-30\%}$	
Failure mechanism	Nonradiative recombination current amplification	
Result: Fluctuation in operation current from high temperature constant-light-emission tests is plotted. Stable operation is obtained even after 1,000 hr.		
Note 400 type: Open-air type		



4. NOTES ON USING

4.1 MOUNTING ON A PRINTED CIRCUIT BOARD

Lead pins of packages are solder-coated or plated so as to be easily mounted on printed circuit boards. Normally, lead pins are soldered with eutectic solder. Typical mounting methods are explained below.

4.1.1 Mounting pin-insertion type packages

Pin-insertion package mounting consists of inserting lead pins of the package into the throughholes of about ϕ0.8mm on a printed circuit board and dipping them in the wave solder bath for soldering. This method can facilitate process up to solder immersion due to fixed lead pins, and realize automatic soldering easily. During soldering no wave solder should touch the package body. Solder touching might cause damage to the package.

4.1.2 Mounting surface mount packages

4.1.2.1 Basic mounting process flow

Fig. 4.1 flowcharts the basic process for mounting surface mount packages. First, soldering paste is applied to the footprint of a printed circuit board and an IC or LSI is placed on the board. Next, after the soldering paste dries, soldering is performed. Residual flux is then removed, followed by a visual inspection.

(1) Several types of solder pastes and fluxes are shown in Tables 4.1 and 4.2, respectively. To select a solder paste, composition, grain size, shape, flux content and viscosity should be considered to suit the application.

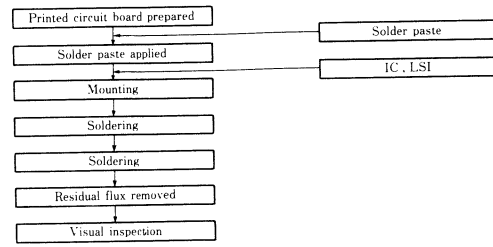


Fig. 4-1 Surface mount package mounting flow

Table 4-1 Typical Solder Paste Properties

Composition	Melting point	Grain size	Shape	Flux		Viscosity (at 25°C)	Remarks
				Content	Chlorine quantity		
Sn63/Pb37	183°C	250 mesh	Irregular Spherical	10Wt%	0.2Wt%	5×10^5 cp 3×10^5 cp	
Sn62/Pb36/Ag2	179°C	200 mesh	Spherical	15Wt%	0.2Wt%	2.5×10^5 cp	For Ag-soldered lead devices

Table 4-2 Types of Fluxes

I	Rosin-based flux 1 WW rosin (WW) 2 Activated rosin (RA) 3 Mild activated rosin (RMA)
II	Water-soluble flux (strongly activated mainly by organic acid)
III	Water-soluble rosin flux
IV	Synthetic rosin flux
V	Ester-based flux

(2) Application of solder paste

Solder paste is applied by screen printing or by discharge from a dispenser.
Screen printing . . . A screen is used as a mask, on which an appropriate amount of soldering paste is placed. Using a squeezer the thin screen is moved being pressed against the board surface to transfer or print the paste through the screen pattern onto the appropriate portion of the board surface.
Dispenser discharge technique . . . This technique involves discharging consistent quantities of solder paste through a needle by air pressure.

(3) Mounting

There are two ways of mounting a surface mount package on a board:
Vacuum pick-up and mechanical chuck. When a package is placed on a printed circuit board to fit the pattern of the package mounting area, it is roughly fixed by the flux's surface tension.

(4) Cleaning

Described in section 4.2.2.

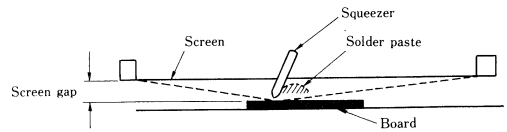


Fig. 4-2 Screen printing

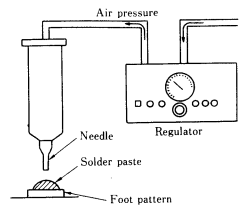


Fig. 4-3 Dispenser discharge

(5) Removal of residual flux

Any residual flux needs to be removed. Use a solvent such as alcohol, chloroethame or Freon. Note that for plastic packages, residual chlorine may deteriorate product reliability.

(6) Visual inspection

Soldered parts should be subjected to a visual inspection to insure good connection. Inspections by ultrasonic waves or laser are also available.

4.1.2 Soldering methods and their standard conditions

Main soldering methods for surface mount packages are shown in Table 4.3. These methods fall into two types: only the parts to be soldered are heated, or the entire device is heated.

Table 4-3 Methods for Soldering Surface Mount Packages

	Soldering method	Setup
Partial heat application	Iron	Soldering iron
	Pulse heater	Pulse current, Heater
	Hot air	Hot air blower
	Laser	Laser beam
Overall heat application	Infrared reflow	Infrared heater
	Vapor phase reflow	Cooling coil, Saturated vapor, Inert fluid, Heater
	Dipping	Wave solder (solder vessel for surface mounting)
	Furnace	Heater

(1) Infrared reflow soldering

Infrared light from a halogen lamp is concentrated using a reflecting mirror into a hot beam used for soldering. This method allows a large number of packages to be soldered at one time; it is suitable for high volume production. Reflow conditions depend on the package shape, board configuration and soldering equipment. Typical reflow conditions are shown in Fig. 4.4.

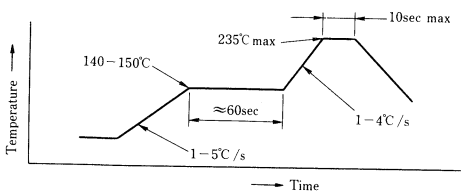


Fig. 4-4 Recommended reflow conditions

(2) Vapor phase reflow soldering

This technique utilizes the heat obtained from a fluorocarbon-type boiling point solvent. This method is advantageous in that soldering is performed independent of the device size and shape due to a constant temperature applied to the entire part (For example, 215°C for 3M company's Fluorinert FC5311). This feature reduces package damage caused by residuals on soldering parts and resulting uneven temperature. Examples of equipment and conditions are shown in Figs. 4.5 and 4.6, respectively.
The soldering methods described here are categorized with emphasis on thermal stress applied to parts and solderability, and do not consider productivity and cost.

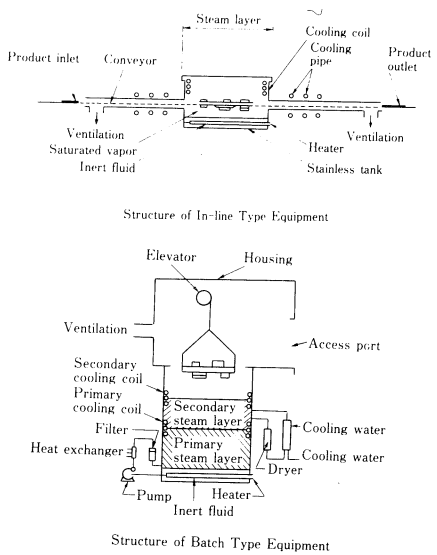


Fig. 4-5 Equipment for Vapor Phase Reflow Soldering (source: catalog from Japan Dynapart Co.)

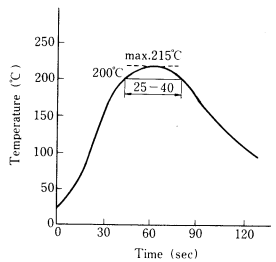


Fig. 4-6 Vapor phase reflow soldering conditions

4.3 APPLICABLE MOUNTING METHODS FOR EACH PACKAGE

Table 4.4 lists the applicable mounting methods for each package.

Table 4-4 Applicable Mounting Methods for Each Package

Mounting methods		IC/LSI packages					
		FPP	SOP	MSP	PLCC	FPG	LCC
Partial heat application	Iron soldering	○	○	○	○	○	X
	Pulse heater soldering	○	○	X	X	○	X
	Hot air soldering	○	○	○	○	○	○
	Laser soldering	○	○	○	○	○	X
Overall heat application	Infrared reflow soldering	○	○	○	○	○	○
	Vapor phase reflow soldering	○	○	○	○	○	○
	Dip-soldering	X	Note 1	○	X	X	X
	Furnace soldering	○	○	○	○	○	○

○ : Applicable for mounting
X : Unapplicable for mounting
Note 1: Applicable for 20-pin or less SOPs, but unapplicable for 24- and 28-in SOPs.

4.2 NOTES ON DESIGNING CIRCUIT SYSTEMS

Reliable circuit systems can be designed considering the following:
Initial specifications are satisfied

- Design margin is insured considering characteristics variations.
- Derating is applied.

Other considerations for achieving reliable circuits include wiring related problems, extraneous surge voltage, reactance loading, noise margin, and area of safety operation (A.S.O), reverse bias fly-back pulse, static electricity and pulse stress.

4.2.1 General precautions

Reliable system design is examined for two cases below :

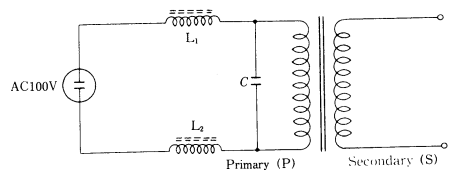
- A device is used in the range of specifications indicated in individual data sheets.
- A device is used in a special application such as digital ICs used in an analog circuit system (oscillator).

The former case allows derating based on parameters variations with time, used duty and temperature. Further, a failure rate can be predicted by simplified environmental factors.
The latter case includes applications such as TTLs driving loading capacitors or LEDs, or cases in which outputs are shorted. The following points should generally be noted when designing these systems.

(1) Ambient temperature should be kept as low as possible to keep semiconductor devices from becoming overheated.
(2) Supply voltages, input voltages and power dissipation should be maintained within rated values, considering derating.
(3) Excessive voltages caused by noise must not be applied to inputs/outputs and power supply pins.
(4) Plastic encapsulated semiconductor devices must be shielded from high electric fields. Devices exposed to a high electric field can cause polarization of plastic and the passivation film, which might result in malfunctions.
(5) No static electricity should appear during use.
(6) Since high speed devices employ fine processing, electrostatic pulses should be prevented by providing a protection circuit at the input stage.
(7) When turning power on/off, voltage must be applied constantly. If a voltage is applied to input and power supply pins with ground pins floated, excessive stress can be applied.
The above considerations are described using the following examples.

4.2.2 Noise and surge preventions

Surge voltage static electricity and noise are problems common to semiconductor devices.
Generally, electric devices are designed considering commercial power supply variations of about 10%. However, if devices are used near a machine generating a surge voltage, this surge can be superimposed on the power supply line causing malfunctions. Thunder may also induce an impulsive surge. This surge can be reduced by providing a filter as shown in Fig. 4-7 on the AC line.



$L_1 = L_2 = 2 - 10\text{mH}$, $C = 0.1 - 0.5\mu\text{H}$

Fig. 4-7 Surge absorber

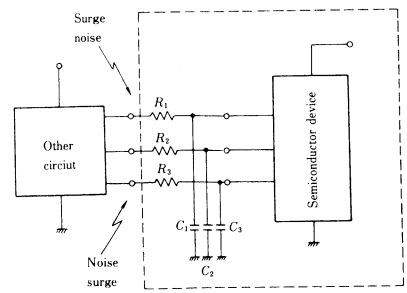
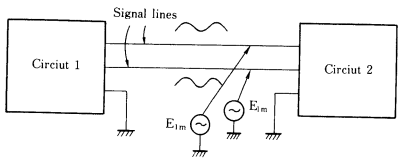


Fig. 4-21 Surge protection circuit

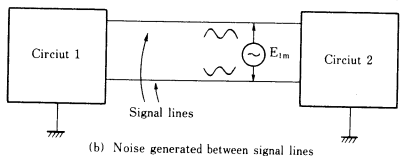
If surge or static electricity can possibly be directly applied to the semiconductor devices and other components on a board (not from the AC line), the device must be shielded. In this case, the impedance between the shield and ground must be low.
If there is a possibility of static electricity or surge pulses applied as noise, a protection circuit as shown in Fig. 4-8 is recommended. Time constants Ri and Ci should be determined so that surge pulses can be effectively absorbed without affecting device operation.

4.2.2.1 Types of noise

Noise is generated between earth and signal lines, or induced between signal lines (Fig. 4-9). The above cases have different effects on devices and require individual prevention techniques.



(a) Noise generated between grounds and signal



(b) Noise generated between signal lines

Fig. 4-9 Noise generation

4.2.2.2 Noise source and signal line coupling

Noise and signal line coupling is caused by:
(1) Conduction — leakage impedance exists between a noise source and signal lines
(2) Electrostatic induction — electrostatic coupling between a noise line and a signal line
(3) Electromagnetic induction — mutual conductance between a signal source and signal lines

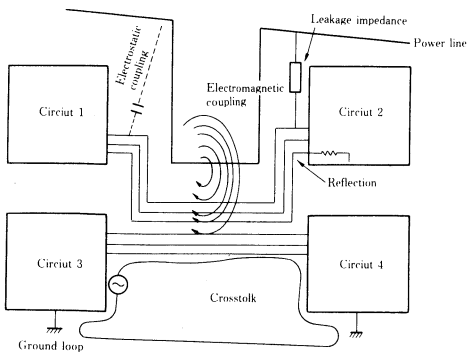


Fig. 4-10 Noise source and signal line coupling

(4) Cross talk — when two or more lines exist adjacently, electrostatic and electromagnetic induction cause one line to induce noise voltage on the other line.
(5) Ground loop — When both ends of a signal line are grounded, the potential difference between the two may cause noise.
(6) Reflection — Reflection caused by signal line impedance mismatching produces noise.
These couplings are illustrated in Fig. 4-10.

4.2.2.3 Countermeasures against noise

To construct a system which is not plagued by noise, the following should be considered.
- Eliminate or reduce the noise
- Pick up no noise
- Increase the noise margin
- Provide a compensation circuit

(1) Noise source

The most effective means of noise prevention is to control noise sources as described below.
- Insert diodes, resistors or capacitors in parallel into a relay coil to reduce surge voltage.
- Install a filter on the AC power line to prevent noise through the AC line.
- Shield equipment producing strong electric fields: these precautions eliminate the need for protecting the entire system from receiving noise. Another precaution is to place the device away from the noise source.

(2) Ground lines

Ground lines for circuits should be exclusively used and not commonly used with other ground systems to remove interference caused by currents flowing to ground. There must be only one connection and no closed loop between circuit systems and the frame (Fig. 4-11).

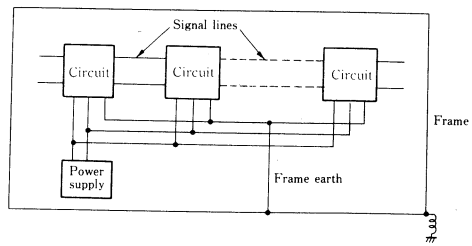
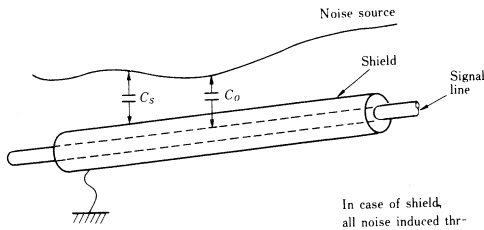


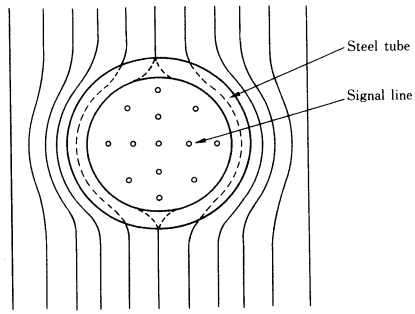
Fig. 4-11 Grounding of a circuit system

(3) Shields

It is recommended that signal lines or the entire system be shielded to reduce extraneous noise effects. A bond should be used to prevent noise due to electrostatic coupling. This permits noise on signal lines to be induced on the shield line and then to be bypassed to earth if there are no shields. The internal magnetic field of a system placed under a strong magnetic field can be attenuated by covering the system using magnetic material (Fig. 4-12). Steel tubes are usually used for the shield. Magnetic permeability materials are not employed due to their high price.



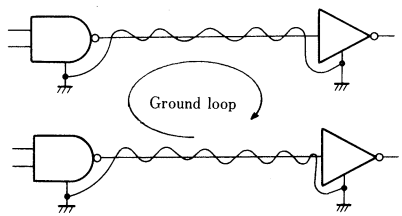
(a) Electrostatic shield



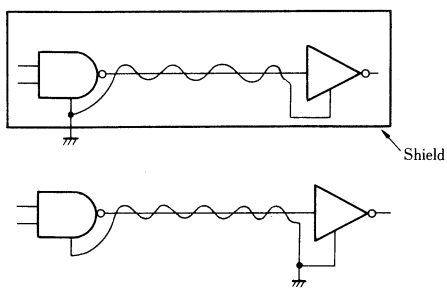
(b) Magnetic shield

Fig. 4-12 Shield example

Another shield type commonly used is twisted pair lines. Noise can be reduced by placing two signal lines symmetrically between receiver circuits, signal sources, ground and noise sources. Extraneous noise can be suppressed by reducing the twist pitch of signal lines in proportion to transmission distance. Further, if a shield is provided, protection against electromagnetic induction can also be obtained. Twisted pair lines may produce a ground loop, but this can be eliminated in the manner shown in Fig. 4-13.



(a) Ground loop is produced (bad example)



(b) No ground loop is produced (good example)

Fig. 4-13 Twisted pair line system

(4) Filters

Most power supply related noise originates from the AC line. This noise can be reduced by installing an AC line filter into the noise generating side or circuit system's AC supply side, which was illustrated in Fig. 4-7. Fig. 4-14 shows an example of the use of a switching regulator. This example reportedly accomplishes a noise voltage reduction of 0.3 to 20 MHz and approximately 20 dB.

From the point of view of circuit systems, power supply impedance should be lowered as much as possible. This can be achieved by placing capacitors at appropriate places on the power supply lines. In this case, it is desired to place in parallel a large capacitor as a bypass for lower frequencies and a small capacitor for higher frequencies.

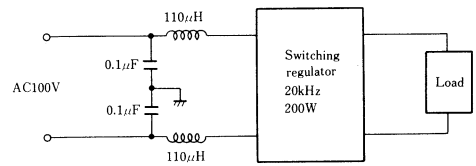
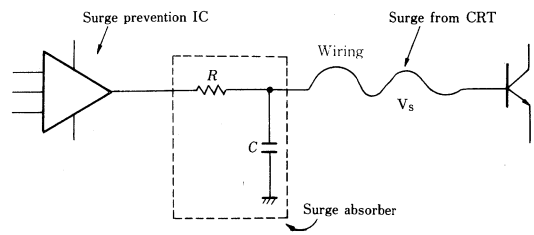


Fig. 4-14 AC line filter

4.2.2.4 Countermeasures against surge

For preventing voltage surges, surge incoming pins and paths should be determined and the following measures taken.

Surge voltage may be generated due to discharge when high voltage circuits are placed adjacent to each other such as when ICs and a CRT are incorporated in the same system. Various types of protection circuits against surge can be provided for an IC pin as shown in Figs. 4-15 to 4-17. Reliability improvement depends heavily on how much a surge voltage can be reduced. Fig. 4-15 illustrates a protection circuit placed at the output stage consisting of a capacitor and a resistor to reduce the surge induced on lead lines. Fig. 4-16 is a protection circuit placed at the input of a transistor used for a high frequency circuit. This circuit proves to be effective based on failure data from the field.



V_S : Surge voltage induced to wiring

Fig. 4-15 Absorber against surge from CRT

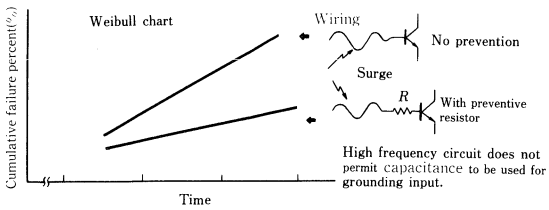
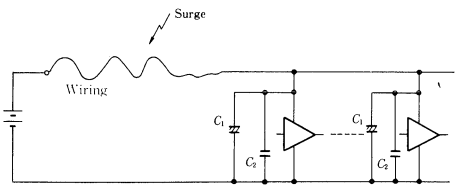


Fig. 4-16 Surge prevention for high frequency transistors



In power supply circiut, capacitors are inserted in parallel, since serial resistor are not permitted.
C_1 : Large capacitance
C_2 : Small capacitance

Fig. 4-17 Power line surge absorbtion

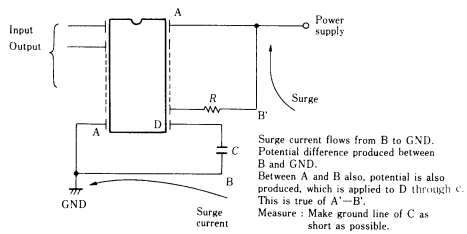


Fig. 4-18 Power line incoming surge prevention

Power supply lines at the same potential may induce a surge, producing a potential which may cause malfunction or destruction. In Fig. 4-18, surge produces potential between points A and B which were at the same potential. This surge can be prevented by employing a layout, wiring system and ground configuration that do not induce surge, or by providing a shield.

4.2.3 Characteristics parameters and reliability

Characteristic parameters of semiconductor devices are specified according to each device functions and application. The importance of each parameter depends on the application. For key parameters and ones having stringent system specifications, initial characteristic variation should be considered in designing systems and derating should be conducted. Since parameter variation is usually small under actual use, initial characteristic specifications may be used for most designs.

Parameters should be considered in terms of:

(1) The importance of the parameter: Is the parameter directly related to failures?
(2) Initial margin value of the parameter
(3) Whether parameter varies with age or not: is the variation in the direction having sufficient margin?
(4) Whether the margin permits the use of other devices or not.
(5) Whether redundant design is possible or not.
(6) Whether a statistical technique can be applied to the parameter design or not?

4.3 CHARACTERISTIC EVALUATION SOCKETS

4.3.1 Notes on handling sockets

(1) The lead spacing of the DIP except for the side brazed ceramic DIP is wider than standard ones of 300, 400, 600 and 900 mil. Therefore, you may have difficulty in inserting an IC in a socket since the lead tips do not match the socket taps. An appropriate jig should be used to insert and in particular to remove ICs.
(2) When soldering an IC inserted in a socket, an iron with high insulating resistance should be used; care should be taken so as to damage the IC by leakage current from the soldering iron.
(3) Use the IC socket within a heat resistance temperature of 125°C.

4.3.2 Socket purchasing

For details on each socket and their purchasing, please contact the agencies below.

(1) Yamaichi Denki Kogyo
Tel: 03(756)1191
(2) AUGAT
Tel 03(244)3788
(3) TEXTOOL
Tel: 044(711) 0022
(4) PLASTRONICS
Tel: 044(711)0022
(5) General Bussan
Tel 03(383)1711

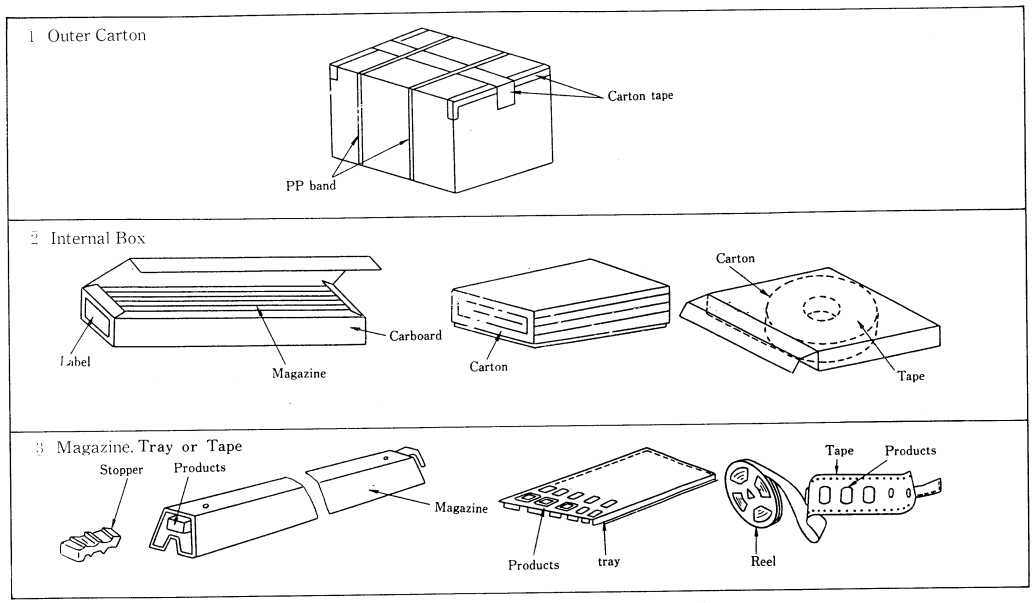
4.4 PACKAGE PACKING FORM

4.4.1 Unpacking cartons

LSIs are packed in magazines or trays in an internal box which is placed in an outer box as shown below. Unpack in the following order ① outer carton ② internal box. ③ magazine or tray. Be careful not to damage packages when unpacking from magazines, though the magazines or trays are designed to resist damage during shipment.

4.4.2 Precautions in handling magazines

(1) Outer cartons must not be subjected to any physical damage such as dropping.
(2) Magazines should be kept away from any water leakage. Do not leave them outdoors or store them under high temperature or humidity.
(3) Special care should be taken when handling the internal box. Dropping may jar the stopper causing devices to fall out of the magazine, resulting in deformed leads. Ceramic packages, if dropped, can be cracked, causing leakage failure.
(4) Though antistatic treatment is provided over the surface of transparent chloroethylene magazines, the following precautions should be taken:



(1) Adsorption of moisture removes the antistatic additives losing their effect.
(2) High temperature and high humidity make magazines sticky.
(3) Storage period should not exceed six months, as antistatic additives deteriorate with time.
(4) The transparent magazine with a surface resistance of less than 1×10^{10} Ω/□ is inferior to the black magazine with a resistance of less than 1×10^{6} Ω/□.

4.5 NOTES ON USING CODEC LSIs

– Latch up protection –

Since all Hitachi CODEC LSIs employ CMOS structure, general latch up protection is useful. In particular, the following protection procedures should be considered when using CODEC devices.

Latch up: A thristor phenomenon caused by parastic pnp or npn transistors unique in CMOS structure.

A CODEC has four power supply pins: AGND, DGND, V_{DD} and V_{SS}. Power should be applied to these pins in proper order. Voltage exceeding the absolute maximum rating may cause damage to the device.

4.5.1 Notes on inserting mounting boards

Special care should be taken when inserting or replacing a CODEC-mounted board with the system powered on. When the usual slow-starter power supply is turned on, voltages at each part of the board change slowly. Accordingly, a reverse current seldom exceeds the maximum rating. On the other hand, when a mounting board is inserted with the power on, a rapid voltage change can occur. This might cause element destruction, thermally disconnecting V_{DD} or V_{SS} on the device. In the case of V_{DD} disconnection, substrate bias is derived from I/O pins because of its CMOS characteristics resulting in unstable operation with the S/N ratio reduced. Thus, 'hot line insertion' is not recommended from the standpoint of reliability. If this is unavoidably required, the following must be considered.

Hitachi CODEC HD44230 and 240 series incorporate an inverse potential prevention circuit to prevent V_{SS} pin voltage from rising. This circuit can effectively prevent element destruction caused through hot line insertion. During power up sequence where a +5V V_{DD} pin is set up first, part of the negative supply current is dissipated to temporary activate the prevention circuit. Thus, ensure that the current capacity is high enough to set up the transition at power up.

When power must be applied to a large number of lines, the current capacity margin must set up a –5V at V_{SS} pin. After the power up sequence is completed, the current flowing in the prevention circuit is cut off. Accordingly, the current of rated input voltage is specified as a supply current in individual data sheets. In Hitachi CODECs, a sufficient current capacity is preserved at the negative power set up by simultaneously setting up two different types of slow-starter power supplies or by first setting up a –5V V_{SS} pin.

4.5.1.1 DGND and AGND connection on a mounting board

It is usually recommended that bypass capacitors are inserted between DGND and V_{DD} and between AGND and V_{SS}. However, CMOS structure is also formed between DGND and V_{DD}. If DGND and AGND are connected separately on a board, the impedance between V_{DD} and DGND becomes higher, which increases the possibility of latch up generated by noise during power up. The best way to prevent this is to connect DGND and V_{DD} pins together just before the CODEC. If the two lines are separately traced, they can be connected together just before the socket.

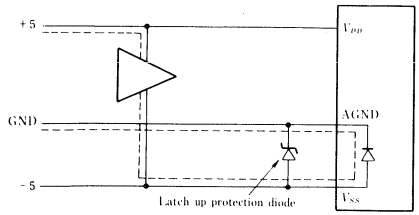


Fig. 4-19 Latch-up protection diode

4.5.1.2 Insertion of diodes against inverse voltage

If elements such as resistors and operational amps are inserted between V_{DD} and V_{SS}, current flows in the path of V_{DD}-V_{SS}-AGND/DGND through parastic diodes in the CODEC (Fig. 4-19). For eliminating this current, it is recommended that a diode such as a Shottky type be placed to suppress the voltage between AGND and V_{SS} to under 0.5V. The current capacity of the diode should be determined based on the amount of flowing from external circuits.

4.5.1.3 Currents flowing from other power supplies

Power supplies available on the CODEC board include ±12V, ±15V and –48V. These supplies may overdrive the +5V CODEC I/O pins. Usually, the current flowing through devices are not large enough to cause latch up, but care should be taken.

4.5.1.4 Bypass capacitors

When bypass capacitors are inserted between different power supplies, the potential may be inversed temporarily depending on the order in which the supplies are on. The following phenomenon can occur: 1) with capacitors placed between V_{DD}, V_{SS} and AGND pins, when V_{DD} and GND are powered with V_{SS} open, V_{SS} potential will rise to V_{DD} x C2/(C1 + C2), which may raise V_{SS} to a positive potential; actually, however, a fairly large capacity is required for potential inversion; and 2) in such an application that a –48V is applied with GND open, the GND potential may be pulled up to –48V and exceed V_{SS} (–5V).
The more power supplies are used, the more cases of inverse potential should be considered. Inverse potential can be prevented by providing larger bypass capacitors between V_{DD}-GND (=AGND=DGND) and between GND – V_{SS}.

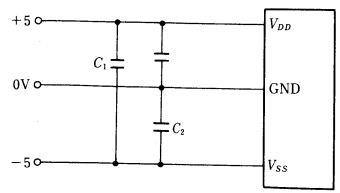


Fig. 4-20

4.5.2 Notes on inserting the CODEC into a socket

Power should be turned off before the CODEC is inserted into a socket. Insertion with power on may destroy the CODEC because the bypass capacitors have no effect.

4.5.3 Connection with a transformer, coil, etc.

Special care should be taken for connecting a transformer for a speech circuit with the CODEC. A voltage beyond the power supply voltage may be applied to the inputs when:

- rush currents are caused by intermittent currents through a telephone circuit.
- thunder surge leakage exist between coils.

and

- substrate potential has risen.

The circuit of Fig. 4-21 can be effectively used to prevent this problem. The peak voltage can be suppressed by a filter consisting of R1 and C (floating capacitance only is sufficient) and clamped by diodes. This prevents AOUT or AIN from being overdriven. Most cases does not require R2.
When long lines are connected to CODEC pins such as a microphone input and earphone output, these pins should be prevented from noise such as external spikes. When piezo elements are used for the microphone and earphone pins, these pins should also be prevented from the piezo effect when stress is applied.

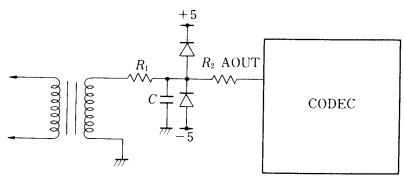


Fig. 4-21 Surge prevention circuit

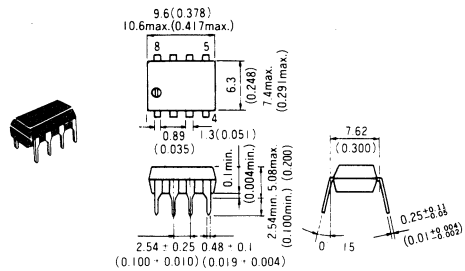
4.5.4 Digital output

Digital output pins employ open drain structure, but its substrate (WELL) is connected to DGND. Accordingly, voltages below DGND (0V) at these pins may cause latch up. Additionally, loading capacitance and transmission reflection effects should be considered. Since a diode is provided between V_{DD} and digital outputs, pull up voltage must not exceed V_{DD}.

PACKAGE INFORMATIONS

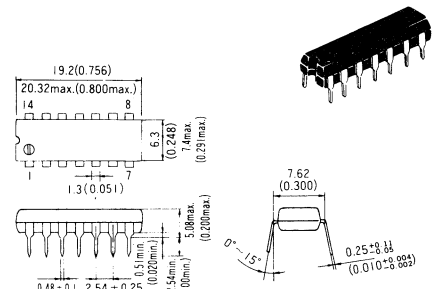
■**Plastic DIP** Unit: mm (inch), Scale: 1/1

8Pin



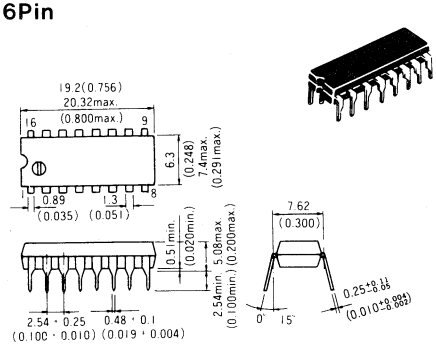
(DP-8)

14Pin



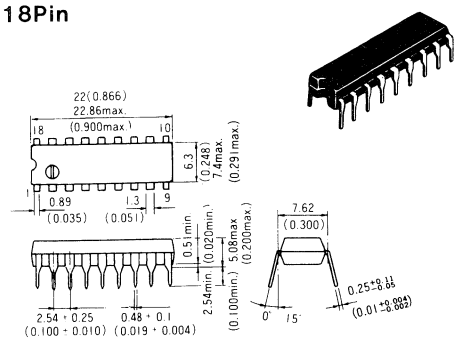
(DP-14)

16Pin



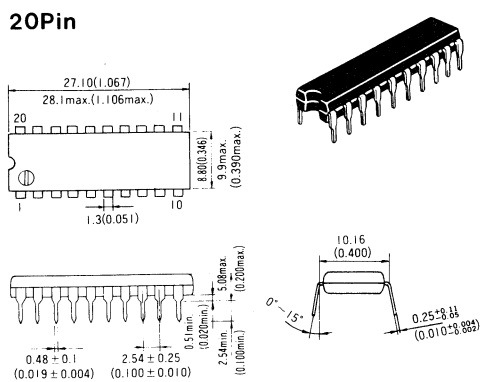
(DP-16)

18Pin



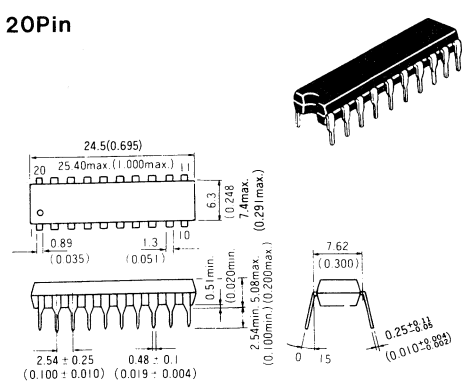
(DP-18)

20Pin



(DP-20)

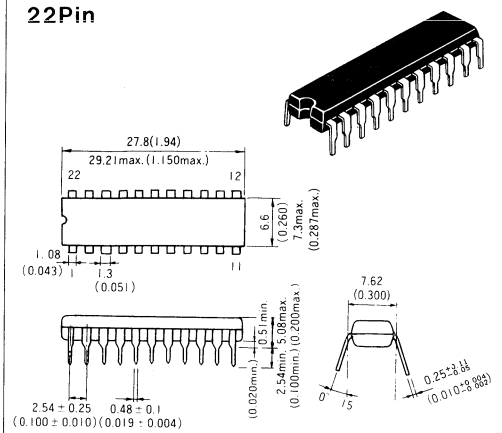
20Pin



(DP-20N)

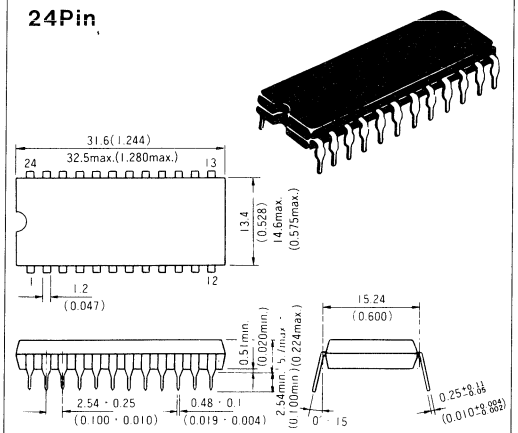
Unit: mm (inch), scale: 1/1

22Pin



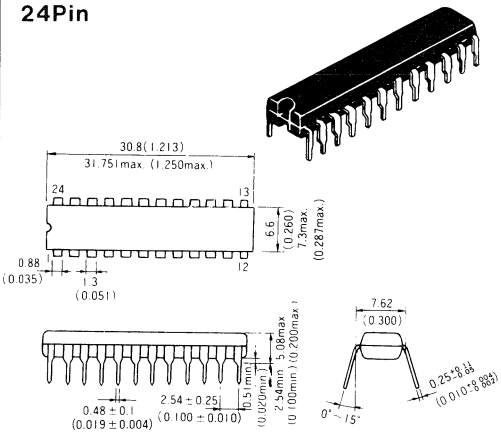
(DP-22N)

24Pin



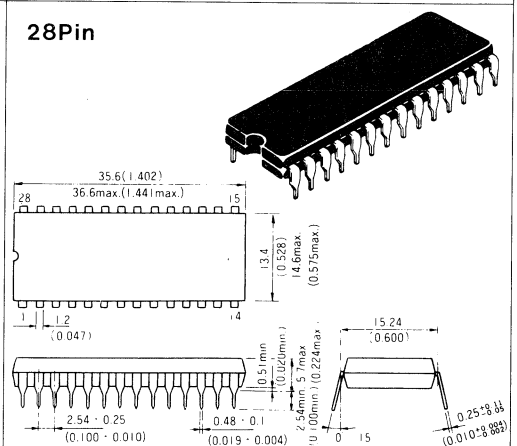
(DP-24)

24Pin



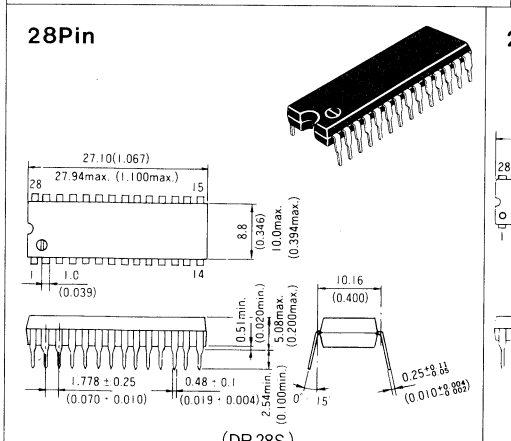
(DP-24N)

28Pin



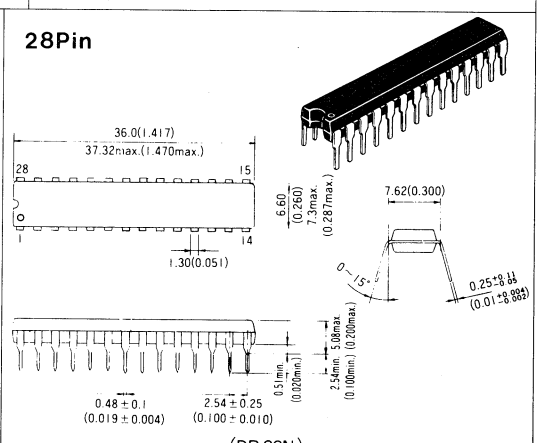
(DP-28)

28Pin



(DP-28S)

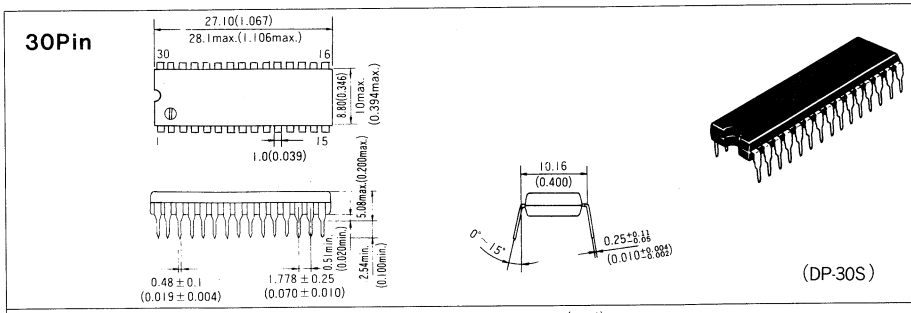
28Pin



(DP-28N)

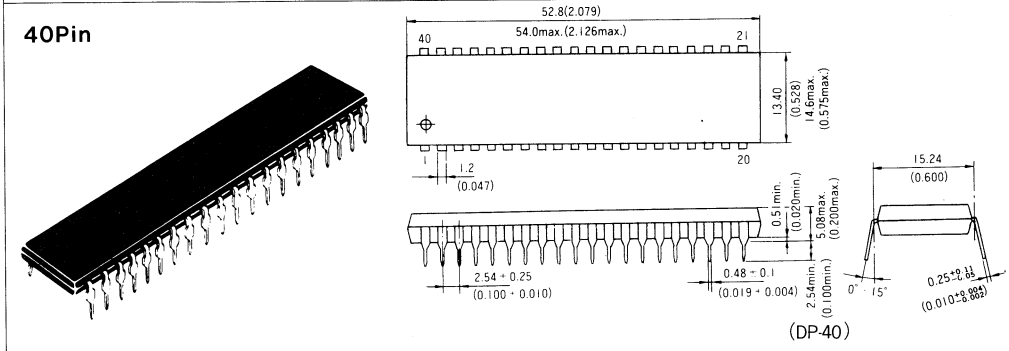
Unit: mm (inch) scale: 1/1

30Pin



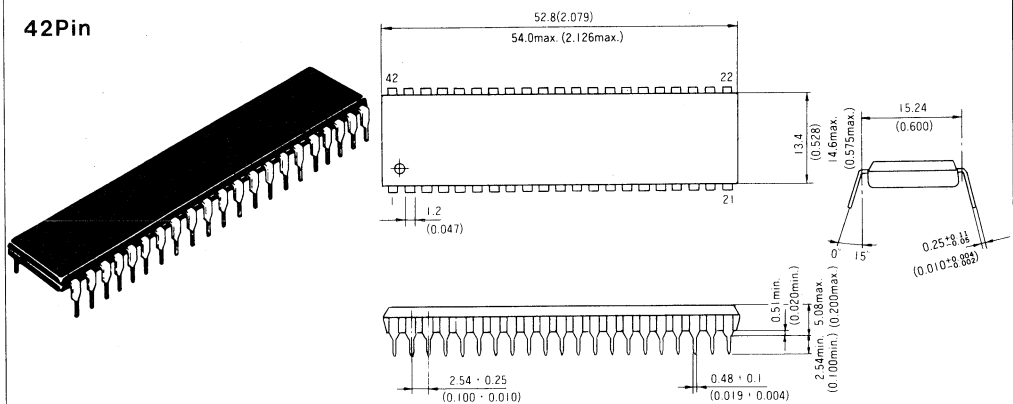
(DP-30S)

40Pin



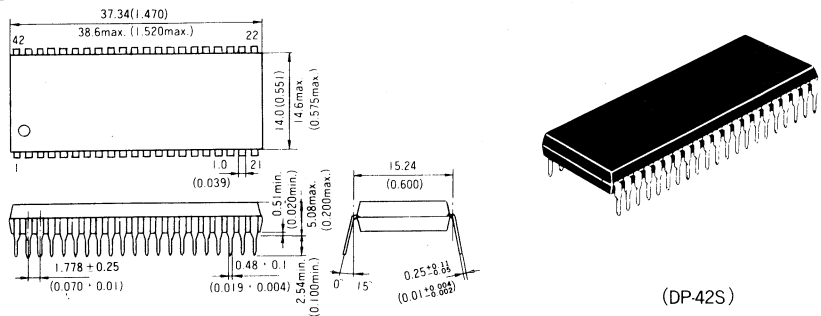
(DP-40)

42Pin



(DP-42)

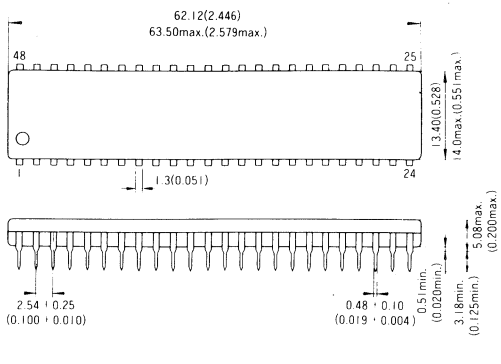
42Pin

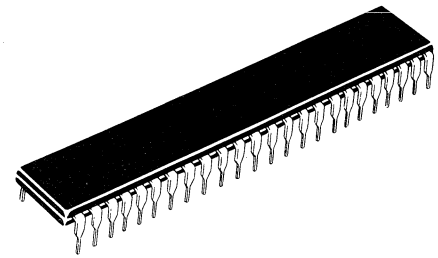


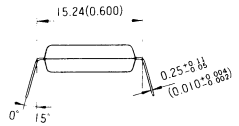
(DP-42S)

Unit: mm (inch), scale: 1/1

48 Pin

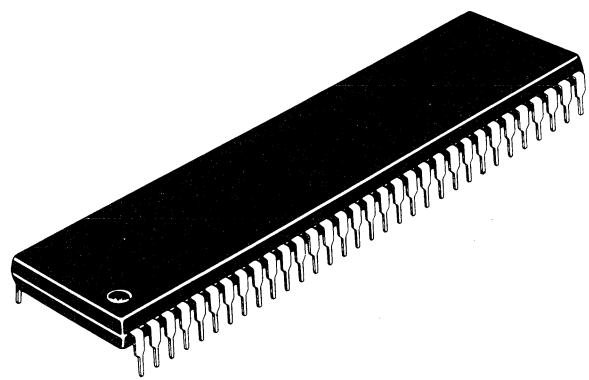


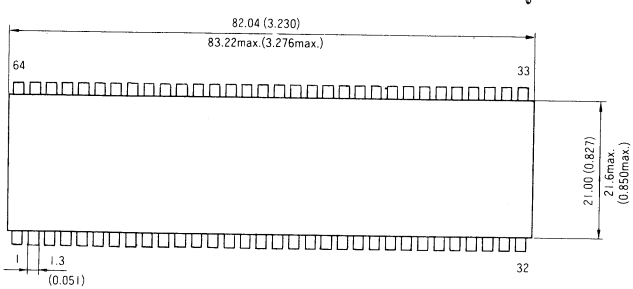


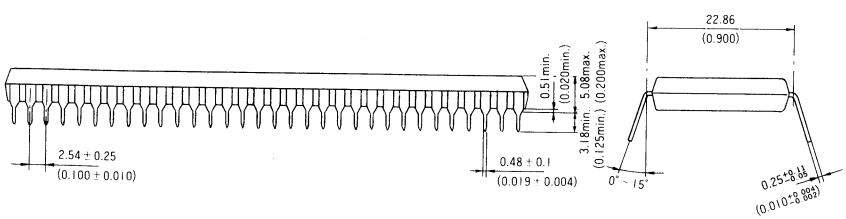


(DP-48)

64Pin



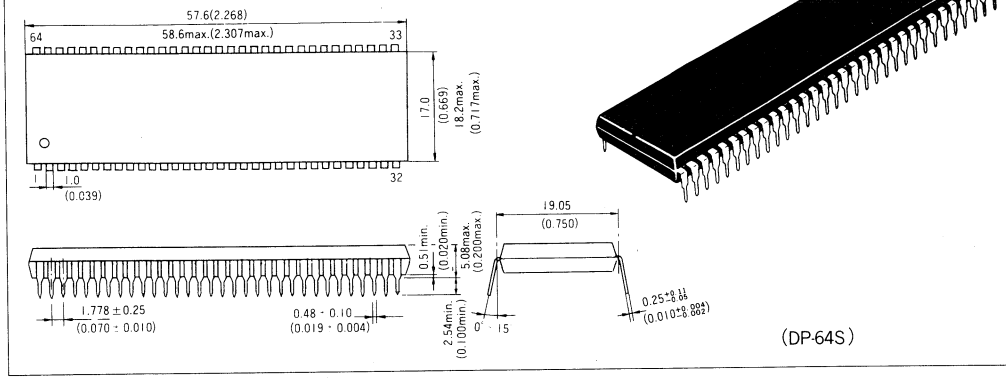




(DP-64)

Unit: mm (inch), scale: 1/1

64Pin

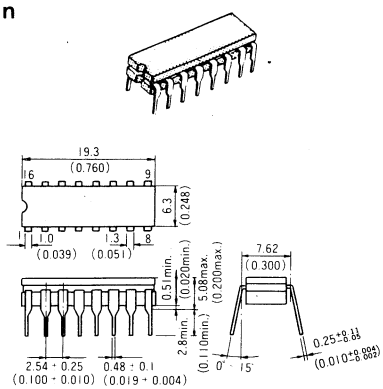


(DP-64S)

■ **Cerdip**

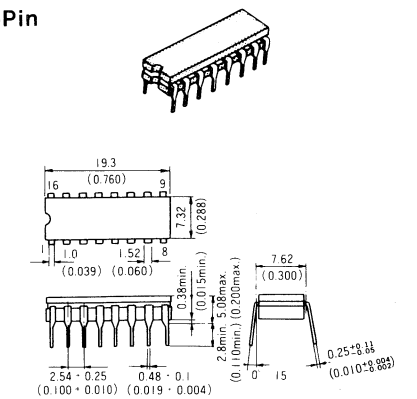
Unit: mm (inch), scale: 1/1

16Pin



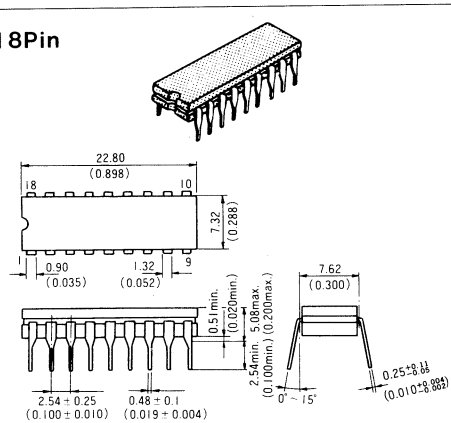
(DG-16)

16Pin



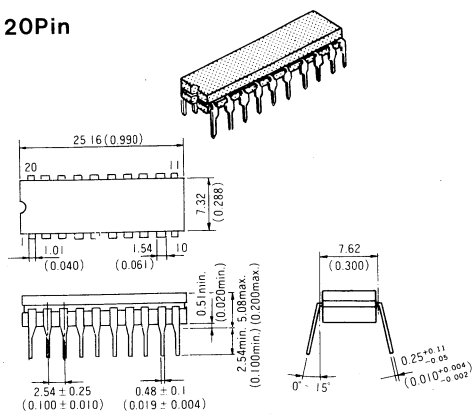
(DG-16A)

18Pin



(DG-18)

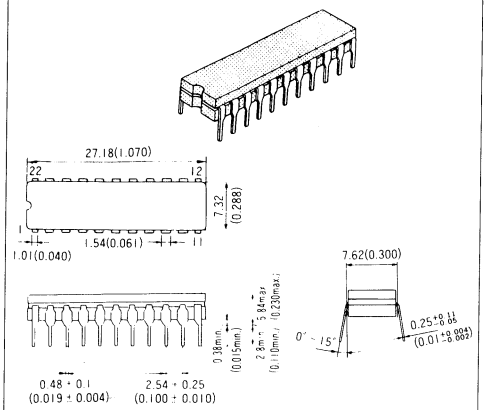
20Pin



(DG-20N)

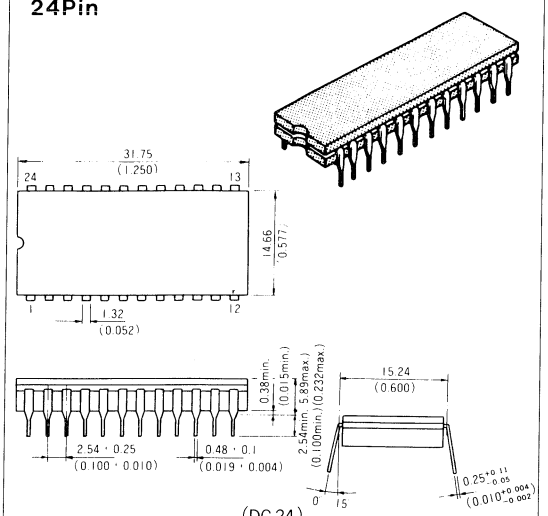
Unit: mm (inch), scale: 1/1

22Pin



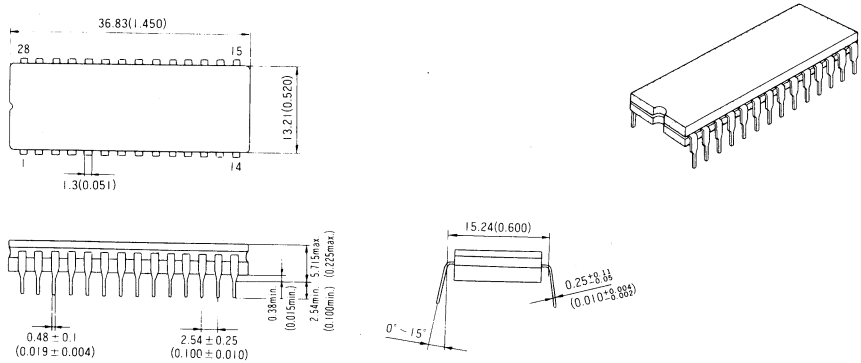
(DG-22N)

24Pin



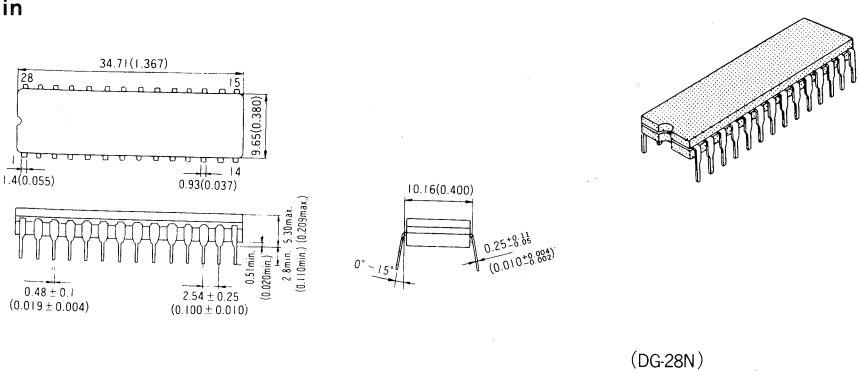
(DG-24)

28Pin



(DG-28B)

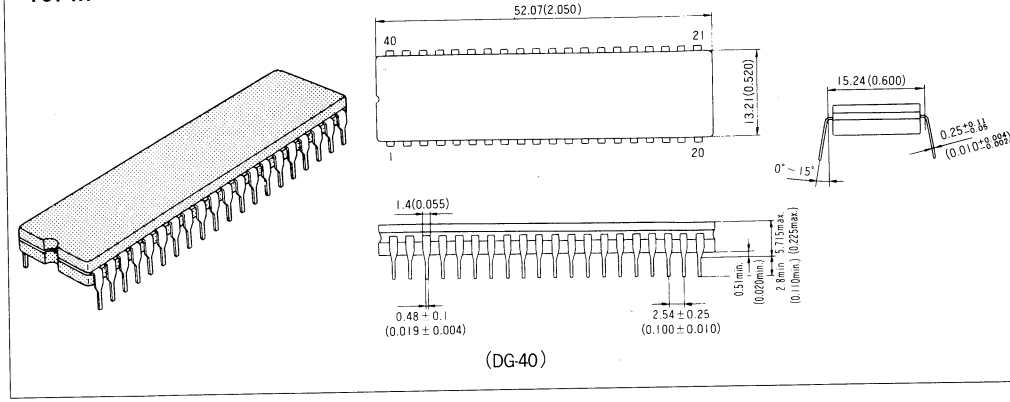
28Pin



(DG-28N)

Unit: mm (inch), scale: 1/1

40Pin

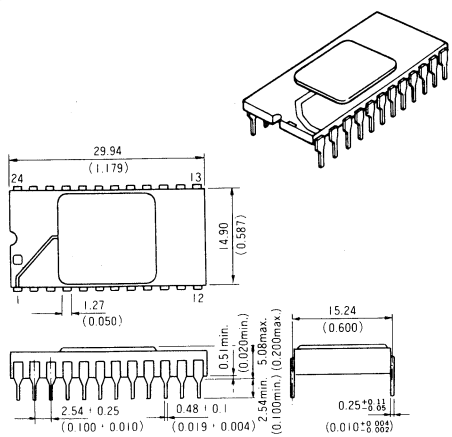


(DG-40)

■Ceramic DIP

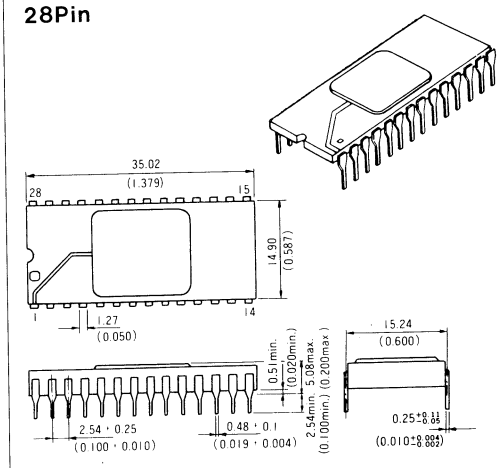
Unit: mm (inch), scale: 1/1

24Pin



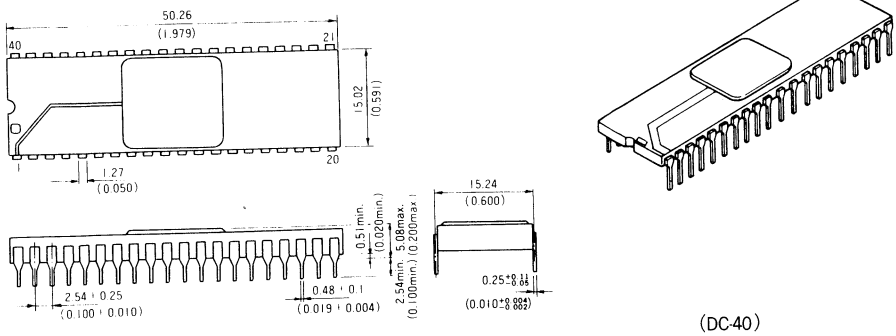
(DC-24)

28Pin



(DC-28)

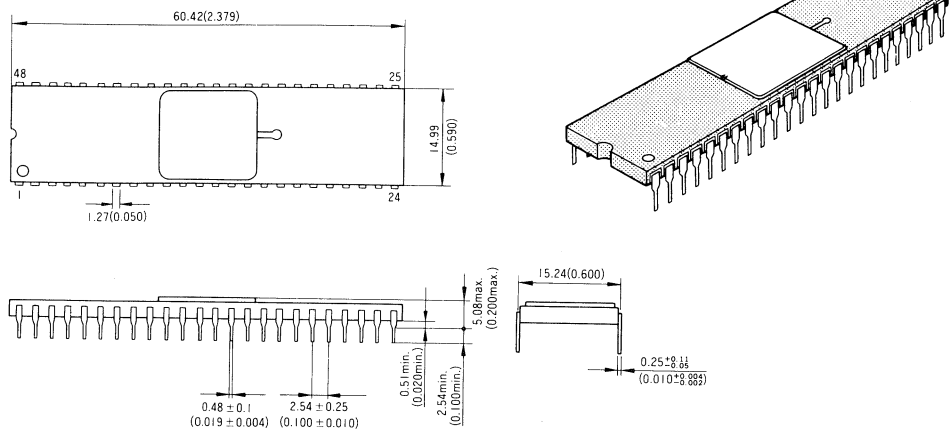
40Pin



(DC-40)

Unit: mm (inch), scale: 1/1

48Pin

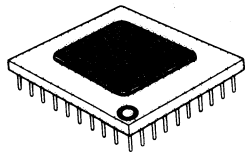


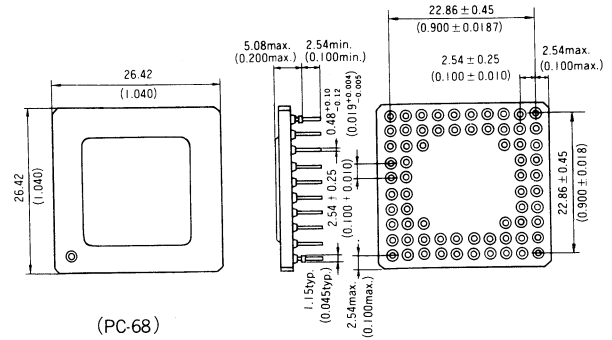
(DC-48)

■Pin Grid Array

Unit: mm (inch), scale: 1/1

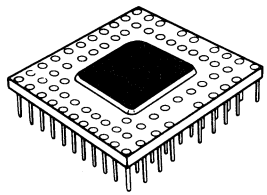
68Pin

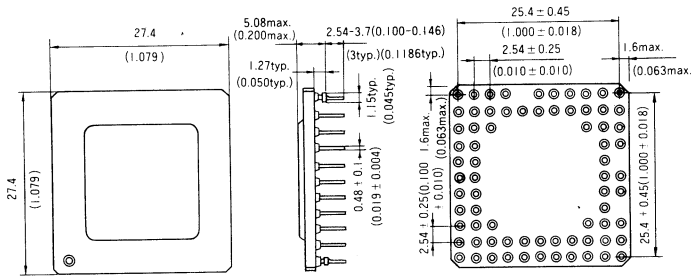




(PC-68)

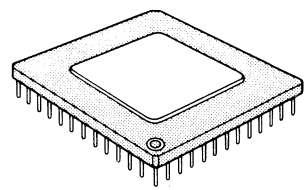
72Pin

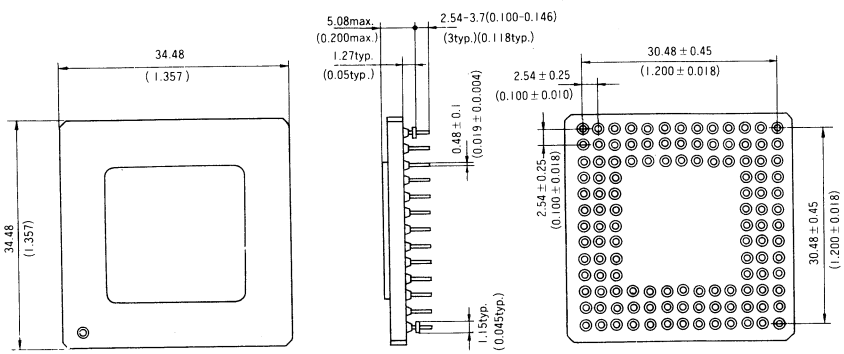




(PC-72)

120Pin



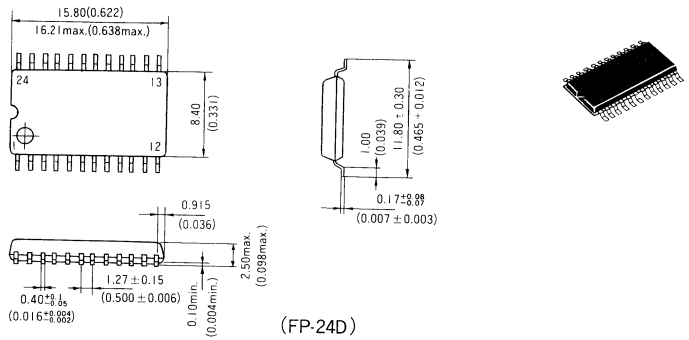


(PC-120)

■Plastic Flat Package

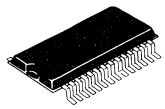
Unit: mm (inch), scale: 1½

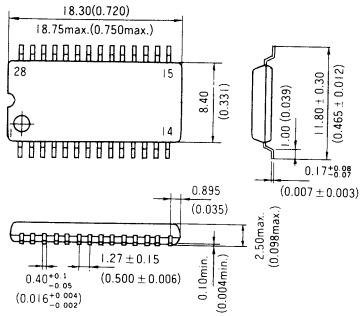
24Pin



(FP-24D)

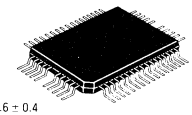
28Pin

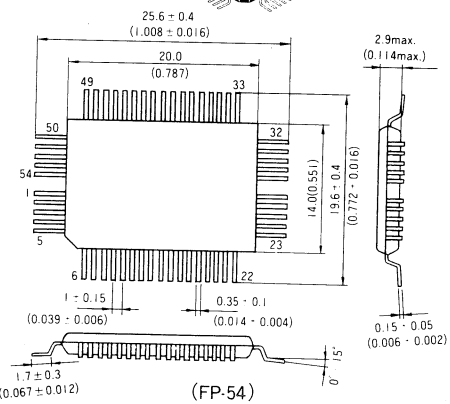




(FP-28D)

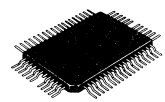
54Pin

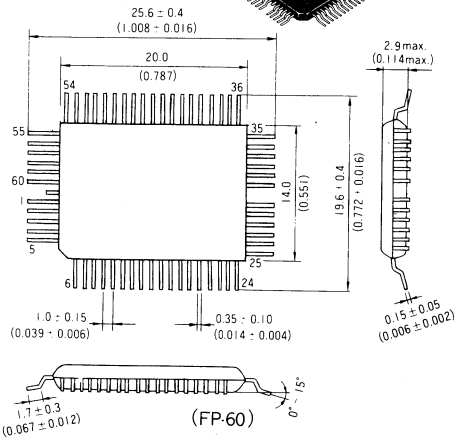




(FP-54)

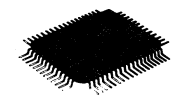
60Pin

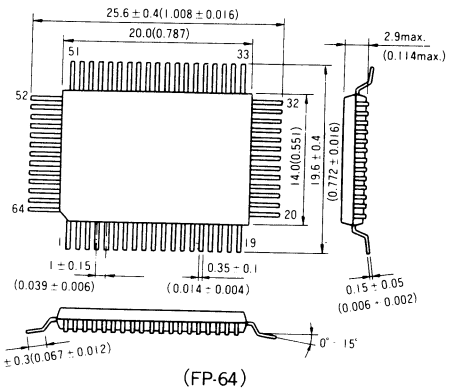




(FP-60)

64Pin

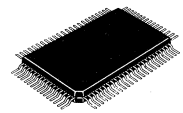


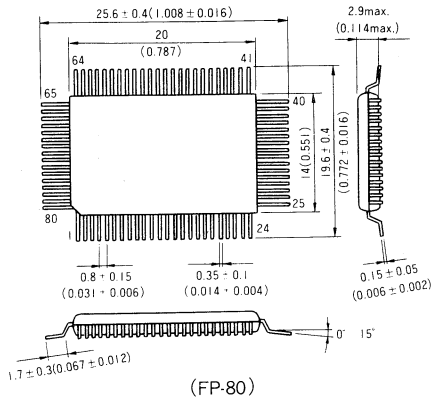


(FP-64)

Unit: mm (inch), scale: 1½

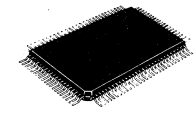
80Pin

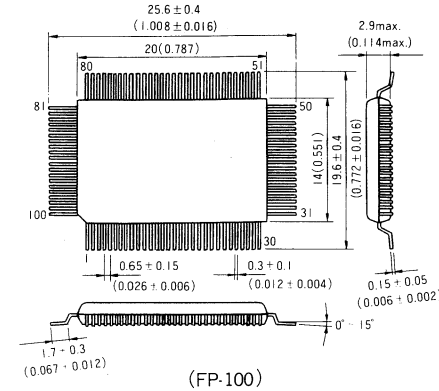




(FP-80)

100Pin



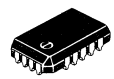


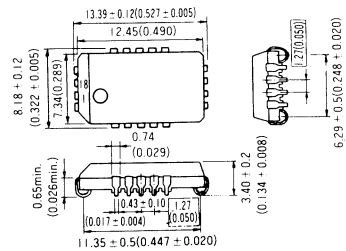
(FP-100)

■Plastic Leaded Chip Carrier

Unit: mm (inch), scale: 1½

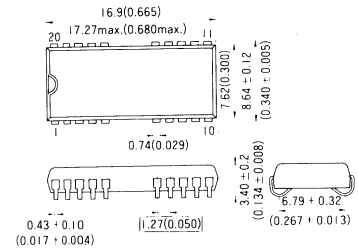
18Pin





(CP-18)

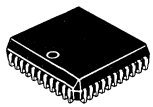
20Pin

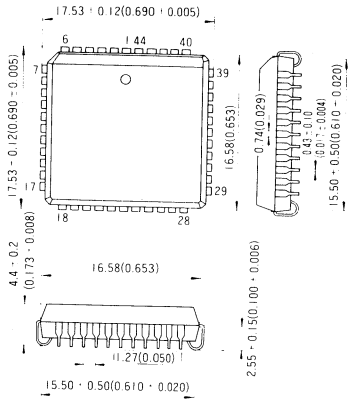


(CP-20D)

Unit: mm (inch), scale: 1½

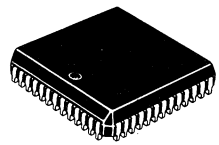
44Pin

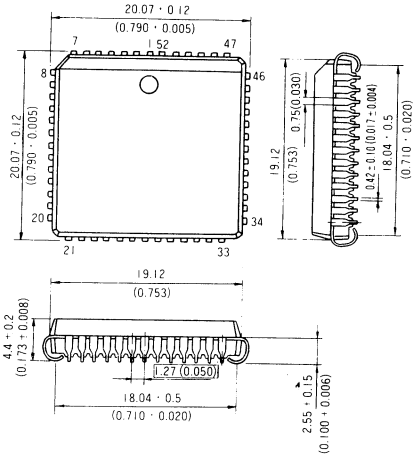




(CP-44)

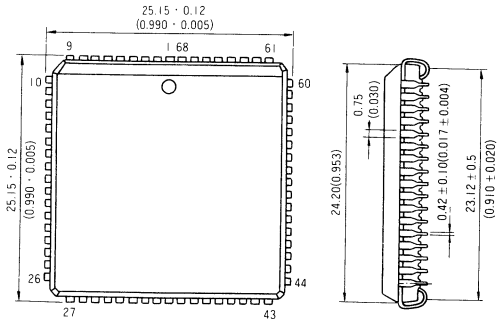
52Pin

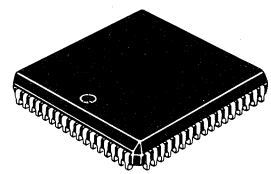


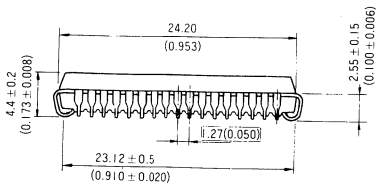


(CP-52)

68Pin



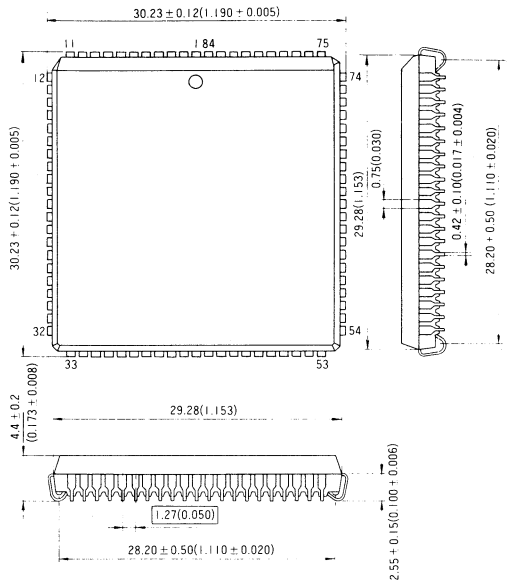


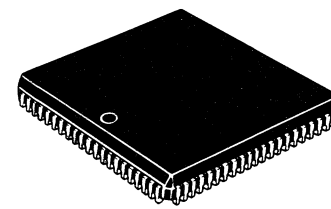


(CP-68)

Unit: mm (inch), scale: 1½

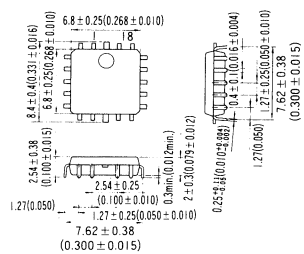
84Pin





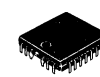
(CP-84)

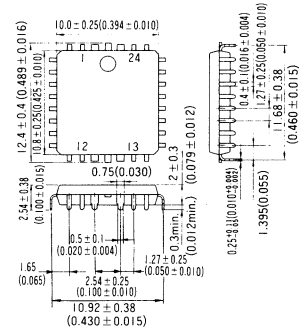
18Pin



(MP-18)

24Pin

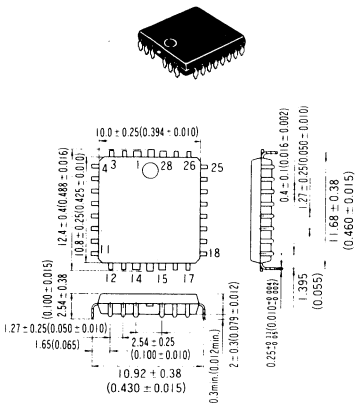




(MP-24T)

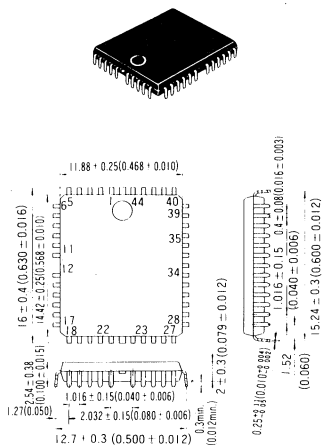
Unit. mm (inch) scale: 1½

28Pin



(MP-28)

44Pin



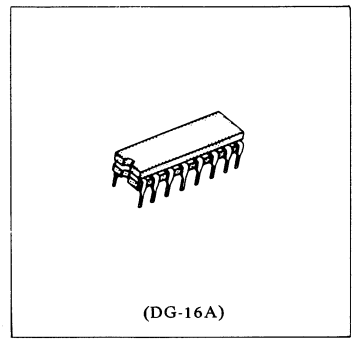
(MP-44)

DATA SHEETS

CODEC, SLIC

HD44230C,HD44240C Series

Single Chip CODEC/Filter Combo LSI



(DG-16A)

■COMMON FEATURES

● COMBO-CODEC ;

The complete function of CODEC with filters is provided in a single chip LSI.

● CMOS Structure ;

The structure and the power down mode to reduce the CODEC power dissipation during the on-hook or nonselected channel reduce the system power requirement.

● Conventional Power Supply Requirement ;

±5V power line operation provides the analog interface on the system ground level without DC decoupling capacitor, and the TTL level interface of digital signals. The digital ground and the analog ground is separated completely and are assigned to the respective pins, to minimize the system noise problem.

● CCITT-followed companding law ;

A-law or μ-law is selected by the metalization mask option using same base chip to assemble as the different LSI. This method is our approach to reduce both the wafer fablication and the testing cost. And the precise A/D or D/A converters are achieved by the circuits which consist of the capacitor array for segments of companding law, and the resistor string for steps.

● Excellent Voltage Reference ;

The 2.5V reference voltage to determine the A/D conversion or D/A conversion is provided on chip. The CMOS band gap reference is stabilized using circuit techniques to the power supply voltage and the ambient temperature. The level of the reference is also adjusted internally during wafer-sort process using poly-Si fusing techniques to achieve the system gain tolerance requirement.

● Offset Cancelled Encoder ;

The internal sign-bit integration circuit with no external component compensates the offset for the small signal level or idle channel state into the first step of the companding law. The idle channel noise of A-law device is squelched by the sign-bit fixation technique.

● Switched Capacitor Filter ;

The filters conform the band pass filter for transmit side, and the low pass filter to compensate the aperture degradation for the receive side. Their clock frequencies are designed as 128 kHz for low pass filtering and 8 kHz for high pass filtering as the best approach to reduce the die size and cost. To protect the folding effect at 128 kHz clock at the analog input, 128 kHz fillter cosine filter and 20 kHz (typ.) roll-off analog filter is provided on chip (antialiasing filters).

● Analog Input Gain Adjustment ;

The operational amplifier is provided to adjust the analog interface level in the range of 0-15dB.

● Open Drain Output of PCM Data ;

This provides the wired-or connection of 2 to 8 channel PCM data outputs using only one pull-up resistor, and reduce the difficulty of noise coupling to analog part through power supply line for the tri-state approach of the pin.

● Master Clock Generator ;

The 128 kHz master clock to determine the A/D, D/A conversion timing and to operate the switched capacitor filter is provided internally by the counter circuit to devide the bit-shift clock, or the PLL circuit to multiply the 8kHz synchronization clock, for the respective types of CODEC.

● Small/Standard Package ;

The CODEC is assembled in the small/standard 16 pin Dual-in-line ceramic package(CERDIP).

■LINEUP & SELECTION GUIDE

The HD44230C series are revised version of HD44231B/232B/233B/234B/235 236/237/238. They have better characteristics of PSRR, absolute delay, gain stability, and analog output drivability than B series. And the CR filter of analog input is separated completely to provide the flexible analog interface configuration and to reduce the noise from negative input. They have upward and pin to pin compatibility with B series. The HD44240C series have the push/pull type of analog output to provide the large output swing for the transformer interface, despite of slitely larger power dissipation. Other configuration and characteristics are just same as HD44237C/HD44238C.

HITACHI SINGLE CHIP CODEC/FILTER LINEUP

Series	Type	Comp. Law	Power (Typ.)	Clock			Decoder Shift	Input Amp	Output Amp	
				Internal Clock	Sync/Async Operation	PCM Bit Clock Rate			Type	Min Load
44230C	HD44233C	A	50mW	Divider Included	Both	1536/ 1544/ 2048kHz	–	Fully Uncommited OP-AMP		600Ω
	HD44234C	μ								
	HD44237C	A		PLL Included	Both	64- 2048kHz	–			
	HD44238C	μ					√			
44240C	HD44247C	A	70mW	PLL Included	Both	64- 2048kHz	–	Same as above	Push-Pull	600Ω
	HD44248C	μ					√			

Single Chip CODEC with Filters (COMBO)

■ FEATURES

- o SINGLE CHIP CMOS CODEC WITH FILTER IN 16-pins DIL PACKAGE
- o POWER SUPPLY VOLTAGE ± 5V±5%, LOW POWER DISSIPATION (50mW typ.)
- o FOLLOWS A-LAW (HD44233C)
- o FOLLOWS μ-LAW (HD44234C)
- o EXCEEDS CCITT SPECIFICATIONS & D4
- o SYNCHRONOUS / ASYNCHRONOUS OPERATION FOR 2048/1544/1536kHz PCM RATE
- o INTERNAL CLOCK GENERATOR
- o ANTI-ALIASING FILTER (2nd order CR Active Filter)
- o VOLTAGE REFERENCE (INTERNAL-TRIMMED)
- o INPUT AMPLIFIER
- o AUTO-ZERO CANCEL CIRCUIT WITHOUT EXTERNAL COMPONENT

■ PIN CONFIGURATION

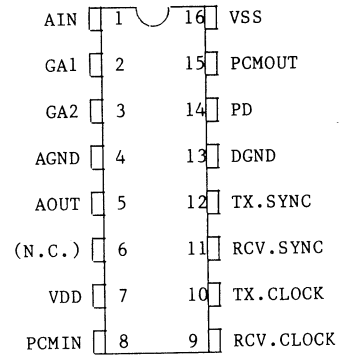


Fig.1 PIN ASSIGNMENT

(top view)

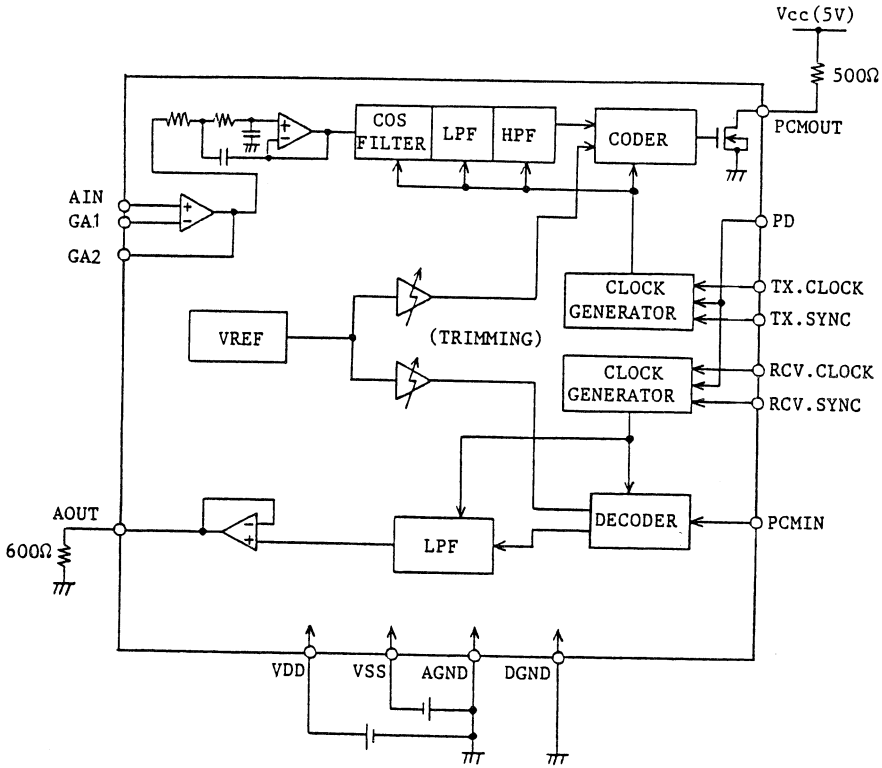


Fig.2 BLOCK DIAGRAM

Table 1. PIN DESCRIPTIONS

HD44233C HD44234C No.	SYMBOL	FUNCTION	REMARKS
1	AIN	ANALOG INPUT	
2	GA1	GAIN ADJUST1	FEED-BACK INPUT
3	GA2	GAIN ADJUST2	10kΩ≦RL CL≦100pF
4	AGND	ANALOG GROUND	
5	AOUT	ANALOG OUTPUT	RL≧600Ω, CL≦100pF
6	N.C.		OPEN
7	VDD	POSITIVE POW. SUP.	5V±5%
8	PCMIN	PCM DATA INPUT	(TTL)
9	RCV.CLK	PCM BIT CLOCK	(TTL)2048/1544/ 1536kHz
10	TX.CLK		
11	RCV.SYNC	SYNCHRONIZATION	(TTL) 8kHz
12	TX.SYNC		
13	DGND	DIGITAL GROUND	
14	PD	POWER DOWN	(TTL) "0" = down
15	PCMOUT	PCM DATA OUTPUT	OPEN DRAIN
16	VSS	NEGATIVE POW.SUP.	-5V±5%
			OPEN
			OPEN

■ GENERAL DESCRIPTION

The HD44233C, HD44234C are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band limiting filters and the analog/digital conversion circuits that conform to the A-Law or μ-law companding characteristic.

HD44233C is A-Law. HD44234C is μ-Law.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of $\pm$ 5V.

For a sampling rate of 8 kHz, PCM input/output data rate can be selected from 1536/1544/2048 kHz in synchronous or asynchronous operation.

■ FUNCTIONAL DESCRIPTION

Figure 2 shows the simplified block diagram of the HD44233C and HD44234C. The devices contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. The relationship between the PCM data word and the audio signal is defined just same as CCITT G711 Table 1 for HD44233C, Table 2 for HD44234C respectively. A band-gap voltage generator supplies the reference level for the conversion process. 2nd Order CR Active Filter is implemented on chip to avoid the aliasing noise which is caused by the clock of transmit filter.

1) TRANSMIT SECTION

Input analog signals first enter the chip at the uncommitted amplifier terminals. This op amp allows gain trim to be used if desired to set the 0dB or 0 level in the system. This amplifier also operates as the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 32dB (typ) at 256kHz and 40dB (typ) at 512kHz, the "effective" clock frequency of the following switched-capacitor Cosine Filter. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 128kHz, followed by a 3rd Order High-Pass Filter clocked at 8kHz. The resulting band-pass characteristics meet the CCITT, G.712 specifications. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The 8-bit PCM data is clocked out by the shift clock at one of 1536/1544 /2048kHz. A auto-zero loop (without any external capacitor) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

An additional feature of the HD44233C is a signbit fixation circuit to reduce the idle channel noise during quiet periods. It is of particular importance because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

2) RECEIVE SECTION

A shift clock, at one of 1536/1544/2048kHz, clock the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 128kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 600Ω.

3) COMPANDING LAW

The encoding and decoding characteristics of the Codecs comply with the requirements of CCITT G711 table 1 or Table 2, corresponding to their comparing law. The even bits of PCM words are inverted for A-Law devices. Positive logic is used (the High level corresponds to '1').

4) POWER DOWN LOGIC

Powering down the CODEC can be done in several ways. The most direct method is to drive the PD pin to a low level. Stopping SYNC input will also put the chip into the stand-by mode. The input can be held high, low or disconnected. After the chip being activated by these functions, the PCMOUT is in high impedance state and the AOUT is connected to AGND for about 1 msec to avoid the power-on noise.

5) VOLTAGE REFERENCE CIRCUIT

A temperature compensated band-gap voltage generator provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply it to the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed to ensure a minimum gain error of $\pm$ 0.1 dB at the nominal power supply voltage and the room temperature.

6)TIMING REQUIREMENTS

The CODECs do not require that the 8kHz transmit and receive sampling strobes should be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe, forcing the PCM output in a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and shift clock is synchronized to it. The clock rate can be selected from 1536/1544/2048 kHz.

7)SYSTEM CLOCK

The basic timing of the Codecs is provided by the shift clock.

This 1.536/1.544/2.048 MHz clock is divided down internally to provide the various filter clocks and the timing for the conversions. No external control signal for the selection is required.

PIN/FUNCTION DESCRIPTIONS

PIN	NO	DESCRIPTIONS
TX.CLOCK RCV.CLOCK	9 10	One of 1.536 ,1.544, 2.048 MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the SYNC, TX.SYNC/RCV.SYNC respectively.
TX.SYNC RCV.SYNC	11 12	These TTL compatible pulse inputs (typ.8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the CLOCK, TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the CLOCK, TX.CLOCK/RCV.CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK,TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC,TX.SYNC/RCV.SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500Ω pull-up per 8 Codecs is required.
PCMIN	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of CLOCK, RCV.CLOCK.
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of -VREF to +VREF to the device. The input stage can be connected as a unity gain amplfier, amplifier with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10kΩ or directly connected to GA1. GA1 is the negative feed back input of the amplifier. CL should be less than 100 pF.
AOUT	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 ohms. CL should be less than 100 pF.
VDD VSS AGND DGND	7 16 4 13	These are power supply pins. VDD and VSS are positive and negative supply pins respectively (typ. +5V, -5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	When this TTL compatible input is held low, the chip is put into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect. This pin should be pulled-up to VDD to keep the device active or to control ON/OFF with strobes.

■ ABSOLUTE MAXIMUM RATING

No.	ITEM	RATING
1	VDD	-0.3 to +7V
2	VSS	+0.3 to -7V
3	STORAGE TEMPERATURE	-55°C to 125°C
4	POWER DISSIPATION	0.5W
5	DIGITAL INPUT/OUTPUT VOLTAGE	-0.3V<VIN<VDD+0.3
6	ANALOG INPUT/OUTPUT VOLTAGE	VSS-0.3V<VIN<VDD+0.3

■ ELECTRICAL CHARACTERISTICS

1) STATIC CHARACTERISTICS

(VDD = 5±0.25V, VSS = -5±0.25V, VCC = 5±0.25V, TA = 0-70°C)

No.	SYMBOL	PIN No.	DESCRIPTIONS	SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE/ CONDITIONS
1	IDD	7	VDD CURRENT(OPE.)		5.5	10	mA	Note 1) AIN=0V PCMIN = +0 CODE RL(GA2) = 10kΩ RL(AOUT)= 600Ω
2	ISS	16	VSS CURRENT(OPE.)	-10	-4.5			
3	IDDST	7	VDD CURRENT(St.By.)		0.3	1		
4	ISSST	16	VSS CURRENT(St.By.)	-0.2				
5	IL	1,2,8 9,10 14	LEAK CURRENT	-10.0		10.0	µA	VM=0.8V
				-10.0		10.0	µA	VM=2.0V
						10.0	µA	VDD=VM=5.25V
6	IPL	11,12	PULL UP CURRENT	-100		0	µA	
7	IDL	15	LEAK CURRENT			10.0	µA	VDD=VM=5.25V
8	CAIN2	1,2	ANALOG INPUT CAP.			10	pF	at 1MHz Vbias = 0V
9	CDIN	8,9 10,11 12,14	INPUT CAPACITANCE			10	pF	at 1MHz Vbias = 0V
10	ROUTA	5	AOUT RESISTANCE		1	10	Ω	
11	ROUTG	3	GA2 RESISTANCE			30	Ω	NOTE 1
12	VGSW	3	GA2 OUTPUT SWING	-3.0		3.0	V	RL = 10kΩ
13	VOFFIN	1	ANALOG OFFSET INPUT	-500		500	mV	NOTE 1
14	VOFFG	3	GA2 OFFSET OUTPUT	-50		50	mV	NOTE 1
15	VOFFA	5	AOUT OFFSET OUTPUT	-50		50	mV	PCMIN = +0-CODE
16	CDOUT	15	PCMOUT CAPACITANCE			15.0	pF	at 1MHz Vbias = 0V
17	VOL	15	PCMOUT LOW VOLTAGE			0.4	V	RL= 500Ω +IOL= 0.8mA
18	VOH	15	PCMOUT HIGH VOLTAGE	VCC-0.3			V	IOH = -150µA
19	VIH	8,10,11 9,12,14	DIGITAL INPUT HIGH VOLTAGE	2.0			V	
20	VIL	8,10,11 9,12,14	DIGITAL INPUT LOW VOLTAGE			0.8	V	

NOTE 1) ANALOG INPUT AMPLIFIER GAIN = 0 dB (GA1 is connected to GA2)

2) DYNAMIC-CHARACTERISTICS
(VDD=5±0.25V, VSS=-5±0.25V,
VCC=5±0.25V, Ta=0-70°C)

No.	SYM.	DESCRIPTIONS	SPECIFICATIONS				NOTE
			MIN	TYP	MAX	UNIT	
1	FS	SYNCHRONIZATION RATE		8		kHz	
2	FC	PCM BIT CLOCK RATE		1536/ 1544/ 2048		kHz	
3	twc	CLOCK PULSE WIDTH	200			ns	
4	twSH	SYNC PULSE HIGH WIDTH	200			ns	
5	twSL	SYNC PULSE LOW WIDTH	8			μs	
6	tr	LOGIC INPUT RISE TIME	5		50	ns	
7	tf	LOGIC INPUT FALL TIME	5		50	ns	
8	t_{BCS}	PREVIOUS CLOCK TO SYNC DELAY	40			ns	NOTE 1
9	tcs	CLOCK TO SYNC DELAY			100	ns	NOTE 1,3
10	tcdl	CLOCK TO PCM MSB DELAY			170	ns	NOTE 1,2,4
11	tsd	SYNC TO PCM MSB DELAY			170	ns	NOTE 1,2,4
12	tcd	CLOCK TO PCMOUT DELAY			180	ns	NOTE 1,2,5
13	tsu	PCMIN SETUP TIME	65			ns	NOTE 1
14	thd	PCMIN HOLD TIME	120			ns	NOTE 1

NOTE 1) tr,tf of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT LOAD CONDITION: 500Ω + 165pF+ two LS-TTL Equivalent (IIL=0.8mA, IIH=-150μA) Threshold Level (VOH = 2.4V,VOL = 0.4V)
3) Positive value shows SYNC delay from CLOCK.
4) tcdl, tsd are specified by CLOCK or SYNC which has slower rise time.
5) tcd specification is valid for the data except MSB.

3) SYSTEM RELATED CHARACTERISTICS
(VDD=5±0.25V, VSS=-5±0.25V, VCC=5±0.25V, Ta=0-70°C,
INPUT AMPLIFIER GAIN = 0dB
GA2 LOAD = 10KΩ , AOUT LOAD = 600Ω, Synchronous operation. FC (PCM BIT CLOCK) = 2048 kHz)

3-1 FOR HD44233C

NO	SYM.	DESCRIPTIONS	TEST CONDITIONS		SPECIFICATIONS				NOTE
					MIN	TYP	MAX	UNIT	
1	SDA	Signal to Dist. (A to A)	820Hz tone	-45dBm0	25			dB	p-wgt
				-40	30			dB	
				-30 to +3	35			dB	
2	SNA	Signal to Dist. (A to A)	Noise	-55dBm0	14			dB	
				-40	29			dB	
				-34	34			dB	
				-27 to -6	36			dB	
				-3	28			dB	

to be continued

(con'd)

No	SYM.	DESCRIPTION	TEST CONDITIONS		SPECIFICATIONS				NOTE
					MIN	TYP	MAX	UNIT	
3	SDX	Signal to Dist. (A to D)	820Hz tone	-45dBm0	26			dB	p-wgt
				-40	31			dB	
				-30 to +3	36			dB	
4	SNX	Signal to Dist. (A to D)	Noise	-55dBm0	15			dB	
				-40	30			dB	
				-34	35			dB	
				-27 to -6	37			dB	
5	SDR	Signal to Dist. (D to A)	820Hz tone	-45dBm0	26			dB	p-wgt
				-40	31			dB	
				-30 to +3	36			dB	
6	SNR	Signal to Dist. (D to A)	Noise	-55dBm0	15			dB	
				-40	30			dB	
				-34	35			dB	
				-27 to -6	37			dB	
7	GTA	Gain Track. (A to A)	820Hz tone	-55 to -50dBm0	-1.0		1.0	dB	
			Relative to -10dBm0	-50to-40	-0.5		0.5	dB	
				-40 to +3	-0.3		0.3	dB	
8	GNA	Gain Track. (A to A)	Noise Relative to -10dBm0	-60 to -55dBm0	-0.8		0.8	dB	
				-55 to -10	-0.4		0.4	dB	
9	GTX	Gain Track. (A to D)	820Hz tone	-55to-50	-0.8		0.8	dB	
			Relative to -10dBm0	-50to-40	-0.4		0.4	dB	
				-40 to +3 dBm0	-0.2		0.2	dB	
10	GNX	Gain Track (A to D)	Noise	-60 to -55dBm0	-0.6		0.6	dB	
			Relative to -10dBm0	-55 to -40	-0.4		0.4	dB	
				-40 to -10	-0.2		0.2	dB	
11	GTR	Gain Track (D to A)	820Hz tone	-55to-50	-0.8		0.8	dB	
			Relative to -10dBm0	-50to-40	-0.4		0.4	dB	
				-40 to +3 dBm0	-0.2		0.2	dB	
12	GNR	Gain Track (D to A)	Noise	-60 to -55dBm0	-0.4		0.4	dB	
			Relative to -10dBm0	-55 to -10	-0.2		0.2	dB	

(to be continued)

(con'd)

No	SYM.	DESCRIPTION	TEST CONDITIONS		SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE
13	FRX	Freq.Response. (A to D) (Loss)	Relative to 820Hz 0dBm0	0.06kHz	24			dB	
				0.2	0		2.0		
				0.3 to 3	-0.15		0.15		
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				
14	FRR	Freq.Response. (D to A) (Loss)	Relative to 820Hz 0dBm0	0 to 3 kHz	-0.15		0.15	dB	
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				
15	AIL	Analog Input Level	820Hz 0dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
16	AOL	Analog Output Level	820Hz 0dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
17	ICNA	Idle Ch. Noise	A to A	AIN=AGND			-78	dBmOP	
18	ICNX	Idle Ch. Noise	A to D	AIN=AGND			-80	dBmOP	
19	ICNR	Idle Ch. Noise	D to A	PCMIN= +0-CODE			-81	dBmOP	
20	XTKA	AIN to AOUT Crosstalk	820Hz	0dBm0			-65	dB	
21	XTKD	PCMIN to PCMOUT	820Hz	0dBm0			-65	dB	

3-2. FOR HD44234C

NO	SYM.	DESCRIPTIONS	TEST CONDITIONS		SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE
1	SDA	Signal to Dist. (A to A)	1020Hztone	-45dBm0	25			dB	c-wgt
				-40	30			dB	
				-30 to +3	35			dB	
2	SDX	Signal to Dist. (A to D)	1020Hztone	-45dBm0	26			dB	c-wgt
				-40	31			dB	
				-30 to +3	36			dB	
3	SDR	Signal to Dist. (D to A)	1020Hztone	-45dBm0	26			dB	c-wgt
				-40	31			dB	
				-30 to +3	36			dB	
4	GTA	Gain Tracking (A to A)	1020Hztone Relative to -10dBm0	-55 to -50dBm0	-1.0		1.0	dB	
				-50to-40	-0.5		0.5	dB	
				-40 to +3	-0.3		0.3	dB	
5	GTX	Gain Tracking (A to D)	1020Hztone Relative to -10dBm0	-55to-50	-0.8		0.8	dB	
				-50to-40	-0.4		0.4	dB	
				-40 to +3 dBm0	-0.2		0.2	dB	
6	GTR	Gain Tracking (D to A)	1020Hztone Relative to -10dBm0	-55to-50	-0.8		0.8	dB	
				-50to-40	-0.4		0.4	dB	
				-40 to +3 dBm0	-0.2		0.2	dB	
7	FRX	Freq.Response. (A to D) (Loss)	Relative to 1020Hz 0dBm0	0.06kHz	24			dB	
				0.2	0		2.0		
				0.3 to 3	-0.15		0.15		
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				

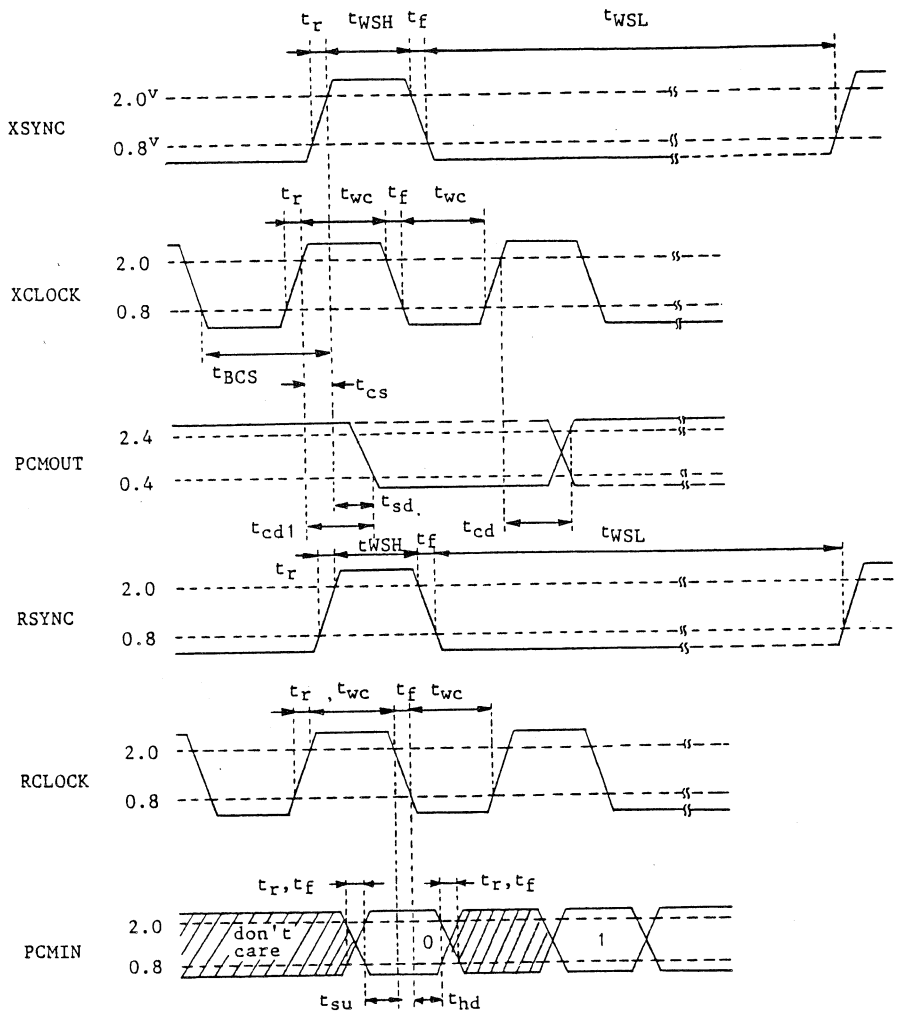
8	FRR	Freq.Response. (D to A) (Loss)	Relative to 1020Hz 0dBm0	0 to 3 kHz	-0.15		0.15	dB	
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				
9	AIL	Analog Input Level	1020Hz 0dBm0	25°C nom.P.S.	1.213	1.227	1.241	Vrms	
10	AOL	Analog Output Level	1020Hz 0dBm0	25°C nom.P.S.	1.213	1.227	1.241	Vrms	
11	ICNA	Idle Ch. Noise	A to A	AIN=AGND			15	dBrnC0	
12	ICNX	Idle Ch. Noise	A to D	AIN=AGND			14	dBrnC0	
13	ICNR	Idle Ch. Noise	D to A	PCMIN= +0-CODE			9	dBrnC0	
14	XTKA	AIN to AOUT Crosstalk	1020Hz 0dBm0				-65	dB	
15	XTKD	PCMIN to PCMOUT	1020Hz 0dBm0				-65	dB	

3-3. FOR HD44233C, HD44234C

No	Sym.	DESCRIPTION	TEST CONDITIONS		SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE
1	AT	AIL,AOL Variation with temp.	Relative to 25°C nominal P.S.			±20		ppm/°C	
2	AP	AIL,AOL Variation with P.S.	25°C, Supplies±5%			±0.01		dB	
3	ALS	GAIN Variation over Temp. P.S.	A to D D to A	INITIAL	-0.2		0.2	dB	Note1)
4	AIP	Peak Analog Input			3.0			V	
5	AOP	Peak Analog Output			2.5			V	
6	PDL	Propagation Delay	A to A	0dBm0		450	480	μs	
7	DD	Delay Distortion	A to A 0dBm0	0.5 to 0.6kHz			1.4	ms	rel. to min. delay
				0.6 to 1.0			0.7		
				1.0 to 2.6			0.2		
				2.6 to 2.8			1.4		
8	PSRR	PSRR	A to A AIN= AGND 0.3 -50kHz	VDD Mod. = +5V+100mVop	30			dB	
				Vss Mod. = -5V+100mVop	30				
9	IM1	Intermodulation	A to A(2a-b) a;0.47kHz,-4dBm0 b;0.32, -4				-38	dB	
10	IM2	Intermodulation	A to A(a-b) a;1.02kHz,-4dBm0 b;0.05, -23				-52	dB	
11	ICS	Single Freq.Noise	A to A AIN=AGND	8,16,24, 32,40kHz			-50	dBm0	
12	DIS	Discrimination	A to A 0dBm0	4.6 to 200kHz	30			dB	

Note 1) Total variation of GAIN including the initial fluctuation temperature variation and power supply dependence (0 - 70°C, VDD/Vss = ±5V±5%)

Timing Chart



Single Chip CODEC with Filters (COMBO)

FEATURES

- o SINGLE CHIP CMOS CODEC WITH FILTER IN 16-pins DIL PACKAGE
- o POWER SUPPLY VOLTAGE ± 5V±5%, LOW POWER DISSIPATION (50mW typ.)
- o FOLLOWS A-LAW (HD44237C) / μ-law HD44238C)
- o EXCEEDS CCITT AND D4 SPECIFICATIONS
- o SYNCHRONOUS / ASYNCHRONOUS OPERATION
- o INTERNAL CLOCK GENERATOR OPERATION FOR 64kHz to 2048kHz PCM RATE AS PLL CIRCUIT
- o ANTI-ALIASING FILTER (2nd order CR Active Filter)
- o VOLTAGE REFERENCE (INTERNAL-TRIMMED)
- o INPUT AMPLIFIER WITH UNCOMITTED PLUS/MINUS TERMINALS
- o AUTO-ZERO CANCEL CIRCUIT WITHOUT EXTERNAL COMPONENT

PIN CONFIGURATION

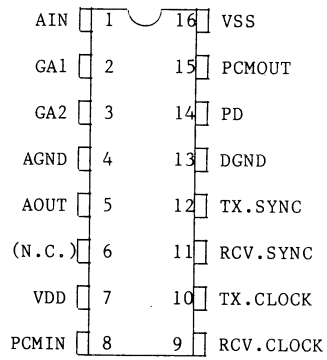


Fig.1 PIN ASSIGNMENT

(top view)

Table 1. PIN DESCRIPTIONS

HD44237C HD44238C		FUNCTION	REMARKS
No.	SYMBOL		
1	AIN	ANALOG INPUT	
2	GA1	GAIN ADJUST1	FEED-BACK INPUT
3	GA2	GAIN ADJUST2	10kΩ≤RL CL≤100pF
4	AGND	ANALOG GROUND	
5	AOUT	ANALOG OUTPUT	RL≥600Ω, CL≤100pF
6	N.C.		OPEN
7	VDD	POSITIVE POW. SUP.	5V±5%
8	PCMIN	PCM DATA INPUT	(TTL)
9	RCV.CLK	PCM BIT CLOCK	(TTL) 64 to 2048kHz
10	TX.CLK		
11	RCV.SYNC	SYNCHRONIZATION	(TTL) 8kHz
12	TX.SYNC		
13	DGND	DIGITAL GROUND	
14	PD	POWER DOWN	(TTL) "0" = down
15	PCMOUT	PCM DATA OUTPUT	OPEN DRAIN
16	VSS	NEGATIVE POW.SUP.	-5V±5%

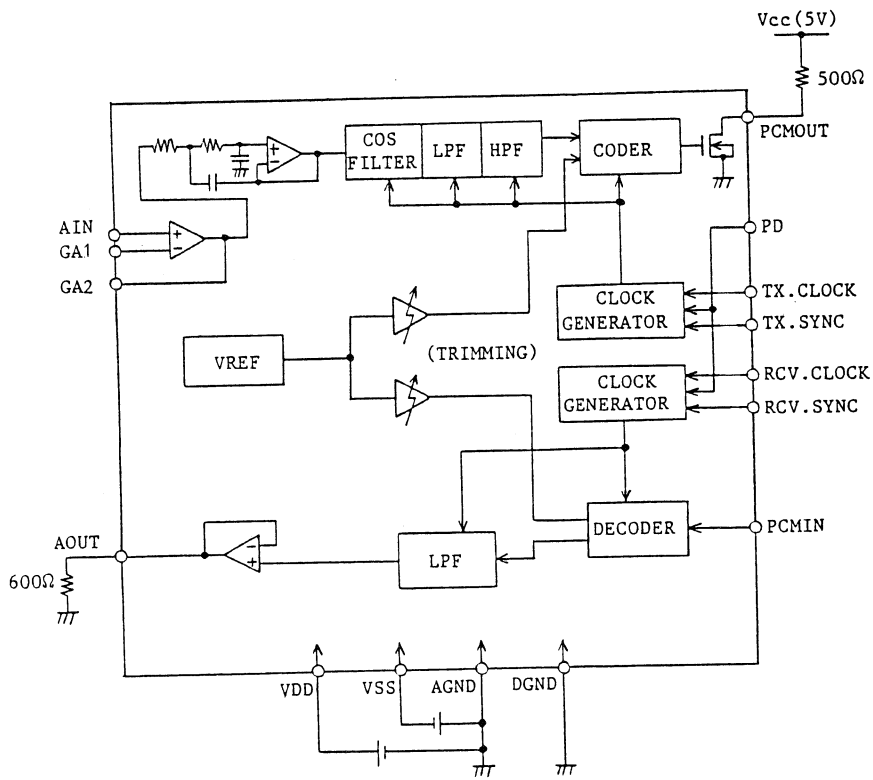


Fig.2 BLOCK DIAGRAM

■ GENERAL DESCRIPTION

The HD44237C, HD44238C are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band limiting filters and the analog/digital conversion circuits that conform to the A-Law or μ-Law companding characteristic.

HD44237C is A-Law. HD44238C is μ-Law.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of $\pm$ 5V.

For a sampling rate of 8kHz, PCM input/output data rate can be selected from 64kHz to 2048kHz in synchronous or asynchronous operation. Internal PLL circuits generate the internal clock from the 8kHz synchronization clock.

■ FUNCTIONAL DESCRIPTION

Figure 2 shows the simplified block diagram of the HD44237C, HD44238C. The devices contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. The relationship between the PCM data word and the audio signal is defined just same as CCITT G711 Table 1 for HD44237C, Table 2 for HD44238C respectively. A band-gap voltage generator supplies the reference level for the conversion process. 2nd Order CR Active Filter is implemented on chip to avoid the aliasing noise which is caused by the clock of transmit filter.

1) TRANSMIT SECTION

Input analog signals first enter the chip at the uncommitted amplifier terminals. This op amp allows gain trim to be used if desired to set the 0dB or 0 level in the system. This amplifier also operates as the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 32dB (typ) at 256kHz and 40dB (typ) at 512kHz, the "effective" clock frequency of the following switched-capacitor Cosine Filter. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 128kHz, followed by a 3rd Order High-Pass Filter clocked at 8kHz. The resulting band-pass characteristics meet the CCITT, G.712 specifications. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The 8-bit PCM data is clocked out by the shift clock at one of 64kHz to 2048kHz. A auto-zero loop (without any external capacitor) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

An additional feature of the HD44237C is a signbit fixation circuit to reduce the idle channel noise during quiet periods. It is of particular importance because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

2) RECEIVE SECTION

A shift clock, from 64kHz to 2048kHz, clock the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 128kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic or transformer directly as long as the impedance is greater than 600Ω.

3) COMPANDING LAW

The encoding and decoding characteristics of the Codecs comply with the requirements of CCITT G711 table 1 or Table 2, corresponding to their comparing law. The even bits of PCM words are inverted for A-Law devices. Positive logic is used (the High level corresponds to '1').

4) POWER DOWN LOGIC

Powering down the CODEC can be done in several ways. The most direct method is to drive the PD pin to a low level. Stopping SYNC input will also put the chip into the stand-by mode. The SYNC input can be held high, low or disconnected. After the chip being activated by these functions, the PCMOUT is in high impedance state and the AOUT is connected to AGND for about 1 msec to avoid the power-on noise.

5) VOLTAGE REFERENCE CIRCUIT

A temperature compensated band-gap voltage generator provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply it to the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed to ensure a minimum gain error of $\pm$ 0.1 dB at the nominal power supply voltage and the room temperature.

6)TIMING REQUIREMENTS

The CODECS do not require that the 8kHz transmit and receive sampling strobes should be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe. The PCM output goes into a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and shift clock is synchronized to it. The clock rate can be selected from 64kHz to 2048kHz.

7)SYSTEM CLOCK

The basic timing of the Codecs is provided by the internally generated clock from synchronization. The internal PLL (Phase Locked Loop) circuits generate 128kHz clocks. These features make it possible that the clock rate of PCM bit shifting may be free in the range from 64kHz to 2.048MHz.

8)BIT STEAL CONTROL (HD44238C only)

For the bit steal period, the decoder output of μ-law CODEC should be shifted as half-bit of steps. For the CODECs, the power down control pin provides this function. If the low state of PD pin is less than 6 frames (0.75 msec), the device is not deactivated and the decoder output corresponding to the frame of the rising and falling edge of the pin is shifted as half-bit. And, if the low state is longer than 1.0 msec, the device is deactivated.

PIN/FUNCTION DESCRIPTIONS

PIN	NO	DESCRIPTIONS
TX.CLOCK RCV.CLOCK	9 10	Any of 64kHz to 2.048 MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the SYNC, TX.SYNC/RCV.SYNC respectively.
TX.SYNC RCV.SYNC	11 12	These TTL compatible pulse inputs (typ.8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the CLOCK, TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the CLOCK, TX.CLOCK/RCV.CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK,TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC,TX.SYNC/RCV.SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500Ω pull-up per 8 Codecs is required.
PCMIN	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of CLOCK, RCV.CLOCK.
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of -VREF to +VREF to the device. The input stage can be connected as a unity gain amplfier, amplifier with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10kΩ or directly connected to GA1. GA1 is the negative feed back input of the amplifier. CL should be less than 100 pF.
AOUT	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 ohms. CL should be less than 100 pF.
VDD VSS AGND DGND	7 16 4 13	These are power supply pins. VDD and VSS are positive and negative supply pins respectively (typ. +5V, -5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	When this TTL compatible input is held low, the chip is put into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect. This pin should be pulled-up to VDD to keep the device active or to control ON/OFF with strobes. For the μ-law devices, this pin also provides the half-bit decoder shift for the bit-steal frame according to alternating the state of the input.

■ ABSOLUTE MAXIMUM RATING

No.	ITEM	RATING
1	VDD	-0.3 to +7V
2	VSS	+0.3 to -7V
3	STORAGE TEMPERATURE	-55°C to 125°C
4	POWER DISSIPATION	0.5W
5	DIGITAL INPUT/OUTPUT VOLTAGE	-0.3V<VIN<VDD+0.3
6	ANALOG INPUT/OUTPUT VOLTAGE	VSS-0.3V<VIN<VDD+0.3

■ ELECTRICAL CHARACTERISTICS

1) STATIC CHARACTERISTICS

(VDD = 5±0.25V, VSS = -5±0.25V, VCC = 5±0.25V, TA = 0-70°C)

No.	SYMBOL	PIN No.	DESCRIPTIONS	SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE/ CONDITIONS
1	IDD	7	VDD CURRENT(OPE.)		5.5	10	mA	NOTE 1
2	ISS	16	VSS CURRENT(OPE.)	-10	-4.5			AIN=0V
3	IDDST	7	VDD CURRENT(St.By.)		0.3	1		PCMIN = +0 CODE
4	ISSST	16	VSS CURRENT(St.By.)	-0.2				RL(GA2)= 10kΩ RL(AOUT) =600Ω
5	IL	1,2,8 9,10 14	LEAK CURRENT	-10.0		10.0	µA	VM=0.8V
				-10.0		10.0	µA	VM=2.0V
						10.0	µA	VDD=VM=5.25V
6	IPL	11,12	PULL UP CURRENT	-100		0	µA	
7	IDL	15	LEAK CURRENT			10.0	µA	VDD=VM=5.25V
8	CAIN2	1,2	ANALOG INPUT CAP.			10	pF	at 1MHz Vbias = 0V
9	CDIN	8,9 10,11 12,14	INPUT CAPACITANCE			10	pF	at 1MHz Vbias = 0V
10	ROUTA	5	AOUT RESISTANCE		1	10	Ω	
11	ROUTG	3	GA2 RESISTANCE			30	Ω	NOTE 1
12	VGSW	3	GA2 OUTPUT SWING	-3.0		3.0	V	RL = 10kΩ
13	VOFFIN	1	ANALOG OFFSET INPUT	-500		500	mV	NOTE 1
14	VOFFG	3	GA2 OFFSET OUTPUT	-50		50	mV	NOTE 1
15	VOFFA	5	AOUT OFFSET OUTPUT	-50		50	mV	PCMIN = +0-CODE
16	CDOUT	15	PCMOUT CAPACITANCE			15.0	pF	at 1MHz Vbias = 0V
17	VOL	15	PCMOUT LOW VOLTAGE			0.4	V	RL= 500Ω +IOL=0.8mA
18	VOH	15	PCMOUT HIGH VOLTAGE	VCC-0.3			V	IOH= -150 µA
19	VIH	8,10,11 9,12,14	DIGITAL INPUT HIGH VOLTAGE	2.0			V	
20	VIL	8,10,11 9,12,14	DIGITAL INPUT LOW VOLTAGE			0.8	V	

NOTE 1) ANALOG INPUT AMPLIFIER GAIN = 0 dB (GA1 is connected to GA2)

2) DYNAMIC-CHARACTERISTICS
(VDD=5±0.25V, VSS=-5±0.25V,
VCC=5±0.25V, Ta=0-70°C)

No.	SYM.	DESCRIPTIONS	SPECIFICATIONS				NOTE
			MIN	TYP	MAX	UNIT	
1	FS	SYNCHRONIZATION RATE		8		kHz	
2	FC	PCM BIT CLOCK RATE	64		2048	kHz	
3	twc	CLOCK PULSE WIDTH	200			ns	
4	twSH	SYNC PULSE HIGH WIDTH	200			ns	
5	twSL	SYNC PULSE LOW WIDTH	8			µs	
6	tr	LOGIC INPUT RISE TIME	5		50	ns	
7	tf	LOGIC INPUT FALL TIME	5		50	ns	
8	t_{BCS}	PREVIOUS CLOCK TO SYNC DELAY	40			ns	NOTE 1
9	tcs	CLOCK TO SYNC DELAY			100	ns	NOTE 1,3
10	tcdl	CLOCK TO PCM MSB DELAY			170	ns	NOTE 1,2,4
11	tsd	SYNC TO PCM MSB DELAY			170	ns	NOTE 1,2,4
12	tcd	CLOCK TO PCMOUT DELAY			180	ns	NOTE 1,2,5
13	tsu	PCMIN SETUP TIME	65			ns	NOTE 1
14	thd	PCMIN HOLD TIME	120			ns	NOTE 1
15	tbs	PD(bit-steal) SETUP	200			ns	NOTE 1,6
16	tbh	PD(bit-steal) HOLD	200			ns	NOTE 1,6

NOTE 1) tr,tf of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT LOAD CONDITION: 500Ω + 165pF+ two LS-TTL Equivalent (IIL=0.8mA, IIH=-150µA) Threshold Level (VOH = 2.4V,VOL = 0.4V)
3) Positive value shows SYNC delay from CLOCK.
4) tcdl, tsd are specified by CLOCK or SYNC which has slower rise time.
5) tcd specification is valid for the data except MSB.
6) Applicable HD44238C

3) SYSTEM RELATED CHARACTERISTICS
(VDD=5±0.25V, VSS=-5±0.25V, VCC=5±0.25V, Ta=0-70°C,
INPUT AMPLIFIER GAIN = 0dB,
GA2 LOAD = 10KΩ , AOUT LOAD = 600Ω, Synchronous operation. FC (PCM BIT CLOCK) = 2048 kHz)

3-1 FOR HD44237C

NO	SYM.	DESCRIPTIONS	TEST CONDITIONS		SPECIFICATIONS				NOTE
					MIN	TYP	MAX	UNIT	
1	SDA	Signal to Dist. (A to A)	820Hz tone	-45dBm0	25			dB	p-wgt
				-40	30			dB	
				-30 to +3	35			dB	
2	SNA	Signal to Dist. (A to A)	Noise	-55dBm0	14			dB	
				-40	29			dB	
				-34	34			dB	
				-27 to -6	36			dB	
				-3	28			dB	

to be continued

(con'd)

No	SYM.	DESCRIPTION	TEST CONDITIONS		SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE
3	SDX	Signal to Dist. (A to D)	820Hz tone	-45dBm0	26			dB	p-wgt
				-40	31			dB	
				-30 to +3	36			dB	
4	SNX	Signal to Dist. (A to D)	Noise	-55dBm0	15			dB	
				-40	30			dB	
				-34	35			dB	
				-27 to -6	37			dB	
5	SDR	Signal to Dist. (D to A)	820Hz tone	-45dBm0	26			dB	p-wgt
				-40	31			dB	
				-30 to +3	36			dB	
6	SNR	Signal to Dist. (D to A)	Noise	-55dBm0	15			dB	
				-40	30			dB	
				-34	35			dB	
				-27 to -6	37			dB	
7	GTA	Gain Track. (A to A)	820Hz tone	-55 to -50dBm0	-1.0		1.0	dB	
			Relative to -10dBm0	-50to-40	-0.5		0.5	dB	
				-40 to +3	-0.3		0.3	dB	
8	GNA	Gain Track. (A to A)	Noise Relative to -10dBm0	-60 to -55dBm0	-0.8		0.8	dB	
				-55 to -10	-0.4		0.4	dB	
9	GTX	Gain Track. (A to D)	820Hz tone	-55to-50	-0.8		0.8	dB	
			Relative	-50to-40	-0.4		0.4	dB	
			to -10dBm0	-40 to +3 dBm0	-0.2		0.2	dB	
10	GNX	Gain Track (A to D)	Noise	-60 to -55dBm0	-0.6		0.6	dB	
			Relative to -10dBm0	-55 to -40	-0.4		0.4	dB	
				-40 to -10	-0.2		0.2	dB	
11	GTR	Gain Track (D to A)	820Hz tone	-55to-50	-0.8		0.8	dB	
			Relative	-50to-40	-0.4		0.4	dB	
			to -10dBm0	-40 to +3 dBm0	-0.2		0.2	dB	
12	GNR	Gain Track (D to A)	Noise Relative to -10dBm0	-60 to -55dBm0	-0.4		0.4	dB	
				-55 to -10	-0.2		0.2	dB	

(to be continued)

(con'd)

NO	SYM.	DESCRIPTIONS	TEST CONDITIONS		SPECIFICATIONS				NOTE
					MIN	TYP	MAX	UNIT	
13	FRX	Freq.Response. (A to D) (Loss)	Relative to 820Hz 0dBm0	0.06kHz	24			dB	
				0.2	0		2.0		
				0.3 to 3	-0.15		0.15		
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				
14	FRR	Freq.Response. (D to A) (Loss)	Relative to 820Hz 0dBm0	0 to 3 kHz	-0.15		0.15	dB	
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				
15	AIL	Analog Input Level	820Hz 0dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
16	AOL	Analog Output Level	820Hz 0dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
17	ICNA	Idle Ch. Noise	A to A	AIN=AGND			-78	dBmOP	
18	ICNX	Idle Ch. Noise	A to D	AIN=AGND			-80	dBmOP	
19	ICNR	Idle Ch. Noise	D to A	PCMIN= +0-CODE			-80	dBmOP	
20	XTKA	AIN to AOUT Crosstalk	820Hz	0dBm0			-65	dB	
21	XTKD	PCMIN to PCMOUT	820Hz	0dBm0			-65	dB	

3-2. FOR HD44238C

NO	SYM.	DESCRIPTIONS	TEST CONDITIONS		SPECIFICATIONS				NOTE
					MIN	TYP	MAX	UNIT	
1	SDA	Signal to Dist. (A to A)	1020Hztone	-45dBm0	25			dB	c-wgt
				-40	30			dB	
				-30 to +3	35			dB	
2	SDX	Signal to Dist. (A to D)	1020Hztone	-45dBm0	26			dB	c-wgt
				-40	31			dB	
				-30 to +3	36			dB	
3	SDR	Signal to Dist. (D to A)	1020Hztone	-45dBm0	26			dB	c-wgt
				-40	31			dB	
				-30 to +3	36			dB	
4	GTA	Gain Tracking (A to A)	1020Hztone	-55 to -50dBm0	-1.0		1.0	dB	
			Relative to -10dBm0	-50to-40	-0.5		0.5	dB	
				-40 to +3	-0.3		0.3	dB	
5	GTX	Gain Tracking (A to D)	1020Hztone	-55to-50	-0.8		0.8	dB	
			Relative	-50to-40	-0.4		0.4	dB	
			to -10dBm0	-40 to +3 dBm0	-0.2		0.2	dB	
6	GTR	Gain Tracking (D to A)	1020Hztone	-55to-50	-0.8		0.8	dB	
			Relative	-50to-40	-0.4		0.4	dB	
			to -10dBm0	-40 to +3 dBm0	-0.2		0.2	dB	
7	FRX	Freq.Response. (A to D) (Loss)	Relative to 1020Hz 0dBm0	0.06kHz	24			dB	
				0.2	0		2.0		
				0.3 to 3	-0.15		0.15		
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				

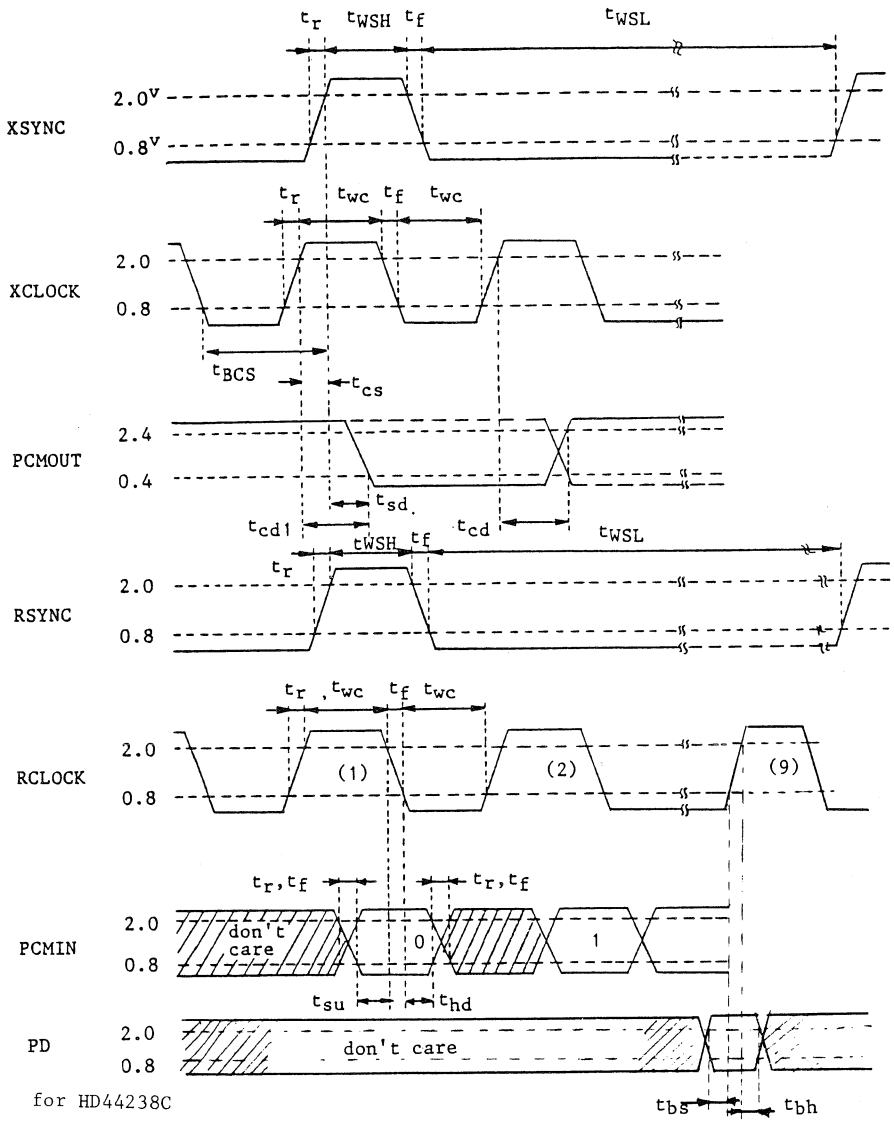
8	FRR	Freq.Response. (D to A) (Loss)	Relative to 1020Hz 0dBm0	0 to 3 kHz	-0.15		0.15	dB	
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				
9	AIL	Analog Input Level	1020Hz 0dBm0	25°C nom.P.S.	1.213	1.227	1.241	Vrms	
10	AOL	Analog Output Level	1020Hz 0dBm0	25°C nom.P.S.	1.213	1.227	1.241	Vrms	
11	ICNA	Idle Ch. Noise	A to A	AIN=AGND			16	dBrnC0	
12	ICNX	Idle Ch. Noise	A to D	AIN=AGND			16	dBrnC0	
13	ICNR	Idle Ch. Noise	D to A	PCMIN= +0-CODE			10	dBrnC0	
14	XTKA	AIN to AOUT Crosstalk	1020Hz 0dBm0				-65	dB	
15	XTKD	PCMIN to PCMOUT	1020Hz 0dBm0				-65	dB	

3-3. FOR HD44237C, HD44238C

No	Sym.	DESCRIPTION	TEST CONDITIONS		SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE
1	AT	AIL,AOL Variation with temp.	Relative to 25°C nominal P.S.			±20		ppm/°C	
2	AP	AIL,AOL Variation with P.S.	25°C, Supplies±5%			±0.01		dB	
3	ALS	GAIN Variation over Temp. P.S.	A to D D to A	INITIAL	-0.2		0.2	dB	Note1)
4	AIP	Peak Analog Input			3.0			V	
5	AOP	Peak Analog Output			2.5			V	
6	PDL	Propagation Delay	A to A	0dBm0		450	480	μs	
7	DD	Delay Distortion	A to A 0dBm0	0.5 to 0.6kHz			1.4	ms	rel. to min. delay
				0.6 to 1.0			0.7		
				1.0 to 2.6			0.2		
				2.6 to 2.8			1.4		
8	PSRR	PSRR	A to A AIN= AGND	Vdd Mod. =+5V+100mVop	30			dB	
			0.3-50kHz	Vss Mod. =-5V+100mVop	30				
9	IM1	Intermodulation	A to A(2a-b) a;0.47kHz,-4dBm0 b;0.32, -4				-38	dB	
10	IM2	Intermodulation	A to A(a-b) a;1.02kHz,-4dBm0 b;0.05, -23				-52	dB	
11	ICS	Single Freq.Noise	A to A AIN=AGND	8,16,24, 32,40kHz			-50	dBm0	
12	DIS	Discrimination	A to A 0dBm0	4.6 to 200kHz	30			dB	

Note 1) Total variation of GAIN including the initial fluctuation temperature variation and power supply dependence (0 - 70°C, Vdd/Vss=±5V±5%)

Timing Chart



Single Chip CODEC with Filters (COMBO)

FEATURES

- o SINGLE CHIP CMOS CODEC WITH FILTER IN 16-pins DIL PACKAGE
- o POWER SUPPLY VOLTAGE ± 5V±5%, LOW POWER DISSIPATION
- o FOLLOWS μ-LAW (HD44248C) OR A-LAW (HD44247C)
- o EXCEEDS CCITT AND D4 SPECIFICATIONS
- o ASYNCHRONOUS AND SYNCHRONOUS OPERATION
- o INTERNAL CLOCK GENERATOR FOR 64 kHz TO 2048 kHz PCM RATE AS PLL CIRCUIT.
- o ANTI-ALIASING FILTER (2nd order CR Active Filter)
- o VOLTAGE REFERENCE (INTERNAL-TRIMMED)
- o INPUT AMPLIFIER WITH UNCOMMITTED PLUS/MINUS TERMINALS
- o AUTO-ZERO CANCEL CIRCUIT WITHOUT EXTERNAL COMPONENT
- o PUSH/PULL ANALOG OUTPUT

PIN CONFIGURATION

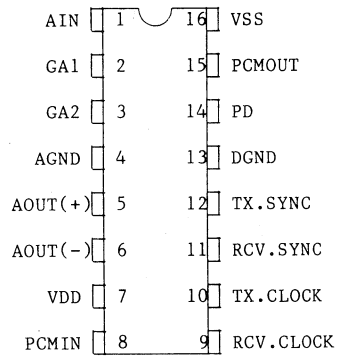


Fig.1 PIN ASSIGNMENT

(top view)

Table 1. PIN DESCRIPTIONS

NO.	SYMBOL	FUNCTION	REMARKS
1	AIN	ANALOG INPUT	
2	GA1	GAIN ADJUST1	FEED-BACK INPUT
3	GA2	GAIN ADJUST2	10kΩ≤RL CL≤100pF
4	AGND	ANALOG GROUND	
5	AOUT(+)	ANALOG OUTPUT	RL≥600Ω, CL≤100pF
6	AOUT(-)		RL≥600Ω, CL≤100pF
7	VDD	POSITIVE POW. SUP.	5V±5%
8	PCMIN	PCM DATA INPUT	(TTL)
9	RCV.CLK	PCM BIT CLOCK	(TTL)64kHz to 2048kHz
10	TX.CLK		
11	RCV.SYNC	SYNCHRONIZATION	(TTL) 8kHz
12	TX.SYNC		
13	DGND	DIGITAL GROUND	
14	PD	POWER DOWN	(TTL) "0" = down
15	PCMOUT	PCM DATA OUTPUT	OPEN DRAIN
16	VSS	NEGATIVE POW.SUP.	-5V±5%

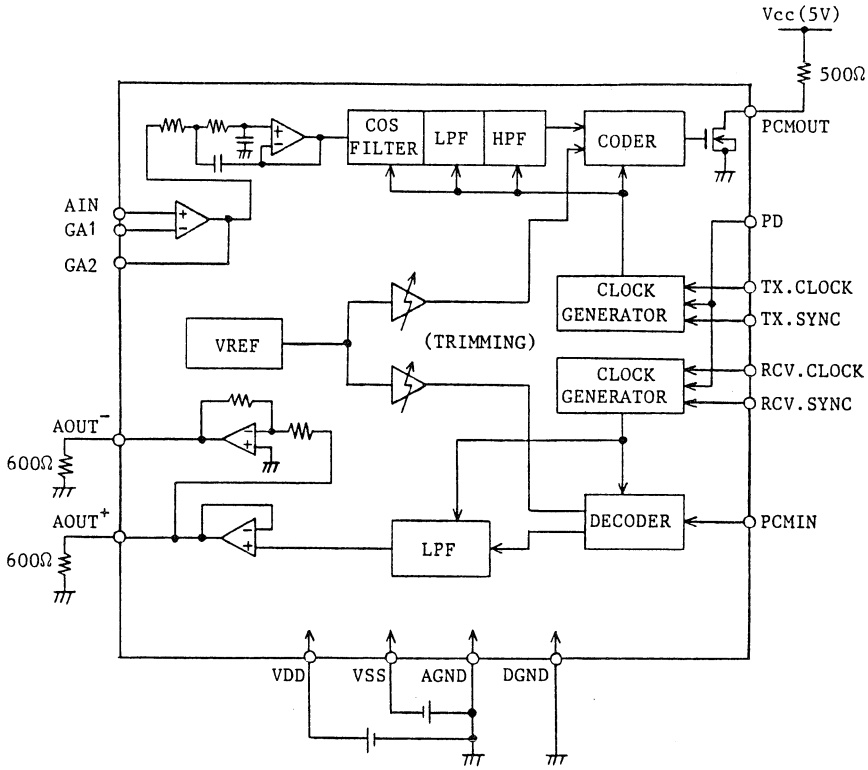


Fig.2 BLOCK DIAGRAM

GENERAL DESCRIPTION

The HD44247C and HD44248C are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band limiting filters and the analog/digital conversion circuits that conform to the A-Law or μ-Law companding characteristic.

HD44247C is A-Law device and HD44248C is μ-Law device.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ± 5V.

For a sampling rate of 8kHz, PCM input/output data rate can be selected from 64kHz to 2048kHz in synchronous or asynchronous operation. The inverted analog output is provided for the balanced transformer interface.

FUNCTIONAL DESCRIPTION

Figure 2 shows the simplified block diagram of the HD44247C and HD44248C. The devices contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. The relationship between the PCM data word and the audio signal is defined just same as CCITT G711 Table 1 for HD44247C, Table 2 for HD44248C respectively. A band-gap voltage generator supplies the reference level for the conversion process. 2nd Order CR Active Filter is implemented on chip to avoid the aliasing noise which is caused by the clock of transmit filter.

1) TRANSMIT SECTION

Input analog signals first enter the chip at the uncommitted amplifier terminals. This op amp allows gain trim to be used if desired to set the 0dB or 0 level in the system. This amplifier also operates as the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 32dB (typ) at 256kHz and 40dB (typ) at 512kHz, the "effective" clock frequency of the following switched-capacitor Cosine Filter. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 128kHz, followed by a 3rd Order High-Pass Filter clocked at 8kHz. The resulting band-pass characteristics meet the CCITT, G.712 specifications. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The 8-bit PCM data is clocked out by the shift clock at one of from 64kHz to 2048kHz. A auto-zero loop (without any external capacitor) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

An additional feature of the HD44247C is a signbit fixation circuit to reduce the idle channel noise during quiet periods. It is of particular importance because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

2) RECEIVE SECTION

A shift clock, from 64kHz to 2048kHz, clock the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 128kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic or transformer directly as long as the impedance is greater than 600Ω.

3) COMPANDING LAW

The encoding and decoding characteristics of the Codecs comply with the requirements of CCITT G711 Table 1 or Table 2, corresponding to their comparing law. The even bits of PCM words are inverted for A-Law devices. Positive logic is used (the High level corresponds to '1').

4) POWER DOWN LOGIC

Powering down the CODEC can be done in several ways. The most direct method is to drive the PD pin to a low level. Stopping SYNC input will also put the chip into the stand-by mode. The SYNC input can be held high, low or disconnected. After the chip being activated by these functions, the PCMOUT is in high impedance state and the AOUT is connected to AGND for about 1 msec to avoid the power-on noise.

5) VOLTAGE REFERENCE CIRCUIT

A temperature compensated band-gap voltage generator provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply it to the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed to ensure a minimum gain error of $\pm$ 0.1 dB at the nominal power supply voltage and the room temperature.

6)TIMING REQUIREMENTS

The CODECS do not require that the 8kHz transmit and receive sampling strobes should be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe. The PCM output goes into a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and shift clock is synchronized to it. The clock rate can be selected from 64 to 2048kHz.

7)SYSTEM CLOCK

The basic timing of the Codecs is provided by the internally generated clock form synchronization. The internal PLL (Phase Locked Loop) circuits generate 128kHz clocks. These features make it possible that the clock rate of PCM bit shifting may be free in the range from 64kHz to 2.048MHz.

8)BIT STEAL CONTROL (HD44248C only)

For the bit steal period, the decoder output of μ-law CODEC should be shifted as half-bit of steps. For the CODECs, the power down control pin provides this function. If the low state of PD pin is less than 6 frames (0.75 msec), the device is not deactivated and the decoder output corresponding to the frame of the rising and falling edge of the pin is shifted as half-bit. And, if the low state is longer than 1.0 msec, the device is deactivated.

9)PUSH-PULL ANALOG OUTPUT

The CODECs have the inverted output (AOUT-) of the buffered filters output of receive side (AOUT+). So, the CODECs can be interfaced directly to the balanced transformer to get the larger output level using the conventional power supply voltage ($\pm$5V).

PIN/FUNCTION DESCRIPTIONS

PIN	NO	DESCRIPTIONS
TX.CLOCK RCV.CLOCK	9 10	Any of 64kHz to 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX.SYNC/RCV.SYNC respectively.
TX.SYNC RCV.SYNC	11 12	These TTL compatible pulse inputs (typ.8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK/RCV.CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK,TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC,TX.SYNC/RCV.SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500Ω pull-up per 8 CODECs is required.
PCMIN	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV.CLOCK.
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of -VREF to +VREF to the device. The input stage can be connected as a unity gain amplfier, amplifier with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10kΩ or directly connected to GA1. GA1 is the negative feed back input of the amplifier. CL should be less than 100 pF.
AOUT(+)	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600Ω. CL should be less than 100 pF.
VDD VSS AGND DGND	7 16 4 13	These are power supply pins. VDD and VSS are positive and negative supply pins respectively (typ. +5V, -5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect. This pin should be pulled-up to VDD to keep the device active or to control ON/OFF with strobes. For the μ-Law devices, this pin also provides the half-bit decoder shift for the bit-steal frame according to alternating the state of the input.
AOUT(-)	6	This is the inverted output of pin 5 signal output to drive the 600Ω transformer as the push-pull operation. RL≥600Ω, CL≤100pF

■ ABSOLUTE MAXIMUM RATING

No.	ITEM	RATING
1	VDD	-0.3 to +7V
2	VSS	+0.3 to -7 V
3	STORAGE TEMPERATURE	-55°C to 125°C
4	POWER DISSIPATION	0.5W
5	DIGITAL INPUT/OUTPUT VOLTAGE	-0.3V<VIN<VDD+0.3
6	ANALOG INPUT/OUTPUT VOLTAGE	VSS-0.3V<VIN<VDD+0.3

■ ELECTRICAL CHARACTERISTICS

1) STATIC CHARACTERISTICS

(VDD = 5±0.25V, VSS = -5±0.25V, VCC = 5±0.25V, TA = 0-70°C)

No.	SYMBOL	PIN	DESCRIPTIONS	SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE/ CONDITIONS
1	IDD	7	VDD CURRENT(OPE.)		8.0	13.5	mA	NOTE 1 AIN = 0V PCMIN = +0 CODE RL(GA2)= 10kΩ RL(AOUT)= 600Ω
2	ISS	16	VSS CURRENT(OPE.)	-13.0	-7.5			
3	IDDST	7	VDD CURRENT(St.By.)		0.4	1.0		
4	ISSST	16	VSS CURRENT(St.By.)	-0.2				
5	IL	1,2,8 9,10 14	LEAK CURRENT	-10.0		10.0	µA	VM=0.8V
				-10.0		10.0	µA	VM=2.0V
						10.0	µA	VDD=VM=5.25V
6	IPL	11,12	PULL UP CURRENT	-100		0	µA	
7	IDL	15	LEAK CURRENT			10.0	µA	VDD=VM=5.25V
8	CAIN1	1	ANALOG INPUT CAP.			10	pF	at 1MHz Vbias = 0V
9	CAIN2	2	ANALOG INPUT CAP.			10	pF	at 1MHz Vbias = 0V
10	CDIN	8,9 10,11 12,14	INPUT CAPACITANCE			10	pF	at 1MHz Vbias = 0V
11	ROUTA	5,6	AOUT RESISTANCE		1	10	Ω	
12	ROUTG	3	GA2 RESISTANCE			30	Ω	NOTE 1
13	VGSW	3	GA2 OUTPUT SWING	-3.0		3.0	V	RL = 10kΩ
14	VOFFIN	1	ANALOG OFFSET INPUT	-500		500	mV	NOTE 1
15	VOFFG	3	GA2 OFFSET OUTPUT	-50		50	mV	NOTE 1
16	VOFFA	5,6	AOUT OFFSET OUTPUT	-50		50	mV	PCMIN = +0-CODE
17	CDOUT	15	PCMOUT CAPACITANCE			15.0	pF	at 1MHz Vbias = 0V
18	VOL	15	PCMOUT LOW VOLTAGE			0.4	V	RL= 500Ω +IOL = 0.8mA
19	VOH	15	PCMOUT HIGH VOLTAGE	VCC-0.3			V	IOH=-150µA
20	VIH	8,10,11 9,12,14	DIGITAL INPUT HIGH VOLTAGE	2.0			V	
21	VIL	8,10,11 9,12,14	DIGITAL INPUT LOW VOLTAGE			0.8	V	

NOTE 1) ANALOG INPUT AMPLIFIER GAIN = 0 dB (GA1 is connected to GA2)

2) DYNAMIC-CHARACTERISTICS
(VDD=5±0.25V, VSS=-5±0.25V,
VCC=5±0.25V, Ta=0-70°C)

No.	SYM.	DESCRIPTIONS	SPECIFICATIONS				NOTE
			MIN	TYP	MAX	UNIT	
1	FS	SYNCHRONIZATION RATE		8		kHz	
2	FC	PCM BIT CLOCK RATE	64		2048	kHz	
3	twc	CLOCK PULSE WIDTH	200			ns	
4	twSH	SYNC PULSE HIGH WIDTH	200			ns	
5	twSL	SYNC PULSE LOW WIDTH	8			μs	
6	tr	LOGIC INPUT RISE TIME	5		50	ns	
7	tf	LOGIC INPUT FALL TIME	5		50	ns	
8	t_{BCS}	PREVIOUS CLOCK TO SYNC DELAY	40			ns	NOTE 1
9	tcs	CLOCK TO SYNC DELAY			100	ns	NOTE 1,3
10	tcdl	CLOCK TO PCM MSB DELAY			170	ns	NOTE 1,2,4
11	tsd	SYNC TO PCM MSB DELAY			170	ns	NOTE 1,2,4
12	tcd	CLOCK TO PCMOUT DELAY			180	ns	NOTE 1,2,5
13	tsu	PCMIN SETUP TIME	65			ns	NOTE 1
14	thd	PCMIN HOLD TIME	120			ns	NOTE 1
15	tbs	PD(bit-steal)SETUP	200			ns	NOTE 1,6
16	tbh	PD(bit-steal)HOLD	200			ns	NOTE 1,6

NOTE 1) tr,tf of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT LOAD CONDITION: 500Ω + 165pF+ two LS-TTL Equivalent (IIL=0.8mA, IIH=-150μA) Threshold Level (VOH = 2.4V,VOL = 0.4V)
3) Positive value shows SYNC delay from CLOCK.
4) tcdl, tsd are specified by CLOCK or SYNC which has slower rise time.
5) tcd specification is valid for the data except MSB.
6) Applicable HD44248C

3) SYSTEM RELATED CHARACTERISTICS
(VDD=5±0.25V, VSS=-5±0.25V, VCC=5±0.25V, Ta=0-70°C,
INPUT AMPLIFIER GAIN = 0dB, ANALOG OUTPUT = AOUT(-),
GA2 LOAD = 10KΩ , AOUT LOAD = 600Ω, Synchronous
operation. FC (PCM BIT CLOCK) = 2048 kHz)

3-1 FOR HD44247C

NO	SYM.	DESCRIPTIONS	TEST CONDITIONS		SPECIFICATIONS				NOTE
					MIN	TYP	MAX	UNIT	
1	SDA	Signal to Dist. (A to A)	820Hz tone	-45dBm0	25			dB	p-wgt
				-40	30			dB	
				-30 to +3	35			dB	
2	SNA	Signal to Dist. (A to A)	Noise	-55dBm0	14			dB	
				-40	29			dB	
				-34	34			dB	
				-27 to -6	36			dB	
				-3	28			dB	

to be continued

(con'd)

No	SYM.	DESCRIPTION	TEST CONDITIONS		SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE
3	SDX	Signal to Dist. (A to D)	820Hz tone	-45dBm0	26			dB	p-wgt
				-40	31			dB	
				-30 to +3	36			dB	
4	SNX	Signal to Dist. (A to D)	Noise	-55dBm0	15			dB	
				-40	30			dB	
				-34	35			dB	
				-27 to -6	37			dB	
5	SDR	Signal to Dist. (D to A)	820Hz tone	-45dBm0	26			dB	p-wgt
				-40	31			dB	
				-30 to +3	36			dB	
6	SNR	Signal to Dist. (D to A)	Noise	-55dBm0	15			dB	
				-40	30			dB	
				-34	35			dB	
				-27 to -6	37			dB	
7	GTA	Gain Track. (A to A)	820Hz tone Relative to -10dBm0	-55 to -50dBm0	-1.0		1.0	dB	
				-50to-40	-0.5		0.5	dB	
				-40 to +3	-0.3		0.3	dB	
8	GNA	Gain Track. (A to A)	Noise Relative to -10dBm0	-60 to -55dBm0	-0.8		0.8	dB	
				-55 to -10	-0.4		0.4	dB	
9	GTX	Gain Track. (A to D)	820Hz tone Relative to -10dBm0	-55to-50	-0.8		0.8	dB	
				-50to-40	-0.4		0.4	dB	
				-40 to +3 dBm0	-0.2		0.2	dB	
10	GNX	Gain Track (A to D)	Noise Relative to -10dBm0	-60 to -55dBm0	-0.6		0.6	dB	
				-55 to -40	-0.4		0.4	dB	
				-40 to -10	-0.2		0.2	dB	
11	GTR	Gain Track (D to A)	820Hz tone Relative to -10dBm0	-55to-50	-0.8		0.8	dB	
				-50to-40	-0.4		0.4	dB	
				-40 to +3 dBm0	-0.2		0.2	dB	
12	GNR	Gain Track (D to A)	Noise Relative to -10dBm0	-60 to -55dBm0	-0.4		0.4	dB	
				-55 to -10	-0.2		0.2	dB	

(to be continued)

(con'd)

NO	SYM.	DESCRIPTIONS	TEST CONDITIONS		SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE
13	FRX	Freq.Response. (A to D) (Loss)	Relative to 820Hz 0dBm0	0.06kHz	24				
				0.2	0		2.0		
				0.3 to 3	-0.15		0.15	dB	
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				
14	FRR	Freq.Response. (D to A) (Loss)	Relative to 820Hz 0dBm0	0 to 3 kHz	-0.15		0.15		
				3.18	-0.15		0.65	dB	
				3.4	0		0.8		
				3.78	6.5				
15	AIL	Analog Input Level	820Hz 0dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
16	AOL	Analog Output Level	820Hz 0dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
17	ICNA	Idle Ch. Noise	A to A	AIN=AGND			-78	dBmOP	
18	ICNX	Idle Ch. Noise	A to D	AIN=AGND			-80	dBmOP	
19	ICNR	Idle Ch. Noise	D to A	PCMIN= +0-CODE			-80	dBmOP	
20	XTKA	AIN to AOUT Crosstalk	820Hz	0dBm0			-65	dB	
21	XTKD	PCMIN to PCMOUT	820Hz	0dBm0			-65	dB	

3-2. FOR HD44248C

NO	SYM.	DESCRIPTIONS	TEST CONDITIONS		SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE
1	SDA	Signal to Dist. (A to A)	1020Hztone	-45dBm0	25			dB	c-wgt
				-40	30			dB	
				-30 to +3	35			dB	
2	SDX	Signal to Dist. (A to D)	1020Hztone	-45dBm0	26			dB	c-wgt
				-40	31			dB	
				-30 to +3	36			dB	
3	SDR	Signal to Dist. (D to A)	1020Hztone	-45dBm0	26			dB	c-wgt
				-40	31			dB	
				-30 to +3	36			dB	
4	GTA	Gain Tracking (A to A)	1020Hztone	-55 to -50dBm0	-1.0		1.0	dB	
			Relative to -10dBm0	-50to-40	-0.5		0.5	dB	
				-40 to +3	-0.3		0.3	dB	
5	GTX	Gain Tracking (A to D)	1020Hztone	-55to-50	-0.8		0.8	dB	
			Relative to -10dBm0	-50to-40	-0.4		0.4	dB	
				-40 to +3 dBm0	-0.2		0.2	dB	
6	GTR	Gain Tracking (D to A)	1020Hztone	-55to-50	-0.8		0.8	dB	
			Relative to -10dBm0	-50to-40	-0.4		0.4	dB	
				-40 to +3 dBm0	-0.2		0.2	dB	
7	FRX	Freq.Response. (A to D) (Loss)	Relative to 1020Hz 0dBm0	0.06kHz	24				
				0.2	0		2.0		
				0.3 to 3	-0.15		0.15	dB	
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				

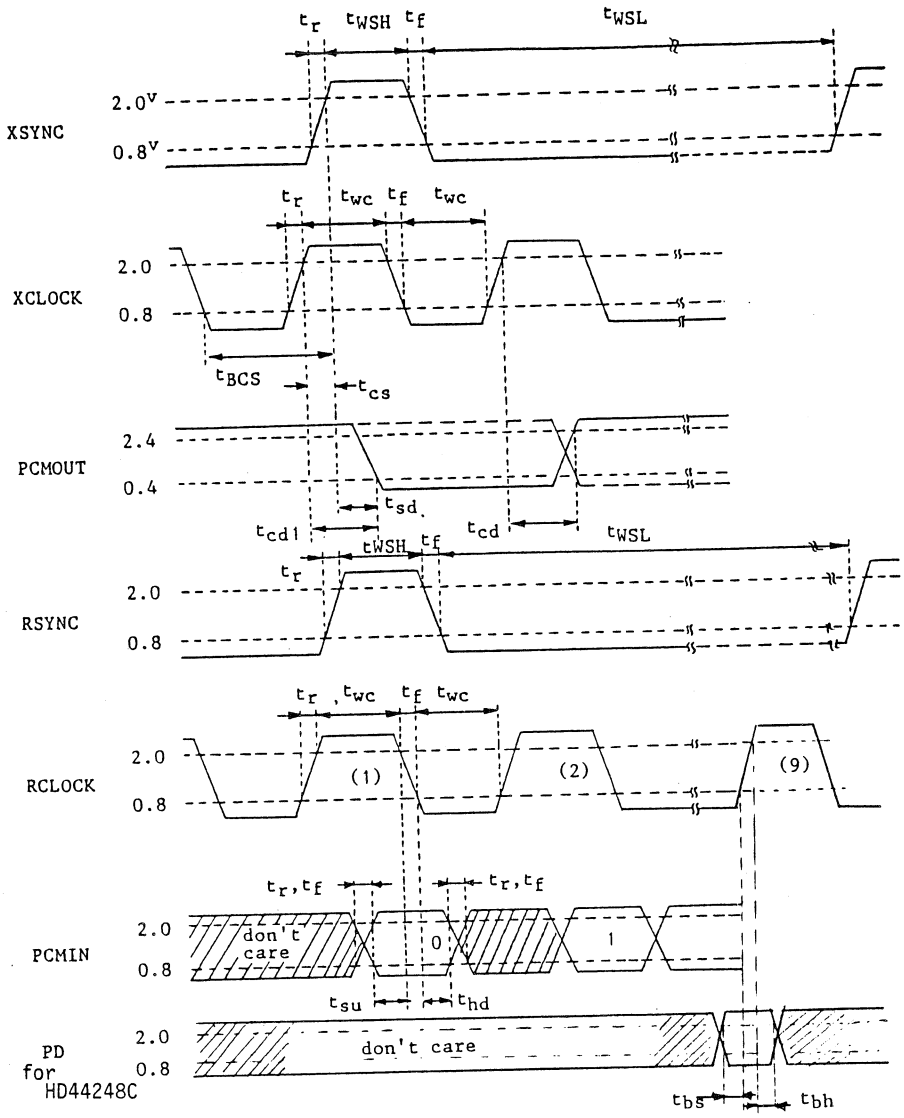
8	FRR	Freq.Response. (D to A) (Loss)	Relative to 1020Hz 0dBm0	0 to 3 kHz	-0.15		0.15	dB	
				3.18	-0.15		0.65		
				3.4	0		0.8		
				3.78	6.5				
9	AIL	Analog Input Level	1020Hz 0dBm0	25°C nom.P.S.	1.213	1.227	1.241	Vrms	
10	AOL	Analog Output Level	1020Hz 0dBm0	25°C nom.P.S.	1.213	1.227	1.241	Vrms	
11	ICNA	Idle Ch. Noise	A to A	AIN=AGND			16	dBrnC0	
12	ICNX	Idle Ch. Noise	A to D	AIN=AGND			16	dBrnC0	
13	ICNR	Idle Ch. Noise	D to A	PCMIN= +0-CODE			10	dBrnC0	
14	XTKA	AIN to AOUT Crosstalk	1020Hz 0dBm0				-65	dB	
15	XTKD	PCMIN to PCMOUT	1020Hz 0dBm0				-65	dB	

3-3. FOR HD44247C, HD44248C

No	Sym.	DESCRIPTION	TEST CONDITIONS		SPECIFICATIONS MIN	TYP	MAX	UNIT	NOTE
1	AT	AIL,AOL Variation with temp.	Relative to 25°C nominal P.S.			±20		ppm/°C	
2	AP	AIL,AOL Variation with P.S.	25°C, Supplies±5%			±0.01		dB	
3	ALS	GAIN Variation over Temp. P.S.	A to D D to A	INITIAL	-0.2		0.2	dB	Note1)
4	AIP	Peak Analog Input			3.0			V	
5	AOP	Peak Analog Output			2.5			V	
6	PDL	Propagation Delay	A to A	0dBm0		450	480	μs	
7	DD	Delay Distortion	A to A 0dBm0	0.5 to 0.6kHz			1.4	ms	rel. to min. delay
				0.6 to 1.0			0.7		
				1.0 to 2.6			0.2		
				2.6 to 2.8			1.4		
8	PSRR	PSRR	A to A AIN= AGND	Vdd Mod. =+5V+100mVop	30			dB	
			0.3-50kHz-	Vss Mod. =-5V+100mVop	30				
9	IM1	Intermodulation	A to A(2a-b) a;0.47kHz,-4dBm0 b;0.32, -4				-38	dB	
10	IM2	Intermodulation	A to A(a-b) a;1.02kHz,-4dBm0 b;0.05, -23				-52	dB	
11	ICS	Single Freq.Noise	A to A AIN=AGND	8,16,24, 32,40kHz			-50	dBm0	
12	DIS	Discrimination	A to A 0dBm0	4.6 to 200kHz	30			dB	

Note 1) Total variation of GAIN including the initial fluctuation temperature variation and power supply dependence (0 - 70°C, Vdd/Vss=±5V±5%)

Timing Chart



HD44270P/CP Series

Single Chip CODEC/Filter Combo LSI

PLASTIC VERSION

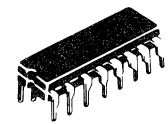
Type	Original Versions	Comp. Law	Power (Typ.)	Clock			Input Amp	Output Amp	
				Internal clock	Sync/Async Operation	PCM bit clock rate		Type	Min load
HD44271P	HD44247C	A	70mW	PLL Included	Both	64-2048kHz	Fully Uncommited Op-amp	Push-Pull	600Ω
HD44272P	HD44248C	μ	70mW						
HD44273P	HD44233C	A	50mW	Divider Included		1536/1544/2048 kHz		Single Ended	
HD44274P	HD44234C	μ	50mW						
HD44277P	HD44237C	A	50mW	PLL Included		64-2048kHz			
HD44278P	HD44238C	μ	50mW						

HD44271P/HD44272P/ HD44271CP/HD44272CP

Single Chip CODEC/Filter Combo LSI

PLASTIC VERSION

HD44271P HD44272P



(DP-16A)

HD44271CP HD44272CP

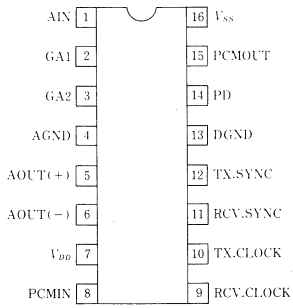
(CP-18)

FEATURES

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package and 18-pins PLCC package.
- Power Supply Voltage ±5V±5%, Low Power Dissipation.
- Follows μ-Law (HD44272P) or A-Law (HD44271P).
- Extremely Low Cost for the Digital PBX Terminal or Digital Handset Application.
- Internal Clock Generator for 64 kHz to 2048 kHz PCM Rate as PLL Circuit.
- Anti-Aliasing Filter (2nd order CR Active Filter).
- Voltage Reference (Internal-Trimmed).
- Input Amplifier with Uncommitted Plus/Minus Terminals.
- Auto-Zero Cancel Circuit without External Component.
- Push/Pull Analog Output.

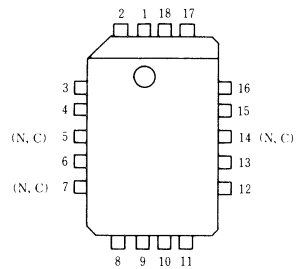
PIN ARRANGEMENT

●HD44271P/272P



(Top View)

●HD44271CP/272CP

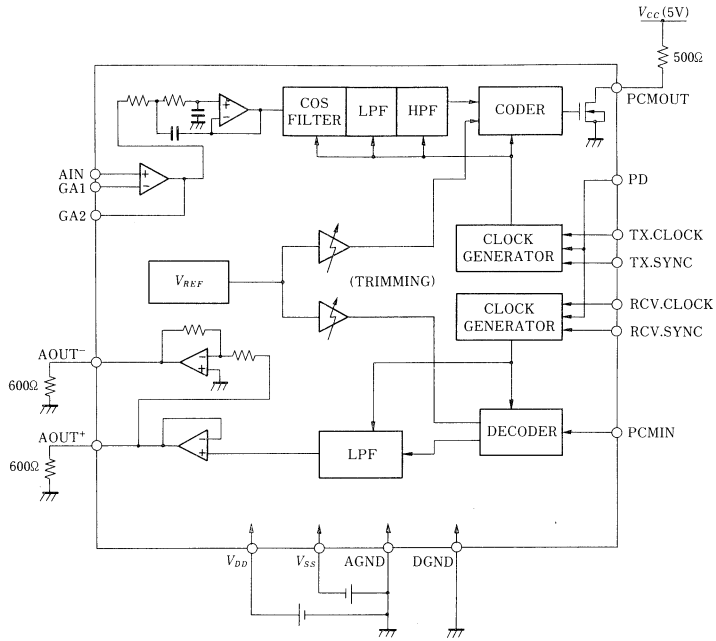


(Top View)

PIN DESCRIPTIONS

No.	Symbol	Function	Remarks
1	AIN	Analog input	
2	GA1	Gain adjust 1	Feed-back input
3	GA2	Gain adjust 2	10kΩ < R_L, C_L < 100pF
4	AGND	Analog ground	
5	AOUT (+)	Analog output	R_L > 600Ω, C_L < 100pF
6	AOUT (−)		R_L > 600Ω, C_L < 100pF
7	V_{DD}	Positive pow. sup.	5V ± 5%
8	PCMIN	PCM data input	(TTL)
9	RCV. CLK	PCM bit clock	(TTL) 64 kHz to 2048kHz
10	TX. CLK		
11	RCV. SYNC	Synchronization	(TTL) 8kHz
12	TX. SYNC		
13	DGND	Digital ground	
14	PD	Power down	(TTL) "0" = down
15	PCMOUT	PCM data output	Open drain
16	V_{SS}	Negative pow. sup.	−5V ± 5%

BLOCK DIAGRAM



PIN/FUNCTION DESCRIPTIONS

Pin	No	Descriptions
TX. CLOCK RCV. CLOCK	9 10	Any of 64kHz to 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX. SYNC/RCV. SYNC respectively.
TX. SYNC RCV. SYNC	11 12	These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK/RCV. CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX/SYNC. RCV. SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV. CLOCK.
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of -V_{REF} to +V_{REF} to the device The input stage can be connected as a unity gain amplifier, with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10k Ω or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT(+)	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100pF.

(to be continued)

Pin	No.	Descriptions
V_{DD} V_{SS} AGND DGND	7 16 4 13	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
AOUT(−)	6	This is the inverted output of pin 5 signal output to drive the 600 Ω transformer as the push-pull operation. R_L<600Ω, C_L<100pF.

■ABSOLUTE MAXIMUM RATINGS

Item	Rating
V_{DD}	−0.3 to +7V
V_{SS}	+0.3 to −7V
Storage temperature	−55°C to +125°C
Power dissipation	0.5W
Digital input/output voltage	$-0.3V < V_{IX} < V_{DD}+0.3V$
Analog input/output voltage	$V_{SS}-0.3V < V_{IX} < V_{DD}+0.3V$

■ELECTRICAL CHARACTERISTICS

●STATIC CHARACTERISTICS ($V_{DD}=5\pm0.25V$, $V_{SS}=-5\pm0.25V$, $V_{CC}=5\pm0.25V$, $T_a=0$ to +70°C)

Descriptions	Symbol	Pin	min	typ	max	Note conditions	Unit
V_{DD} current (ope.)	I_{DD}	7	–	8.0	13.5	Note 1 AIN=0V PCMIN = +0 code R_L (GA2)=10k Ω R_L (AOUT)=600 Ω	mA
V_{SS} current (ope.)	I_{SS}	16	−13.0	−7.5	–		
V_{DD} current (st.by.)	I_{DDST}	7	–	0.4	1.0		
V_{SS} current (st.by.)	I_{SSST}	16	−0.2	–	–		
Leak current	I_L	1, 2, 8	−10.0	–	10.0	V_M 0.8V	μA
		9, 10	10.0	–	10.0	V_M 2.0V	μA
		14	–	–	10.0	V_{DD} V_M 5.25V	μA
Pull up current	I_{PL}	11, 12	100	–	0		μA
Leak current	I_{IL}	15	–	–	10.0	V_{DD} V_M 5.25V	μA
Analog input cap.	C_{AIN1}	1	–	–	10	at 1MHz Vbias=0	pF
Analog input cap.	C_{AIN2}	2	–	–	10	at 1MHz Vbias=0	pF
Input capacitance	C_{DIN}	8,9,10,11,12,14	–	–	10	at 1MHz Vbias=0	pF
AOUT resistance	R_{OUTA}	5, 6	–	1	20		Ω
GA2 resistance	R_{OUTG}	3	–	–	50	Note 1	Ω
GA2 output swing	V_{GSW}	3	3.0	–	3.0	R_l = 10k Ω	V
Analog offset input	V_{OFFIN}	1	200	–	200	Note 1	mV
GA2 offset output	V_{OFFG}	3	50	–	50	Note 1	mV
AOUT offset output	V_{OFFA}	5, 6	100	–	100	PCMIN = +0−code	mV
PCMOUT capacitance	C_{MOUT}	15	–	–	15.0	at 1MHz,Vbias=0V	pF
PCMOUT low voltage	V_{OL}	15	–	–	0.4	R_l =500 Ω, I_{OL} 0.8mA	V
PCMOUT high voltage	V_{OH}	15	V_{CC} 0.3	–		I_{OH} = −150μA	V
Digital input high voltage	V_{IH}	8,9,10,11,12,14	2.0	–			V
Digital input low voltage	V_{IL}	8,9,10,11,12,14	–	–	0.8		V

Note 1) Analog input amplifier gain 0 dB (GA1 is connected to GA2)

●DYNAMIC-CHARACTERISTICS ($V_{DD}=5\pm0.25V$, $V_{SS}=-5\pm0.25V$, $V_{CC}=5\pm0.25V$, $T_a=0$ to $+70°C$)

Descriptions	Symbol	Note	min	typ	max	Unit
Synchronization rate	F_S		–	8	–	kHz
PCM bit clock rate	F_C		64	–	2048	kHz
Clock pulse width	t_{wc}		200	–	–	ns
Sync pulse high width	t_{wSH}		200	–	–	ns
Sync pulse low width	t_{wSL}		8	–	–	ns
Logic input rise time	t_r		5	–	50	ns
Logic input fall time	t_f		5	–	50	ns
Previous clock to Sync delay	t_{HCS}	Note 1	40	–	–	ns
Clock to sync delay	t_{cs}	Note 1, 3	–	–	100	ns
Clock to PCM MSB delay	t_{cdd}	Note 1, 2, 4	–	–	170	ns
Sync to PCM MSB delay	t_{sd}	Note 1, 2, 4	–	–	170	ns
Clock to PCM OUT delay	t_{cd}	Note 1, 2, 5	–	–	180	ns
PCMIN setup time	t_{su}	Note 1	65	–	–	ns
PCMIN hold time	t_{hd}	Note 1	120	–	–	ns

Note 1) t_r, t_f of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT load condition: 500Ω + 165pF + two LS-TTL Equivalent ($I_{IL}=0.8$mA, $I_{IH}=-150\mu$A) Threshold level ($V_{OH}=2.4V$, $V_{OL}=0.4V$)
3) Positive value shows SYNC delay from CLOCK.
4) t_{cdd}, t_{sd} are specified by CLOCK or SYNC which has slower rise time.
5) t_{cd} specification is valid for the data except MSB.

●SYSTEM RELATED CHARACTERISTICS

($V_{DD}=5\pm0.25V$, $V_{SS}=-5\pm0.25V$, $V_{CC}=5\pm0.25V$, $T_a=0$ to $+70°C$, INPUT AMPLIFIER GAIN = 0dB, ANALOG OUT PUT = AOUT(−), GA2 LOAD = 10kΩ, AOUT LOAD = 600Ω, Synchronous operation. F_C (PCM BIT CLOCK) = 2048kHz)

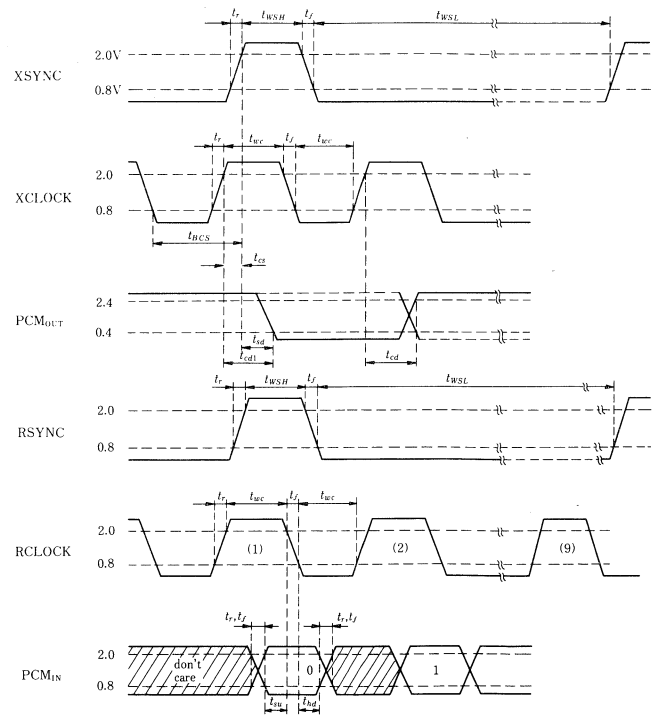
For HD44271P/CP

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	820Hz tone	−45dBm0	23	–	–	dB	p-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain track. (A to A)	GTA	820Hz tone Relative to −10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10,0,3	−0.3	–	0.3		
Freq. response. (A to D)(Loss)	FRX	Relative to 820Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq. response.(D to A)(Loss)	FRR	Relative to 820Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level variation	AIL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	−80	dBm0P	
Idle ch. noise	ICNR	D to A	PCMIN = +0−Code	–	–	−80	dBm0P	
AIN to AOUT crosstalk	XTKA	820Hz	0dBm0	–	–	−65	dB	
PCMIN to PCMOUT	XTKD	820Hz	0dBm0	–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

For HD44272P/CP

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	1020Hz tone	−45dBm0	23	–	–	dB	c-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain Tracking(A to A)	GTA	1020Hz tone relative to −10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10,0.3	−0.3	–	0.3		
Freq.Response.(A to D)(Loss)	FRX	Relative to 1020Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq.Response.(D to A)(Loss)	FRR	Relative to 1020Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level	AIL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	16	dBrnC0	
Idle ch. noise	ICNR	D to A	PCMIN = +0−code	–	–	10	dBrnC0	
AIN to AOUT crosstalk	XTKA	1020Hz 0dBm0		–	–	−65	dB	
PCMIN to PCMOUT crosstalk	XTKD	1020Hz 0dBm0		–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

■TIMING CHART

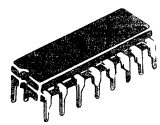


HD44273P/HD274P/ HD44273P/HD44274CP

Single Chip CODEC/Filter Combo LSI

—PLASTIC VERSION—

HD44273P/HD44274P



(DP-16A)

HD44273CP/HD44274CP

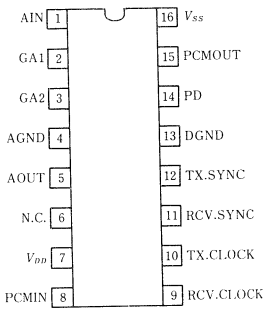
(CP-18)

■FEATURES

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package 18-pins PLCC Package.
- Power Supply Voltage ±5V±5%, Low Power Dissipation.
- Follows μ-Law (HD44274P) or A-Law (HD44273P).
- Extremely Low Cost for the Digital PBX Terminal or Digital Handset Application.
- Asynchronous Operation for 2048/1544/1536 kHz PCM Rate.
- Anti-Aliasing Filter (2nd order CR Active Filter).
- Voltage Reference (Internal-Trimmed).
- Input Amplifier with Uncommitted Plus/Minus Terminals.
- Auto-Zero Cancel Circuit without External Component.

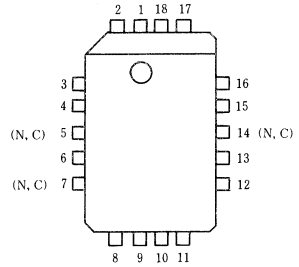
■PIN ARRANGEMENT

● HD44273P/274P



(Top View)

● HD44273CP/274CP



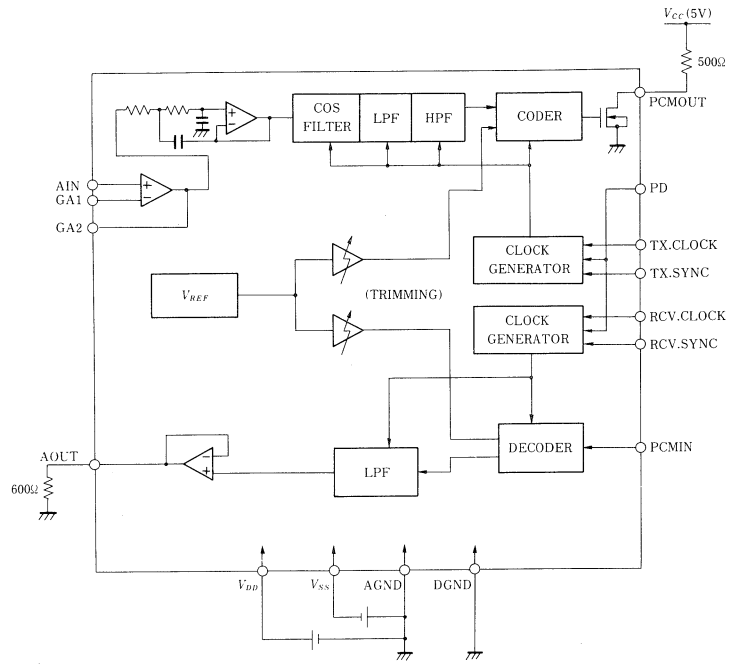
(Top View)

■PIN DESCRIPTIONS

No.	Symbol	Function	Remarks
1	AIN	Analog input	
2	GA1	Gain adjust 1	Feed-back input
3	GA2	Gain adjust 2	10kΩ < RL, CL < 100pF
4	AGND	Analog ground	
5	AOUT	Analog output	R_L > 600Ω, C_L < 100pF
6	N.C.		
7	V_{DD}	Positive pow. sup.	5V ± 5%
8	PCMIN	PCM data input	(TTL)
9	RCV. CLK	PCM bit clock	(TTL) 2048, 1544, 1536kHz
10	TX. CLK		
11	RCV. SYNC	Synchronization	(TTL) 8kHz
12	TX. SYNC		
13	DGND	Digital ground	
14	PD	Power down	(TTL) "0" - down
15	PCMOUT	PCM data output	Open drain
16	V_{SS}	Negative pow. sup.	−5V ± 5%

HITACHI

■BLOCK DIAGRAM



■PIN/FUNCTION DESCRIPTIONS

Pin	No	Descriptions
TX. CLOCK RCV. CLOCK	9 10	One of 1.536, 1.544 and 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX. SYNC RCV. SYNC respectively.
TX. SYNC RCV. SYNC	11 12	These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK/RCV. CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmisson of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX/SYNC. RCV. SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV. CLOCK.
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. The input stage can be connected as a unity gain amplifier, with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10k Ω or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100pF.

(to be continued)

Pin	No.	Descriptions
V_{DD} V_{SS} AGND DGND	7 16 4 13	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.

■ABSOLUTE MAXIMUM RATINGS

Item	Rating
V_{DD}	−0.3 to +7V
V_{SS}	+0.3 to −7V
Storage temperature	−55°C to +125°C
Power dissipation	0.5W
Digital input output voltage	$-0.3V < V_{IN} < V_{DD}+0.3$
Analog input output voltage	$V_{SS}-0.3V < V_{IN} < V_{DD}+0.3$

■ELECTRICAL CHARACTERISTICS

●STATIC CHARACTERISTICS ($V_{DD}=5\pm0.25V$, $V_{SS}=-5\pm0.25V$, $V_{CC}=5\pm0.25V$, $T_a=0$ to +70°C)

Descriptions	Symbol	Pin	min	typ	max	Note conditions	Unit
V_{DD} current (ope.)	I_{DD}	7	–	5.5	10	Note 1 AIN = 0V PCMIN = +0 code R_L (GA2) = 10k Ω R_L (AOUT) = 600 Ω	mA
V_{SS} current (ope.)	I_{SS}	16	−10	−4.5	–		
V_{DD} current (st.by.)	I_{DDST}	7	–	0.3	1.0		
V_{SS} current (st.by.)	I_{SSST}	16	−0.2	–	–		
Leak current	I_L	1, 2, 8 9, 10 14	−10.0	–	10.0	V_M = 0.8V	μA
			−10.0	–	10.0	V_M = 2.0V	
			–	–	10.0	$V_{DD}=V_M$ = 5.25V	
Pull up current	I_{PL}	11, 12	−100	–	0		μA
Leak current	I_{DL}	15	–	–	10.0	$V_{DD}=V_M$ = 5.25V	μA
Analog input cap.	C_{AIN1}	1	–	–	10	at 1MHz, Vbias = 0	pF
Analog input cap.	C_{AIN2}	2	–	–	10	at 1MHz, Vbias = 0	pF
Input capacitance	C_{DIN}	8,9,10,11,12,14	–	–	10	at 1MHz, Vbias = 0	pF
AOUT resistance	R_{OUTA}	5	–	1	20		Ω
GA2 resistance	R_{OUTG}	3	–	–	50	Note 1	Ω
GA2 output swing	V_{GSW}	3	−3.0	–	3.0	R_L = 10k Ω	V
Analog offset input	V_{OFFIN}	1	−200	–	200	Note 1	mV
GA2 offset output	V_{OFFG}	3	−50	–	50	Note 1	mV
AOUT offset output	V_{OFFA}	5	−100	–	100	PCMIN = +0−code	mV
PCMOUT capacitance	C_{DOUT}	15	–	–	15.0	at 1MHz, Vbias = 0V	pF
PCMOUT low voltage	V_{OL}	15	–	–	0.4	R_L = 500 Ω, $+I_{OL}$ = 0.8mA	V
PCMOUT high voltage	V_{OH}	15	$V_{CC}-0.3$	–	–	$I_{OL}=-150\mu A$	V
Digital input high voltage	V_{IH}	8,9,10,11,12,14	2.0	–	–		V
Digital input low voltage	V_{IL}	8,9,10,11,12,14	–	–	0.8		V

Note 1) Analog input amplifier gain = 0 dB (GA1 is connected to GA2)

●DYNAMIC-CHARACTERISTICS (V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C)

Descriptions	Symbol	Note	min	typ	max	Unit
Synchronization rate	F_S		–	8	–	kHz
PCM bit clock rate	F_C		–	1536 1544 2048	–	kHz
Clock pulse width	t_{wc}		200	–	–	ns
Sync pulse high width	t_{wSH}		200	–	–	ns
Sync pulse low width	t_{wSL}		8	–	–	μs
Logic input rise time	t_r		5	–	50	ns
Logic input fall time	t_f		5	–	50	ns
Previous clock to Sync delay	t_{hCS}	Note 1	40	–	–	ns
Clock to Sync delay	t_{CS}	Note 1, 3	–	–	100	ns
Clock to PCM MSB delay	t_{dM}	Note 1, 2, 4	–	–	170	ns
Sync to PCM MSB delay	t_{sd}	Note 1, 2, 4	–	–	170	ns
Clock to PCMOUT delay	t_{cd}	Note 1, 2, 5	–	–	180	ns
PCMIN setup time	t_{su}	Note 1	65	–	–	ns
PCMIN hold time	t_{hd}	Note 1	120	–	–	ns

Note 1) t_r, t_f of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT load condition: 500 Ω + 165pF + two LS-TTL Equivalent (I_{IL} = 0.8mA, I_{IH} = −150μA) Threshold level (V_{OH} = 2.4V, V_{OL} = 0.4V)
3) Positive value shows SYNC delay from CLOCK.
4) t_{dM}, t_{sd} are specified by CLOCK or SYNC which has slower rise time.
5) t_{cd} specification is valid the data except MSB.

●SYSTEM RELATED CHARACTERISTICS

(V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C, INPUT AMPLIFIER GAIN = 0dB, ANALOG OUT PUT = AOUT(−), GA2 LOAD = 10k Ω, AOUT LOAD = 600 Ω, Synchronous operation. F_C (PCM BIT CLOCK) = 2048kHz)

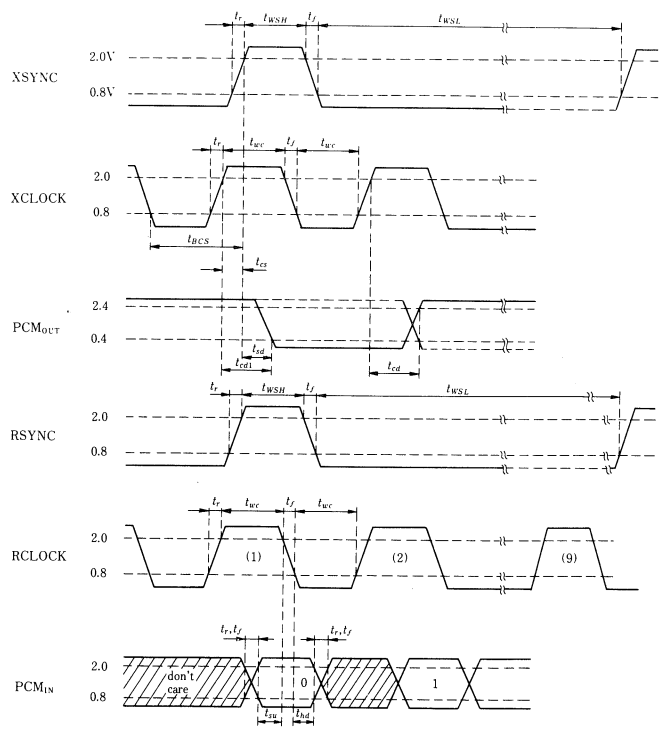
For HD44273P

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	820Hz tone	−45dBm0	23	–	–	dB	p-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain track. (A to A)	GTA	820Hz tone Relative to −10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10, 0, 3	−0.3	–	0.3		
Freq. response. (A to D)(Loss)	FRX	Relative to 820Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq. response.(D to A)(Loss)	FRR	Relative to 820Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level variation	AIL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	−80	dBm0P	
Idle ch. noise	ICNR	D to A	PCMIN = +0−Code	–	–	−80	dBm0P	
AIN to AOUT crosstalk	XTKA	820Hz	0dBm0	–	–	−65	dB	
PCMIN to PCMOUT	XTKD	820Hz	0dBm0	–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

For HD44274P/CP

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	1020Hz tone	45dBm0	23			dB	c-wgt
			−40	28				
			30, 20, 10,0	34				
Gain Tracking(A to A)	GTA	1020Hz tone relative to-10dBm0	−55dBm0	−1.0		1.0	dB	
			−50	−0.5		0.5		
			−40, −30, 20, −10,0.3	−0.3		0.3		
Freq.Response.(A to D)(Loss)	FRX	Relative to 1020Hz 0dBm0	0.06kHz	24		–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq-Response. (D to A)(Loss)	FRR	Relative to 1020Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level	AIL	1020Hz 0dBm0	Relative to 1.227Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	1020Hz 0dBm0	Relative to 1.227Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	−80	dBm0P	
Idle ch. noise	ICNR	D to A	PCMIN = +0−code	–	–	−80	dBm0P	
AIN to AOUT crosstalk	XTKA	820Hz	0 dBm 0	–	–	−65	dB	
PCMIN to PCMOUT crosstalk	XTKD	820Hz	0 dBm 0	–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

TIMING CHART

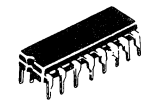


HD44277P/HD44278P/ HD44277CP/HD44278CP

Single Chip CODEC/Filter Combo LSI

—PLASTIC VERSION—

HD44277P/HD44278P



(DP-16A)

HD44277CP HD44278CP

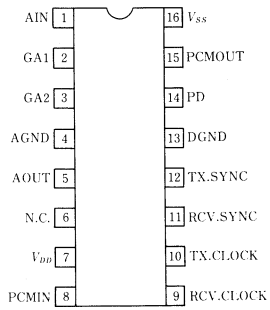
(CP-18)

■FEATURES

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package and 18-pins PLCC Package.
- Power Supply Voltage ±5V±5%, Low Power Dissipation.
- Follows μ-Law (HD44278P) or A-Law (HD44277P).
- Extremely Low Cost for the Digital PBX Terminal or Digital Handset Application.
- Internal Clock Generator for 64 kHz to 2048 kHz PCM Rate as PLL Circuit.
- Anti-Aliasing Filter (2nd order CR Active Filter).
- Voltage Reference (Internal-Trimmed).
- Input Amplifier with Uncommitted Plus/Minus Terminals.
- Auto-Zero Cancel Circuit without External Component.

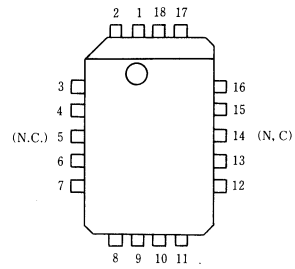
■PIN ARRANGEMENT

●HD44277P/278P



(Top View)

●HD44277CP/278CP

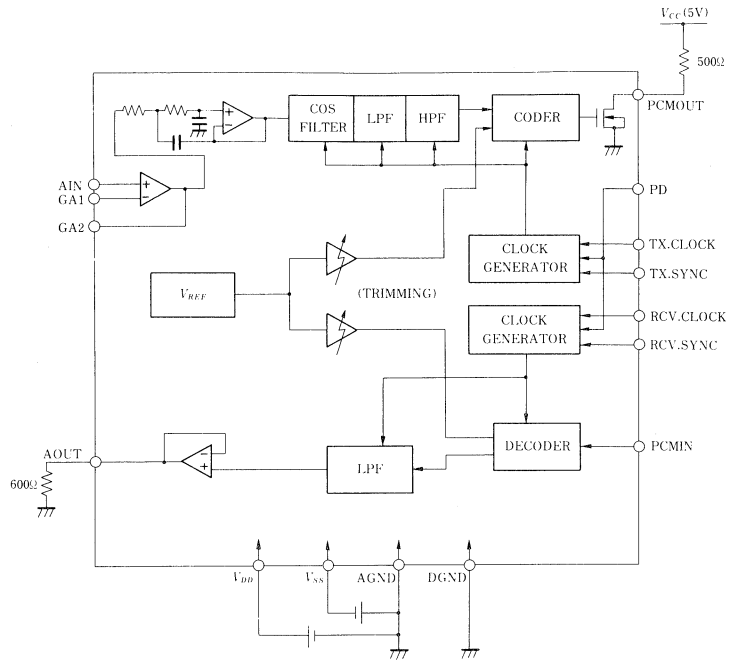


(Top View)

■PIN DESCRIPTIONS

No.	Symbol	Function	Remarks
1	AIN	Analog input	
2	GA1	Gain adjust 1	Feed-back input
3	GA2	Gain adjust 2	10k Ω < R_L, C_L < 100pF
4	AGND	Analog ground	
5	AOUT	Analog output	R_L > 600 Ω, C_L < 100pF
6	N.C.		
7	V_{DD}	Positive pow. sup.	5V ± 5%
8	PCMIN	PCM data input	(TTL)
9	RCV. CLK	PCM bit clock	(TTL) 64kHz to 2048kHz
10	TX. CLK		
11	RCV. SYNC	Synchronization	(TTL) 8kHz
12	TX. SYNC		
13	DGND	Digital ground	
14	PD	Power down	(TTL) "0" down
15	PCMOUT	PCM data output	Open drain
16	V_{SS}	Negative pow. sup.	5V ± 5%

BLOCK DIAGRAM



PIN/FUNCTION DESCRIPTIONS

Pin	No	Descriptions
TX. CLOCK RCV. CLOCK	9 10	Any of 64kHz to 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX. SYNC RCV. SYNC respectively.
TX. SYNC RCV. SYNC	11 12	These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK RCV. CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK, TX.CLOCK RCV.CLOCK signal following a positive edge on the SYNC, TX SYNC. RCV. SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV. CLOCK.
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of-V_{REF} to + V_{REF} to the device. The input stage can be connected as a unity gain amplifier, with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10k Ω or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_1 should be less than 100 pF.
AOUT	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_1 should be less than 100pF.

(to be continued)

Pin	No.	Descriptions
V_{DD} V_{SS} AGND DGND	7 16 4 13	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.

■ABSOLUTE MAXIMUM RATINGS

Item	Rating
V_{DD}	−0.3 to +7V
V_{SS}	+0.3 to −7V
Storage temperature	−55°C to +125°C
Power dissipation	0.5W
Digital input output voltage	$-0.3V < V_{IN} < V_{DD}+0.3$
Analog input output voltage	$V_{SS}-0.3V < V_{IN} < V_{DD}+0.3$

■ELECTRICAL CHARACTERISTICS

●STATIC CHARACTERISTICS ($V_{DD}=5\pm0.25V$, $V_{SS}=-5\pm0.25V$, $V_{CC}=5\pm0.25V$, $T_a=0$ to +70°C)

Descriptions	Symbol	Pin	Min	Typ	Max	Note conditions	Unit
V_{DD} current (ope.)	I_{DD}	7	–	5.5	10	Note 1 AIN=0V PCMIN=+0 code R_L (GA2)=10kΩ R_L (AOUT)=600Ω	mA
V_{SS} current (ope.)	I_{SS}	16	−10	−4.5	–		
V_{DD} current (st.by.)	I_{DDST}	7	–	0.3	1.0		
V_{SS} current (st.by.)	I_{SSST}	16	−0.2	–	–		
Leak current	I_L	1, 2, 8 9, 10 14	−10.0	–	10.0	$V_M=0.8V$	μA
			−10.0	–	10.0	$V_M=2.0V$	
			–	–	10.0	$V_{DD}=V_M=5.25V$	
Pull up current	I_{PL}	11, 12	−100	–	0		μA
Leak current	I_{DL}	15	–	–	10.0	$V_{DD}=V_M=5.25V$	μA
Analog input cap.	C_{AIN1}	1	–	–	10	at 1MHz, Vbias=0V	pF
Analog input cap.	C_{AIN2}	2	–	–	10	at 1MHz, Vbias=0V	pF
Input capacitance	C_{DIN}	8,9,10,11,12,14	–	–	10	at 1MHz, Vbias=0V	pF
AOUT resistance	R_{OUTA}	5	–	1	20		Ω
GA2 resistance	R_{OUTG}	3	–	–	50	Note 1	Ω
GA2 output swing	V_{GSW}	3	−3.0	–	3.0	$R_L=10k\Omega$	V
Analog offset input	V_{OFFIN}	1	−200	–	200	Note 1	mV
GA2 offset output	V_{OFFG}	3	−50	–	50	Note 1	mV
AOUT offset output	V_{OFFA}	5	−100	–	100	PCMIN=+0−code	mV
PCMOUT capacitance	C_{DOUT}	15	–	–	15.0	at 1MHz, Vbias=0V	pF
PCMOUT low voltage	V_{OL}	15	–	–	0.4	$R_L=500\Omega$, $+I_{OL}=0.8mA$	V
PCMOUT high voltage	V_{OH}	15	$V_{CC}-0.3$	–	–	$I_{OH}=-150\mu A$	V
Digital input high voltage	V_{IH}	8,9,10,11,12,14	2.0	–	–		V
Digital input low voltage	V_{IL}	8,9,10,11,12,14	–	–	0.8		V

Note 1) Analog input amplifier gain = 0 dB (GA1 is connected to GA2)

●DYNAMIC-CHARACTERISTICS (V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C)

Descriptions	Symbol	Note	min	typ	max	Unit
Synchronization rate	F_S		–	8	–	kHz
PCM bit clock rate	F_C		64	–	2048	kHz
Clock pulse width	t_{wc}		200	–	–	ns
Sync pulse high width	t_{wSH}		200	–	–	ns
Sync pulse low width	t_{wSL}		8	–	–	μs
Logic input rise time	t_r		5	–	50	ns
Logic input fall time	t_f		5	–	50	ns
Previous clock to sync delay	t_{HCS}	Note 1	40	–	–	ns
Clock to sync delay	t_{cs}	Note 1, 3	–	–	100	ns
Clock to PCM MSB delay	t_{cdd}	Note 1, 2, 4	–	–	170	ns
Sync to PCM MSB delay	t_{sd}	Note 1, 2, 4	–	–	170	ns
Clock to PCMOUT delay	t_{cd}	Note 1, 2, 5	–	–	180	ns
PCMIN setup time	t_{su}	Note 1	65	–	–	ns
PCMIN hold time	t_{hd}	Note 1	120	–	–	ns

Note 1) t_r, t_f of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT load condition: 500Ω + 165pF + two LS-TTL Equivalent (I_{IH} = 0.8mA, I_{IH} = −150μA) Threshold level (V_{OH} = 2.4V, V_{OL} = 0.4V)
3) Positive value shows SYNC delay from CLOCK.
4) t_{cdd}, t_{sd} are specified by CLOCK or SYNC witch has slower rise time.
5) t_{cd} specification is valid for the data except MSB.

●SYSTEM RELATED CHARACTERISTICS

(V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C, INPUT AMPLIFIER GAIN = 0dB, ANALOG OUTPUT = AOUT(−), GA2 LOAD = 10kΩ, AOUT LOAD = 600Ω, Synchronous operation. FC(PCM BIT CLOCK) = 2048kHz)

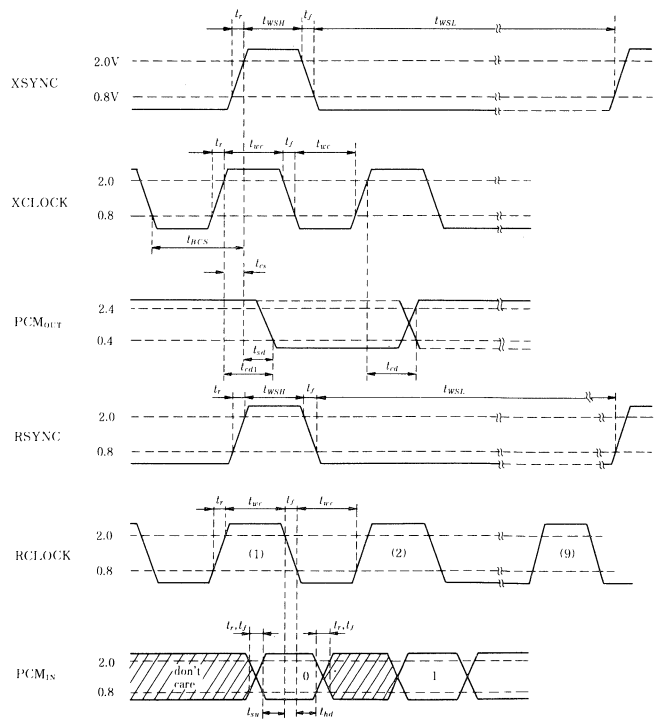
For HD44277P/CP

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	820Hz tone	−45dBm0	23	–	–	dB	p-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain track. (A to A)	GTA	820Hz tone Relative to-10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10,0,3	−0.3	–	0.3		
Freq. response. (A to D)(Loss)	FRX	Relative to 820Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq. response.(D to A)(Loss)	FRR	Relative to 820Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level variation	AIL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	−80	dBm0P	
Idle ch. noise	ICNR	D to A	PCMIN = +0−Code	–	–	−80	dBm0P	
AIN to AOUT crosstalk	XTKA	820Hz	0dBm0	–	–	−65	dB	
PCMIN to PCMOUT	XTKD	820Hz	0dBm0	–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

For HD44278P/CP

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	1020Hz tone	−45dBm0	23	—	—	dB	c-wgt
			−40	28	—	—		
			−30, −20, −10,0	34	—	—		
Gain Tracking(A to A)	GTA	1020Hz tone relative to-10dBm0	−55dBm0	−1.0	—	1.0	dB	
			−50	−0.5	—	0.5		
			−40, −30, −20, −10,0,3	−0.3	—	0.3		
Freq.Response.(A to D)(Loss)	FRX	Relative to 1020Hz 0dBm0	0.06kHz	24	—	—	dB	
			0.2	0	—	2.5		
			0.3 to 3	−0.3	—	0.3		
			3.4	0	—	0.8		
			3.78	6.5	—	—		
Freq.response.(D to A)(Loss)	FRR	Relative to 1020Hz 0dBm0	0 to 3kHz	−0.3	—	0.3	dB	
			3.4	0	—	0.8		
			3.78	6.5	—	—		
Analog input level	AIL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	—	0.5	dB	
Analog output level	AOL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	—	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN=AGND	—	—	16	dBrnC0	
Idle ch. noise	ICNR	D to A	PCMIN = +0−code	—	—	10	dBrnC0	
AIN to AOUT crosstalk	XTKA	1020Hz 0dBm0		—	—	−65	dB	
PCMIN to PCMOUT crosstalk	XTKD	1020Hz 0dBm0		—	—	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	—	40	—	dB	

■TIMING CHART



Application Specific CODEC

▩SUMMARY

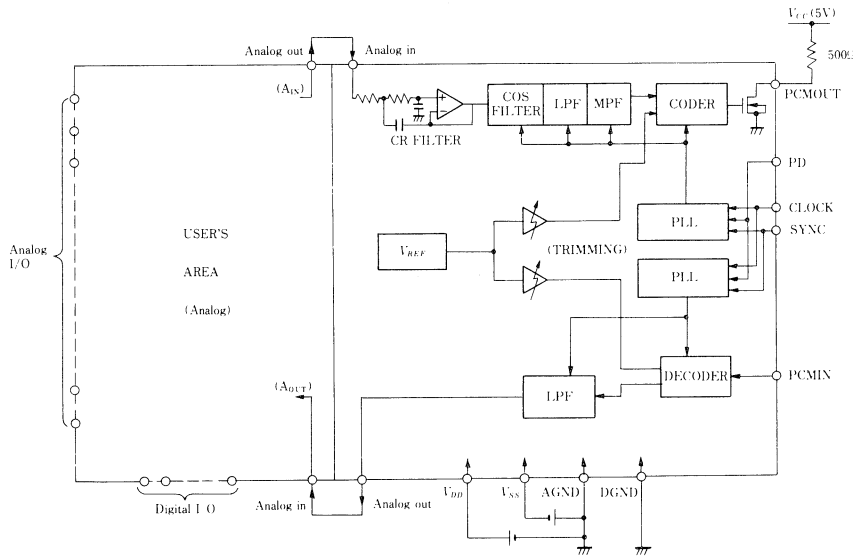
This custom LSI is one chipped based on the request of analog part including codec used in Digital Bottan Telephone. A system cost is possible to be declined by decreasing parts numbers. As core codec, HD44270P series should be used. And designed cell like Op Amp/Analog switch or requested circuit can be used at connecting analog part.

▩CHARACTERISTICS

(1) Silicone Gate process with 5 μm CMOS Capaciter.
(2) Power Voltage ±5V±10%.
Actionable Temperature 0 to +70°C.
(3) HD44270P series codec can be used as core.
(4) A system cost decrease by one-chip custom spec of peripheral analog part including codec.
(5) Save time for development by use cell below.
- CODEC (HD44270P series)
- Op Amp, Buffer amp) Analog I/O for Gain modulation
- Analog switch for pass switching
- Resistance
- Capacitance
- Ringing Generation Circuit
- Level Detection Circuit

(6) Use FPP, PLCC or DILP package (Max 80 pins)

▩BLOCK DIAGRAM

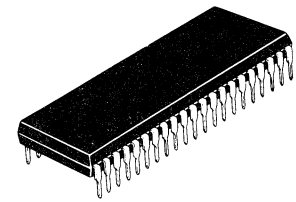


HA16811NT — Preliminary

SLIC IC for PABX Applications

■FEATURES

- Monolithic Integrated Circuit by Bipolar Linear Process.
- Internal Power Transistors for Battery Feed.
- Supply Voltage (Battery Feed Stage) −24V Type.
- Internal Relay Drivers (source type) for Ringing and Messagewaiting.
- Constant Current Feed.
- Current Shutdown Function.
- 2w-4w Conversion.
- Ring Trip Detection.
- Loop Back Function.



(DP-42SA)

■FUNCTIONAL DESCRIPTION

- Basic Function

1) Battery Feed Control

The HITACHI SLIC feeds constant current to a subscriber line. The integration of power transistors for battery feed makes it possible to save the mounting space on line card.

2) Loop Supervision

The SLIC supervises subscriber's hook status (ON HOOK/OFF HOOK).

3) Hybrid Function

This SLIC also provides 2-wire balanced to 4-wire single ended conversion preventing the 4-wire input signal from returning to the 4-wire output (Transhybrid rejection).

- Additional Function

1) Ring Trip Detection

With externally connected CR filter, the HITACHI SLIC can detect the off hook of a called subscriber, while ring relay is sending a ringing signal. When the subscriber goes off hook, a DC current superimposed on the ringing signal flows through the telephone. This superimposed DC current is detected by the SLIC and a ring trip detection signal is sent to the system controller from '$\overline{SCN}$' pin.

2) Current Shut Off Function

When it becomes necessary to protect PBX system by the following causes;

(1) Line fault of subscriber loop.

(2) Overload during an emergency.

the HITACHI SLIC can stop current feeding by the command from the system controller to the '$\overline{BF}$' pin.

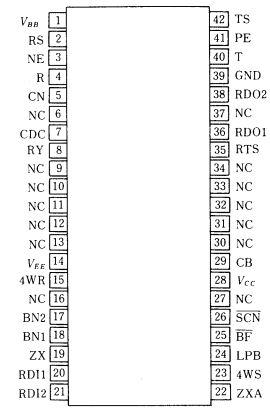
3) Relay Drivers

Our SLIC has two internal relay drivers. They are available to ringing relay and message waiting relay.

4) Loop Back Function

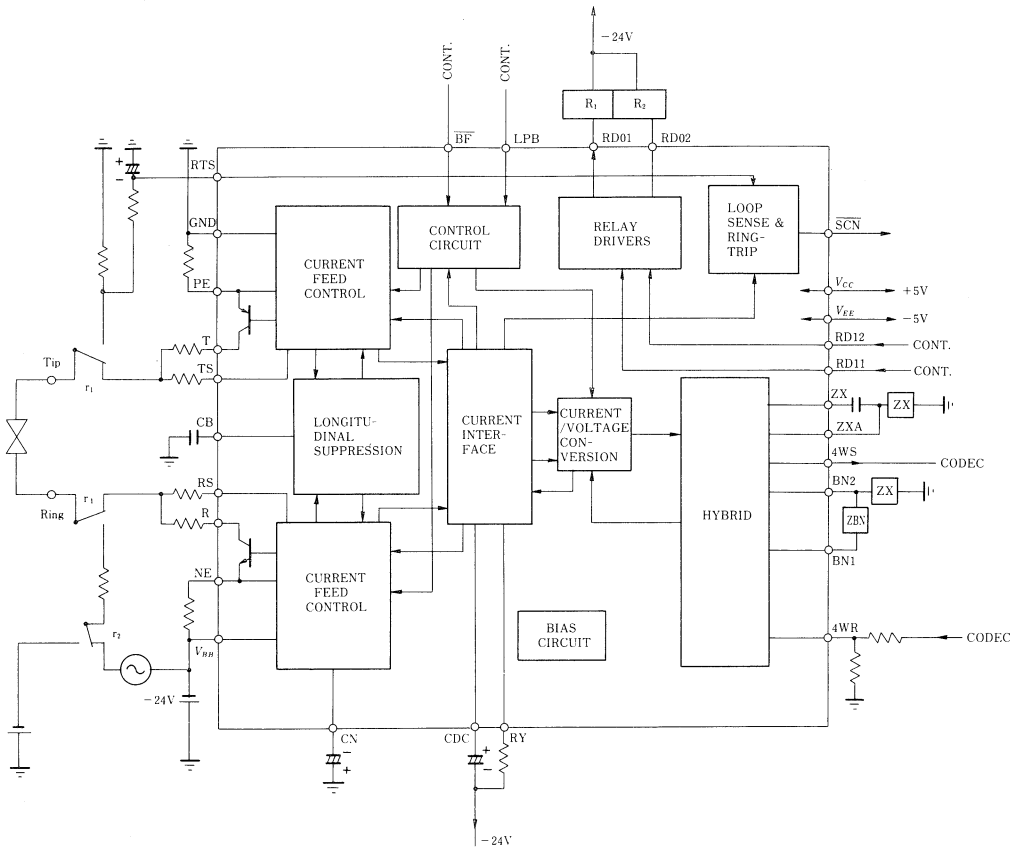
Though HITACHI SLIC usually cancells the 4-wire returning signal, it can send a 4-wire input signal as a 4-wire output signal without sending it to the subscriber loop if there is a loop back command at 'LPB' pin.

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■PIN DESCRIPTIONS

No	Pin	Function
1	V_{BB}	−24V voltage source input
2	RS	Ring side potential detection input which is connected the subscriber line through the resistor for detection.
3	NE	Ring side NPN darlington transistors' emitter potential detection input which is connected to V_{BB} through the emitter resistor.
4	R	Ring side current feed output (sink) which is connected to the subscriber line through protection resistor.
5	CN	is connected to ground through the capacitor for power supply noise rejection.
6	NC	No connection pin. It must not be connected to any other pin or printed circuit.
7	CDC	is connected to −24 voltage source through the AC bypass capacitor.
8	RY	is connected to −24 voltage source through the resistor in order to make a precise differential feedback loop.
9	NC	These are heatsink pins, therefore they are connected to the heatsink area fabricated on the printed board. They must not be connected to any other pin or printed circuit.

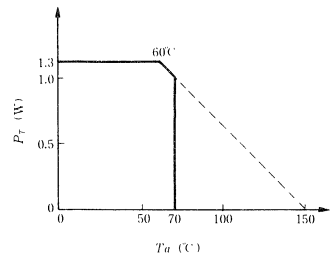
(to be continued)

No	Pin	Function
10	NC	These are heatsink pins, therefore they are connected to the heatsink area fabricated on the printed board. They must not be connected to any other pin or printed circuit.
11	NC	
12	NC	
13	NC	
14	V_{EE}	−5V voltage source input.
15	4WR	4-wire receive input which is connected to CODEC.
16	NC	No connection pin. It must not be connected to any other pin or printed circuit.
17	BN2	An analog input of differential amp. for transhybrid rejection, and is connected to the ground through impedance ZX,, and is also connected to 'BN1' through ZBN.
18	BN1	Received signal output which is connected to 'BN2' through balancing impedance ZBN.
19	ZX	Termination impedance setting output-A DC cut capacitor and termination impedance ZX is connected b between this terminal and the ground.
20	RDI1	A TTL level digital input for relay enable signal from the system controller.
21	RDI2	A TTL level digital input for relay enable signal from the system controller.
22	ZXA	An analog input of differential amp. for transmission which is connected to 'ZX' through DC cut capacitor.
23	4WS	4-wire transmission output which is connected to CODEC.
24	LPB	A TTL level digital input for loop back enable signal from the system controller.
25	$\overline{BF}$	A TTL level digital input for current shut off command from the system controller.
26	$\overline{SCN}$	A TTL compatible digital output which is a common output of loop supervision and ring trip detection signal.
27	NC	No connection pin. It must not be connected to any other pin or printed circuit.
28	V_{CC}	+5V voltage source input.
29	CB	is connected to the ground through the phase compensation capacitor for balance amp.
30	NC	These are heatsink pins, therefore they are connected to the heatsink area fabricated on the printed board. They must not be connected to any other pin or printed circuit.
31	NC	
32	NC	
33	NC	
34	NC	
35	RTS	A CR filter for ring trip detection is connected to this terminal.
36	RDO1	An analog output of relay driver which is connected to −24V voltage source through a relay coil.
37	NC	No connection pin. It must not be connected to any other pin or printed circuit.
38	RDO2	An analog output of relay driver which is connected to −24V voltage source through a relay coil.
39	GND	Ground pin.
40	T	Tip side current feed output (source) which is connected to the subscriber line through protection resistor.
41	PE	Tip side PNP darlington transistors' emitter potential detection input which is connected to the ground through the emitter resistor.
42	TS	Tip side potential detection input which is connected to the subscriber line through the resistor for detection.

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage (Battery Feed Stage)	V_{BB}	30	V
Supply Voltage (Control Stage)	V_{CC}	+7	V
	V_{EE}	−7	V
Power Dissipation *	P_T	1300	mW
Operating Temperature Range	Topr	0 to +70	°C
Storage Temperature Range	Tstg	−55 to +125	°C

* See derating curve



■RECOMMENDED OPERATION CONDITIONS

Item	Symbol	Conditions	Unit
Supply Voltage (Battery Feed Stage)	V_{BB}	−21.6 to −26.4	V
Supply Voltage (Control Stage)	V_{CC}	4.75 to 5.25	V
	V_{EE}	−4.75 to −5.25	V
Maximum Analog Signal Input Level	V_{i2W}	3.5	dBm
	V_{i4W}	1.5	dBm
Maximum High Level Logic Input Voltage	V_{IH}	2.0	V
Maximum Low Level Logic Input Voltage	V_{IL}	0.8	V
Loop Resistance	R_L	0 to 600	Ω
Operating Temperature Range	Topr	0 to +70	°C

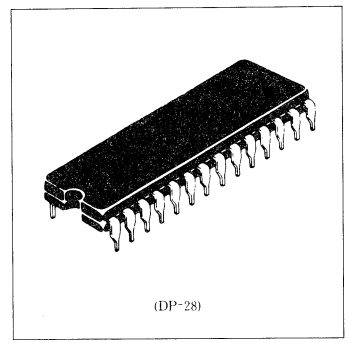
■ELECTRICAL CHARACTERISTICES (V_{BB} = −24V, V_{CC} = 5V, V_{EE} = −5V, T_a = 25°C)

Item	Test Condition	min	typ	max	Unit
On Hook Power Dissipation		−	110	180	mW
Off Hook Power Dissipation	Rloop = 200 Ω	−	750	850	mW
Off Hook Loop Current	Rloop = 200 Ω	−	29	32	mA
	Rloop = 600 Ω	−	25	−	mA
Transmission Gain	2W-4W	−	4	−	dB
	4W-2W	−	2	−	dB
Two Wire Return Loss	f = 3400Hz	25	30	−	dB
Freqency Response	200Hz to 3400Hz, 1kHz and 0dBm Signel Level	−	+0.02	+ 0.1	dB
Idle Channel Noise	2W-4W	−	−	−81.1	dBmop
	4W-2W	−	−	−81.1	dBmop
Longitudinal Balance	200Hz to 3400Hz	40	50	−	dB
PSRR	2W-4W, 4W-2W	20	30	−	dB
Relay Driver	I_{OH} = 30mA	−2.0	−	−	V

ECN1200 Series — Under Development

High Voltage Ring Switch IC for PABX Application

Series No.	Application	Main Specification
ECN1200P3	Ring Switches	Voltage : 280V Current : 70 mA

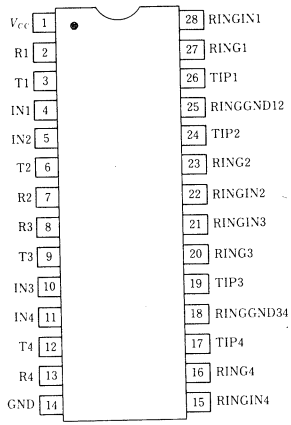

(DP-28)

■FEATURES

- High Voltage Monolithic IC by 280V Bi-CMOS Dielectric Isolation Process.
- 4-ch Ring and Line Switches with incorporated drive circuit in 28-pins DIL-P package.
- Perfect Break before Make operation between Ring Switches and Line Switches.
- CMOS compatible interface to SLIC IC.
- Prepared 4 type ICs to meet all of PABX systems (Type No. ECN1210, ECN1220, ECN1230, ECN1240)

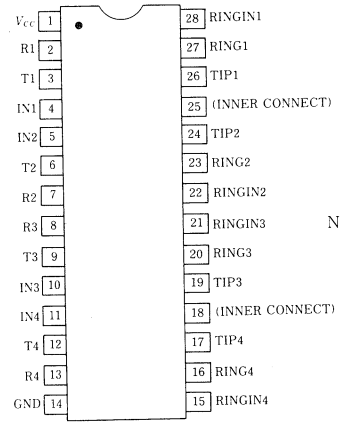
■PIN ARRANGEMENT

●ECN1210P3



(Top View)

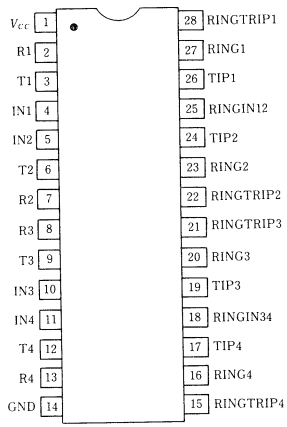
●ECN1220P3



(Top View)

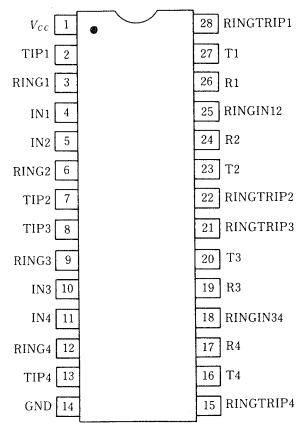
Note) Do not use pin No. 18 and 25 of ECN1220P3 as they are used for internal connection.

●ECN1230P3



(Top View)

●ECN1240P3

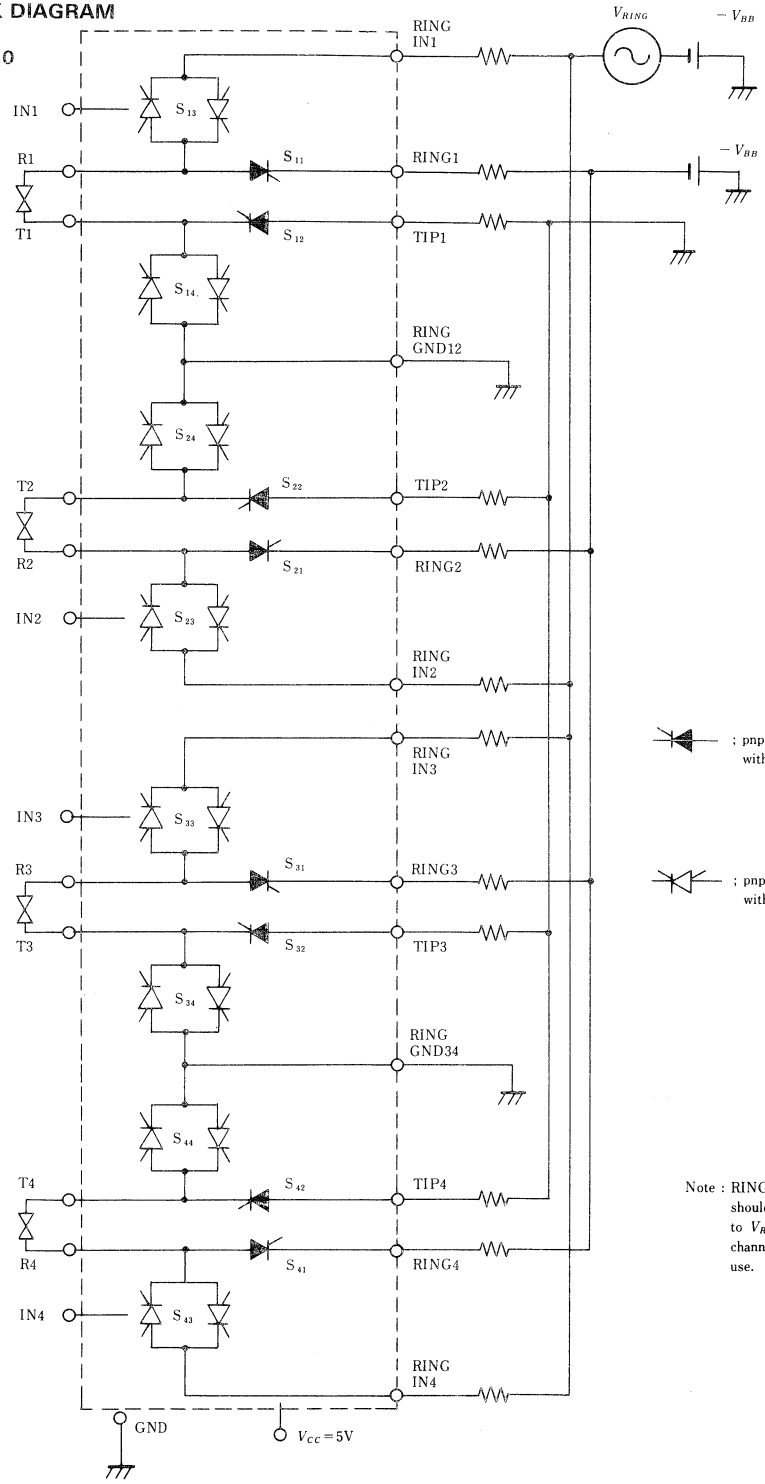


(Top View)

Note) RINGIN2 (ECN1210 and ECN1220) and RINGIN12 (ECN1230 and ECN1240) should be connected to V_{RING} even if channel 2 is not in use.

■BLOCK DIAGRAM

●ECN1210

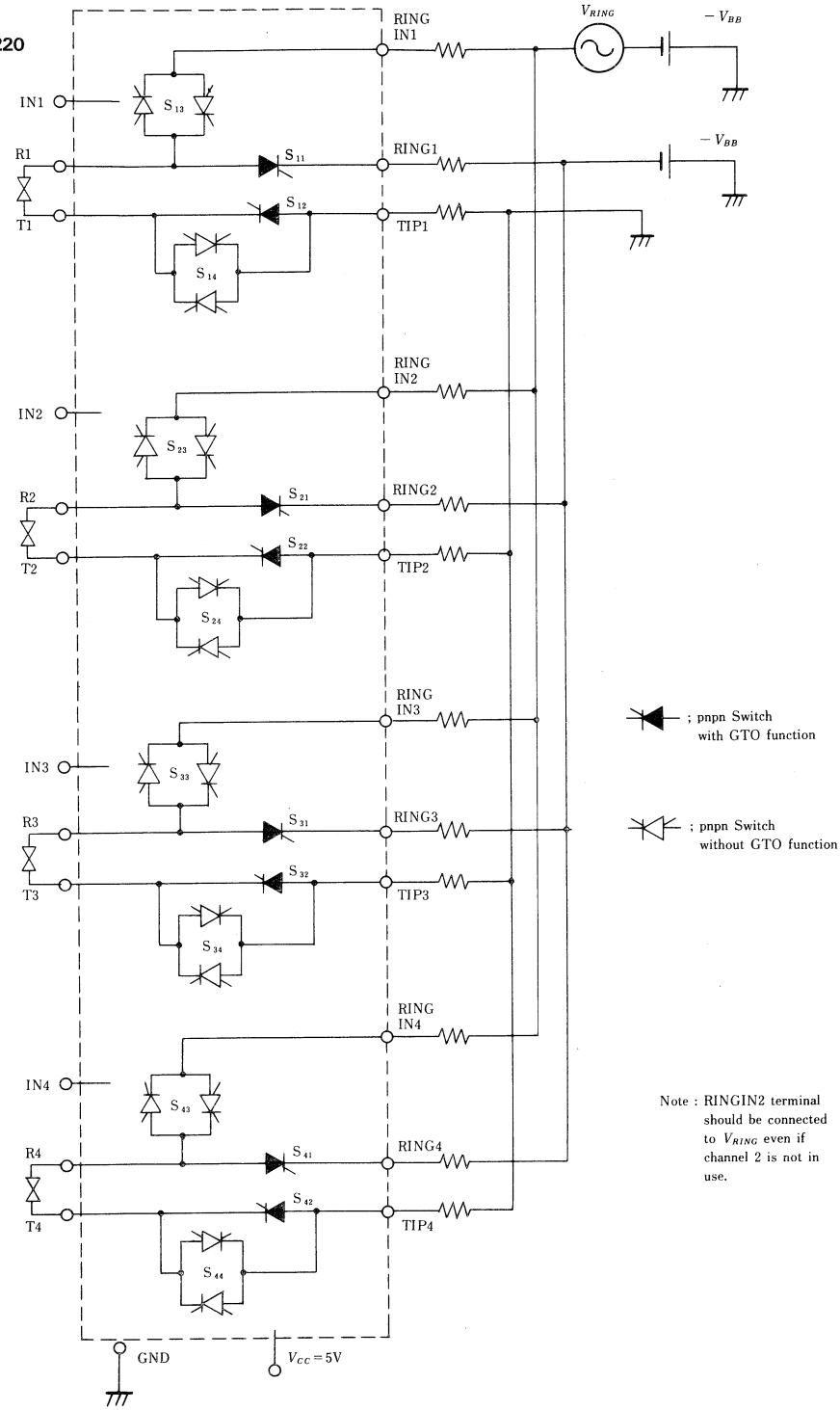


; pnpn Switch with GTO function

; pnpn Switch without GTO function

Note : RINGIN2 terminal should be connected to V_{RING} even if channel 2 is not in use.

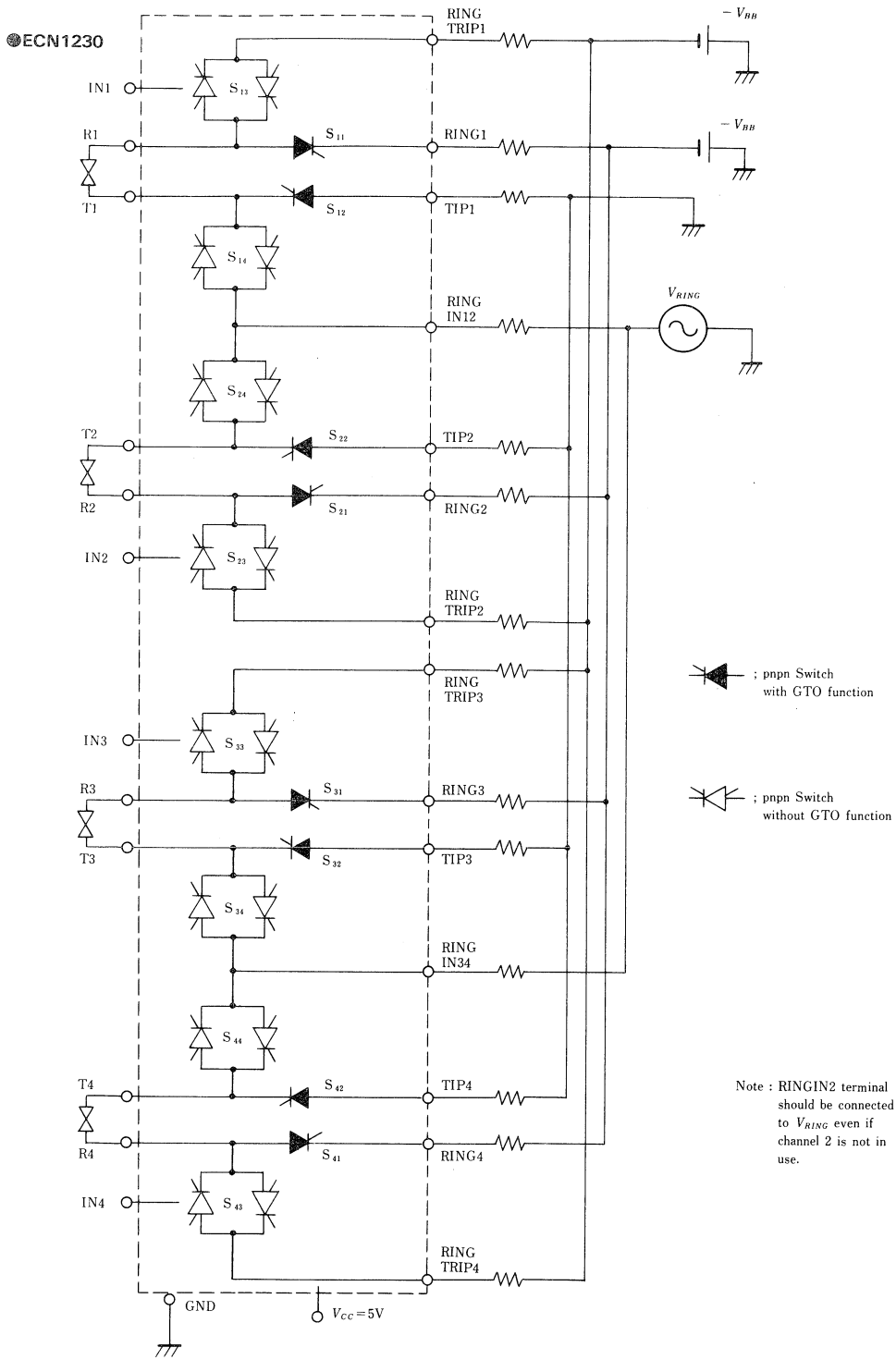
●ECN1220



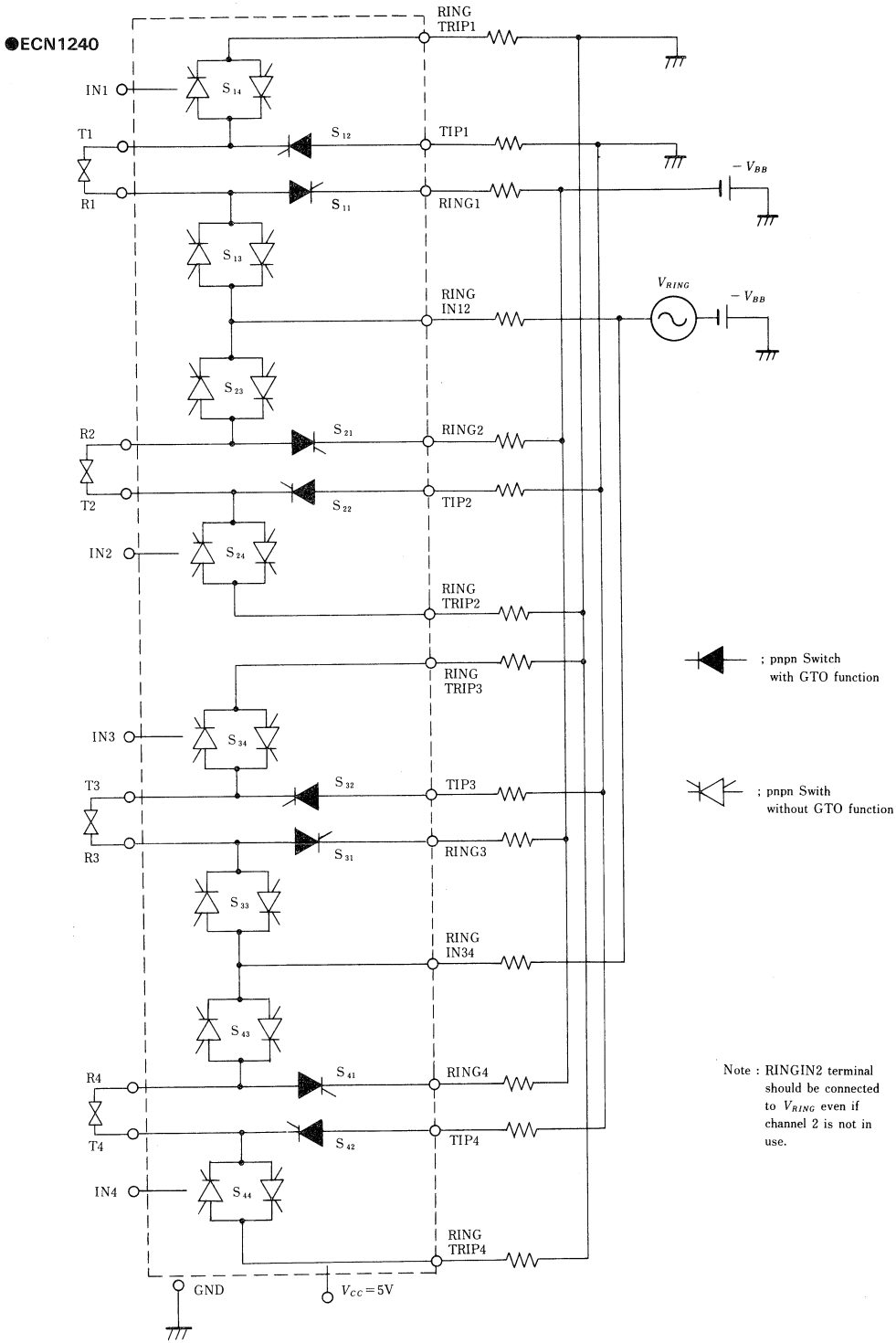
; pnpn Switch with GTO function

; pnpn Switch without GTO function

Note : RINGIN2 terminal should be connected to V_{RING} even if channel 2 is not in use.



Note : RINGIN2 terminal should be connected to V_{RING} even if channel 2 is not in use.



Note : RINGIN2 terminal should be connected to V_{RING} even if channel 2 is not in use.

■ABSOLUTE MAXIMUM RATINGS (T_a=25°C unless otherwise specified)

Items		Symbols	Ratings	Units	Notes
Controls	Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	
	Input Signal Voltage	Vin	−0.5 to V_{CC} +0.5	V	
Switches	Blocking Voltage of Switches	V_{MAX}	−280 to +280	V	R to RING, RINGIN T to TIP, RINGGND (Switch is OFF)
	Blocking Voltage between high voltage portion and control portion	V_L	−220 to +220	V	R, RING, T, TIP, and RINGIN to G
	On-state Current of Switches	I_{MAX}	70	mA_{DC}	Sn1, Sn2
			100	mA_{RMS}	Sn3, Sn4 (on-hook)
			350	mA peak	Sn3, Sn4 (off-hook Ring Trip Duration fR_{ING}=20 Hz half sine wave 0.2 sec. ON)
Power Dissipation		P_T	800 *	mW	Ta=60°C
Operating Temperature		Top	5 to 70	°C	
Storage Temperature		Tst	−55 to +125	°C	

Notes : * Derating Rate is 12 mW/°C from 60 °C to 70 °C.

■SPECIFIED OPERATING CONDITIONS (See Test Circuit A, AA)

Items	Symbols	Values	Units	Notes
Power Supply Voltage for control circuit	V_{CC}	5 ± 0.25	V	
Battery Feed Voltage	$-V_{DC}$	0 MAX. −56 MIN.	V	
Battery Feed Circuit DC Impedance	R_{AA},R_{BB}	200 MIN.	Ω	per one line
Ring Signal Voltage	V_{RING}	110 MAX.	V_{RMS}	
Telephone Equivalent Impedance	Ztel	500 MIN.	Ω	AC Impedance for ring freq. (on-hook)
		20 MIN.	Ω	DC Impedance (off-hook)

Test Circuit A : ECN1210, 1230, 1240
Test Circuit AA : ECN1220

■ELECTRICAL CHARACTERISTICS

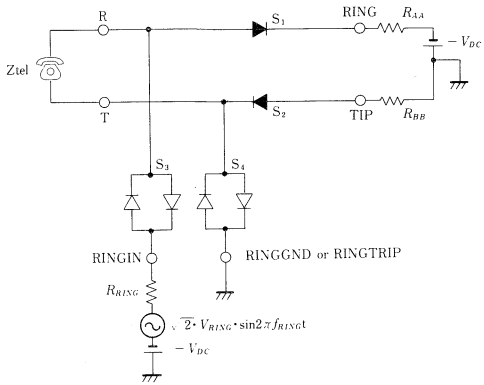
(Conditions: T_a=25°C, Test Circuit A, AA, V_{CC}=5V, $-V_{DC}$=−48V, V_{RING}=90V_{RMS}, 50Hz sine wave, R_{RING}=1000Ω, R_{AA}=R_{BB}=220Ω, $Ztel$=820Ω unless otherwise specified.)

Items	Symbols	Test Conditions	min.	typ.	max.	Units
Input Voltage	V_{IH}		3.6	–	–	V
	V_{IL}		–	–	0.7	V
Input Current	I_{IH}	V_{INDC}=4V	–	–	200	μA
	I_{IL}	V_{INDC}=0.7V	–	–	50	μA
Supply Current	I_{CC}	at Line Monitor, Ztel=open	–	–	20	mA
Cut-off Current (Sn1+Sn2)	Icutoff		70	–	–	mA
On-State Voltage (Sn1, Sn2)	V_F	I_F=30mA	–	–	1.4	V
On-State Resistance (Sn1, Sn2)	R_{ON}	(V_F[@35mA] - V_F[@25mA]) /10mA	–	–	10	Ω
Balance of R_{ON} (Sn1, Sn2)	$\triangle R_{ON}$	| R_{ON}(Sn1) - R_{ON}(Sn2) |	–	–	0.5 *	Ω
On-Driving Current (Sn1, Sn2)	I_{GON}	Test Circuit B, V_{INDC}=0.7V	–	–	1.0	mA
Off-Driving Current (Sn1, Sn2)	I_{GOFF}	Test Circuit B, V_{INDC}=4V	–	–	2.0	mA
dv/dt Capability (Sn3, Sn4)	± (dv/dt)	V_{AK}=±200V	500	–	–	V/μs
Crosstalk (reference)	Lc	EIA RS-464 Fig. 45, f=200 to 3200 Hz	75 *	–	–	dB

* Not guaranteed value but design reference value
* * n=channel number (1 to 4)

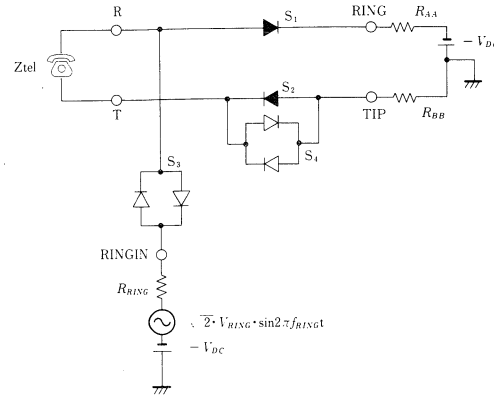
■TEST CIRCUIT

a) Test Circuit A (for ECN1210, 1230, 1240)



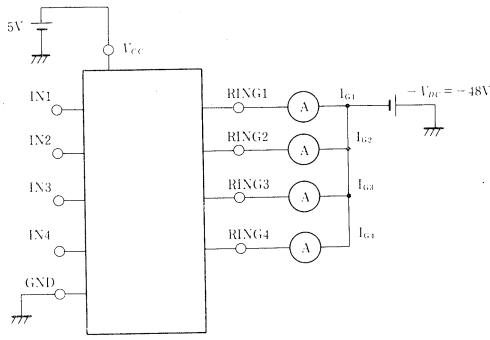
(a) Test Circuit A (for ECN1210, 1230, 1240)

b) Test Circuit AA(for ECN1220)



(b) Test Circuit AA (for ECN1220)

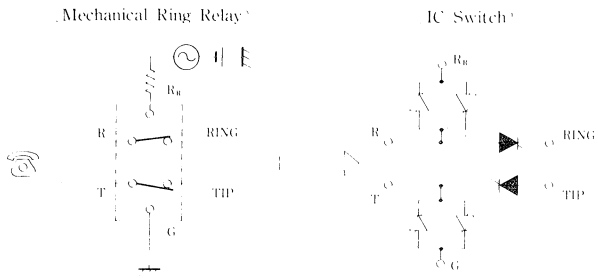
c) Test Circuit B



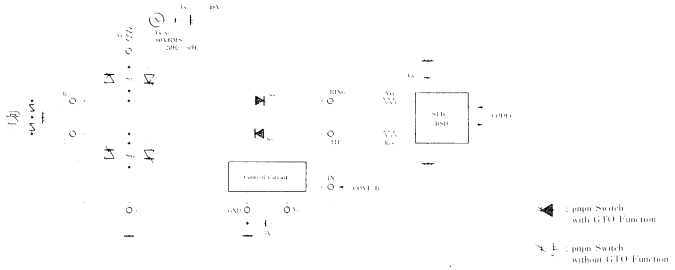
V_{INDC}	I_G
0.7V	I_{GON}
4V	I_{GOFF}

Note) Pins not indicated are open.

■FUNCTION DIAGRAM

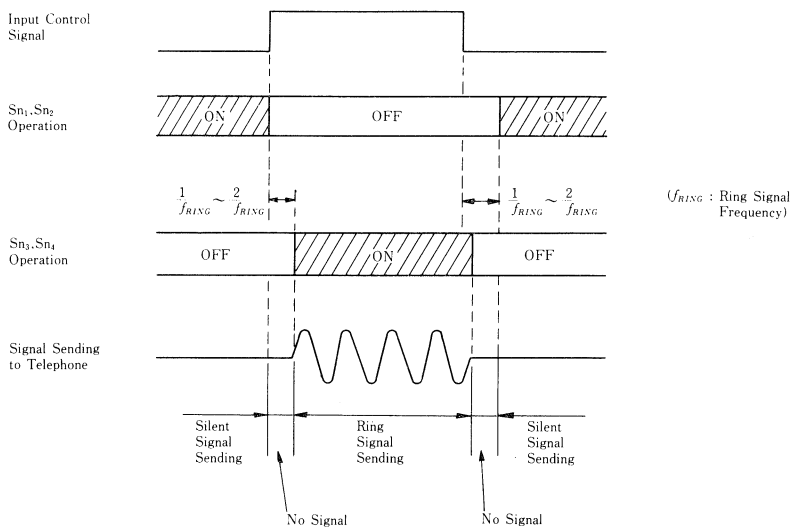


■TYPICAL CIRCUIT APPLICATION (Case of ECN1210)



Note) Varistors should be connected between T and GND, and between R and GND for over voltage protection.

■TIMING CHART OF BREAK before MAKE (BBN) OPERATION between Sn1,Sn2 and Sn3,Sn4



(f_{RING} : Ring Signal Frequency)

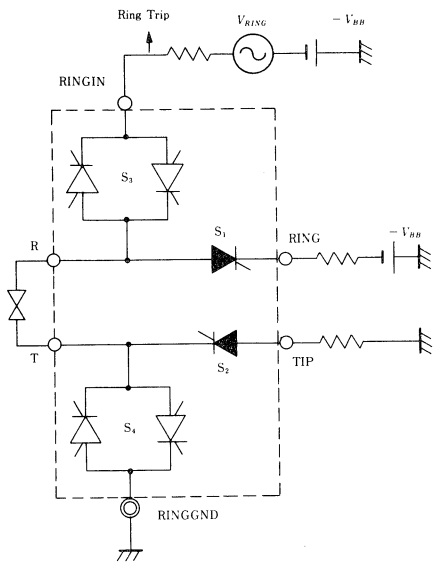
●FUNCTION TABLE

	Input Signal	Sn1, Sn2	Sn3, Sn4
Normal loop forming	L	ON	*
Ringing signal sending	H	OFF	ON

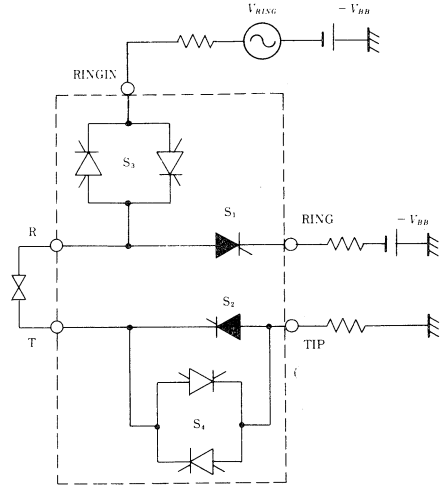
* Sn3, Sn4 turn off at zero crossing point of current.

SYSTEM CONFIGURATIONS OF ECN1200 SERIES

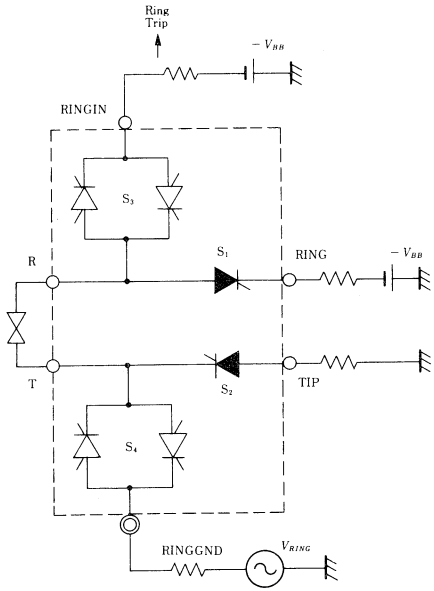
(a) ECN1210



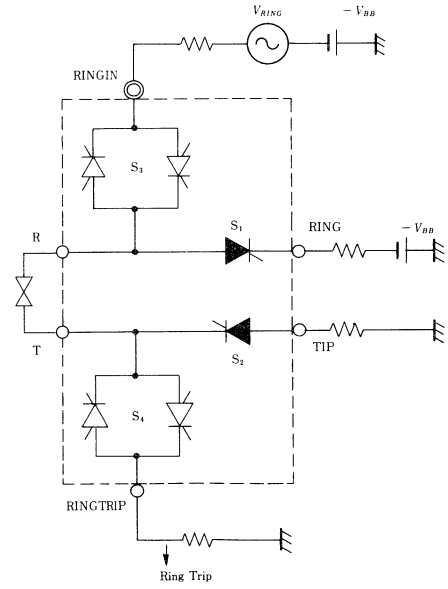
(b) ECN1220



(c) ECN1230



(d) ECN1240



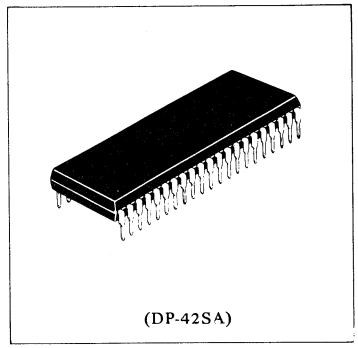
Note: Terminal indicated with @ are common for two channels.

Devices for Telephone Applications

HA12089NT — Preliminary

Sound Signal Processing for Automatic Telephone Answering System

HA12089NT is the IC designed for sound signal processing for automatic telephone answering system and has many functions and high integration in DILP shrink 42-pin package. As the device builds mainly in foundamental features necessary to the automatic answering telephone, it can construct the sound signal processing needed for automatic answering telephone on 1 chip.



(DP-42SA)

■FEATURES

- Adjustable with external frequency characteristic and each gain of LINE • REC • PB • Monitor series for wide use.
- Possible to trim AC current flowing head by external resistance because of using current drive type for OGM/ICM head change.
- High Integration
  (SW Part)
  - OGM/ICM Head Change SW circuit
  - OGM/ICM Bias SW circuit for ERASE
  - MIC/LINE Input Change SW circuit
  - PRE Amp Frequency change circuit

  (REC/PB Part)
  - PRE Amp • Buffer Amp • REC Amp
  - Power Amp • Power Mute Circuit
  - ALC circuit • ATT circuit when FF/REW

  (LINE PART)
  - Filter Amp • LINE Amp • ATT circuit when FF/REW

  (VOX Part)
  - VOX Amp • COMP Amp; (Detection Circuit)

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage*	V_{CC} (max)	7.0	V
Power Dissipation**	P_T	300	mW
Operating Temperature	Topr	−20 to +65	°C
Storage Temperature	Tstg	−55 to +125	°C

Note) * Standard operating Voltage . . . . . V_{CC}= 6.0V ± 0.5V
** Allowable value under the condition of Ta = 65°C.

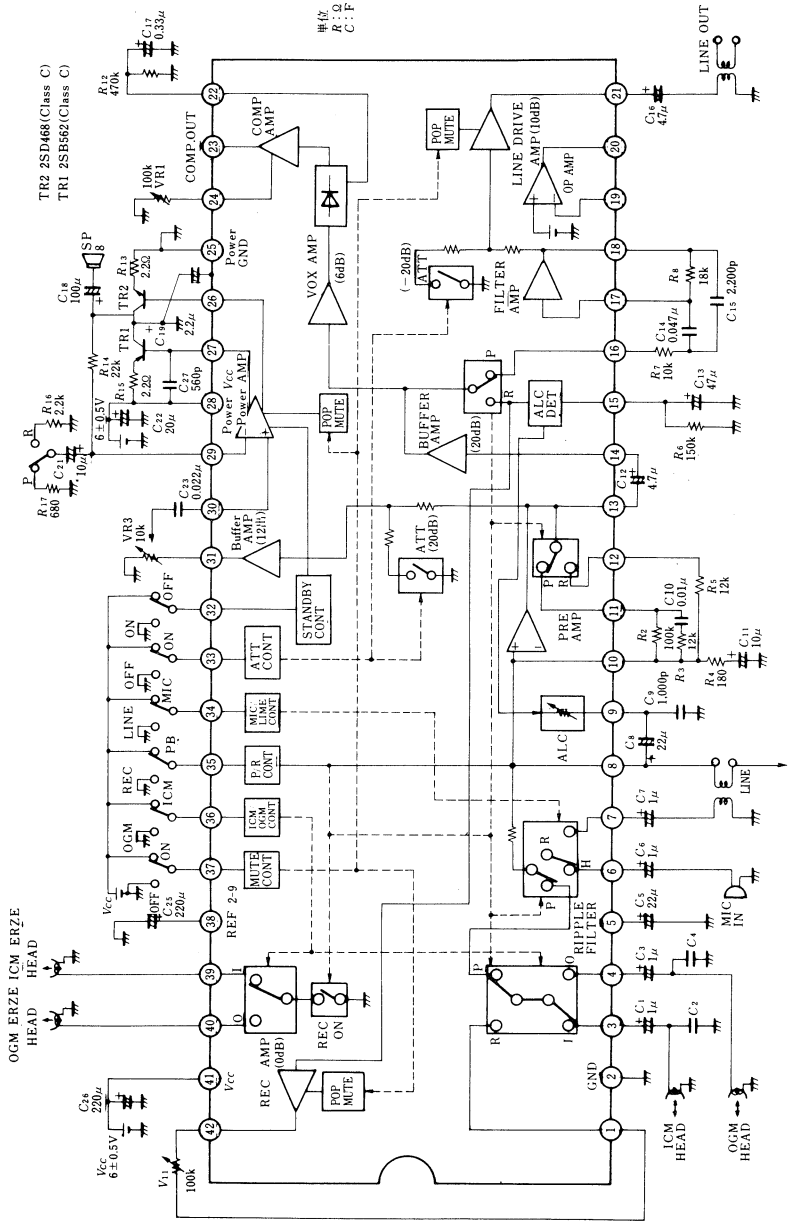


Fig. 1 Standard External Circuit and Block Diagram

■ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 6V f = 1 kHz)

Test Item	Symbol	Test Conditions	min.	typ.	max.	Unit	Application Terminal
Quiscent Current	I_Q	Pin 35 = 5V Non-signal	–	15	23	mA	㊶
PB Voltage Gain	G_V1	V_O = 0 dBm	71	74	77	dB	③ → ㉑
PB Maximum Output Voltage	$V_{om}1$	T.H.D = 10%	1.2	1.7	–	Vrms	
PB Distortion Ratio*	T.H.D1	V_O = 0 dBm	–	0.4	2.0	%	
REC Voltage Gain	G_V2	Vin = −70 dBm	51	54	57	dB	⑥ → ③
REC Maximum Input Voltage	Vim1	T.H.D ≦ 2%	–	–	−30	dBm	
REC Distortion Ratio*	T.H.D2	Vin = −50 dBm	–	0.7	2.0	%	
REC Cross Talk*	C.T1	Vin = −30 dBm	–	–	−60	dB	⑥ → ⑦
REC ALC Voltage when Operating	G_VALC	Vin = −50 dBm	−9	−6	−3	dBm	⑥ → ③
Power Voltage Gain	G_V3	PB mode 10dB ATT, V_O=0dBm	68.5	71.5	74.5	dB	③ → Power output
Power Maximum Output Voltage	Vom2	PB mode 10 dB ATT T.H.D = 10%	1.2	1.7	–	Vrms	
Power Distortion Ratio*	T.H.D3	P9 mode 10dB ATT, V_O=0dBm	–	0.6	20	%	
Power Attenuation*	ATT1	Attenuation when V_O=0dBm, Pin 37=5V PB mode	–	–	−50	dB	
Comparator Output Voltage	V_{OH}	Pin 24 = 1.9V, REC mode Vin = −60 dBm	3.8	–	5.0	V	㉓
Comparator Output Voltage	V_{OL}	Pin 24=1.9V, REC mode Non signal	−0.3	–	0.5	V	
Control Input Voltage	V_{IH}	Lo Mode → Hi Mode Change Voltage	3.8	–	V_{CC}	V	㉜ to ㊲
Control Input Voltage	V_{IL}	Hi Mode → Lo Mode Change Voltage	0	–	0.5	V	

* B P.F in 400 Hz to 15 kHz.

■TEST CIRCUIT

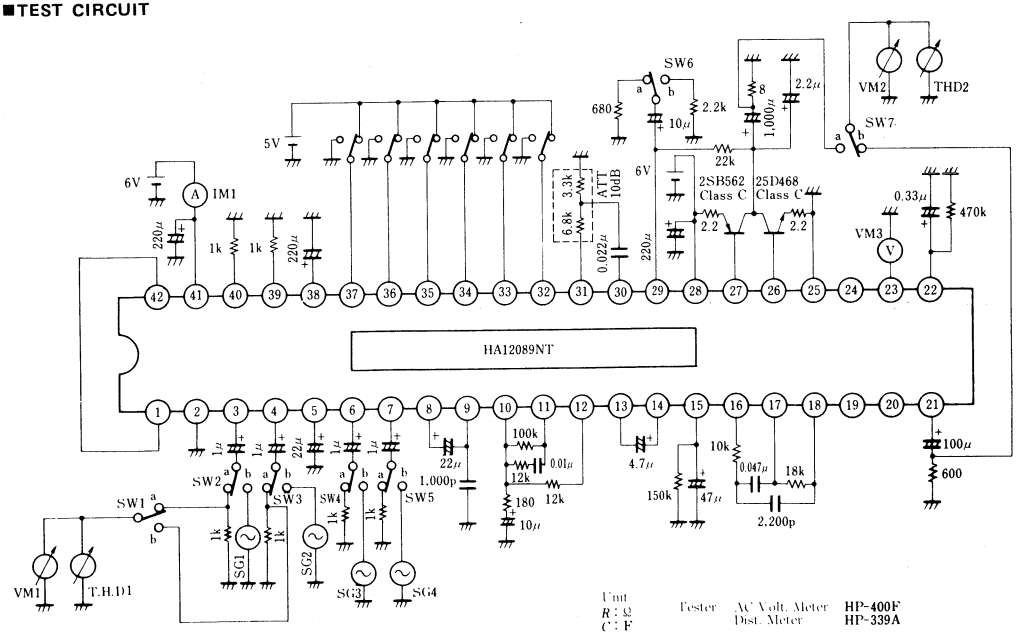
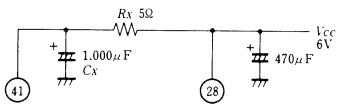


Table 1 Switch Position List

Symbol	Control Terminal						SW Position							Signal so and Instruction
	32	33	34	35	36	37	SW1	SW2	SW3	SW4	SW5	SW6	SW7	
I_Q	L	L	L	H	L	L	a	a	a	a	a	a	a	IM1
G_V1	H	L	L	H	H	L	a	b	a	a	a	a	b	SG1, VM2
Vom1	H	L	L	H	H	L	a	b	a	a	a	a	b	
T.H.D1	H	L	L	H	H	L	a	b	a	a	a	a	b	SG1, T.H.D2
G_V2	H	L	H	L	H	L	a	a	a	b	a	b	a	SG3, VM1
Vim1	H	L	H	L	H	L	a	a	a	b	a	b	a	
T.H.D2	H	L	H	L	H	L	a	a	a	b	a	b	a	SG3, T.H.D1
C.T1	H	L	L	L	H	L	a	a	a	b	a	b	a	SG3, VM1
G_V-ALC	H	L	H	L	H	L	a	a	a	b	a	b	a	SG3, T.H.D1
G_V3	H	L	L	H	L	L	a	b	a	a	a	a	a	SG1, VM2
Vom2	H	L	L	H	L	L	a	b	a	a	a	a	a	
T.H.D3	H	L	L	H	L	L	a	b	a	a	a	a	a	SG1, T.H.D2
ATT1	H	L	L	H	L	H	a	b	a	a	a	a	a	SG1, VM2
V_{OH}	H	L	H	L	L	L	a	a	a	b	a	b	a	SG3, VM3
V_{OL}	H	L	H	L	L	L	a	a	a	a	a	b	a	
V_{IH}	H	H	H	L	H	H	a	a	a	a	a	b	a	——
V_{IL}	L	L	L	L	L	L	a	a	a	a	a	b	a	——

■NOTE

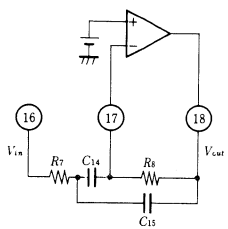
1. This IC is two supply voltage pins; (28), (41) pin and two GND terminal pins; (2), (25) pin. Prevent signal from the supply source of another block by applying supply voltage to power (28) pin and small signal (41) pin respectively. Distortion ratio may become worse by the signal from the supply source of another block.



In the case of single supply voltage of power and small signal, for example, avoid the signal from the supply source of power block to small signal one, by connecting wiring as shown below.

Take care of keeping 5.5V or more voltage of (41) pin by reducing Rx as much possible.

2. Determine the filter constant of (16), (17), (18) pin as shown below.



$$\frac{Vout}{Vin} = T(s) = \frac{-\frac{1}{R_7 C_{14}} S}{S^2 + \frac{1}{R_8}\left(\frac{1}{C_{14}} + \frac{1}{C_{15}}\right) S + \frac{1}{C_{14} C_{15} R_7 R_8}}$$

Cut-off frequency is shown below to use as a band path filter.

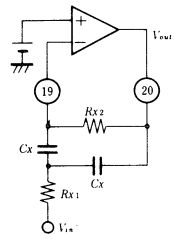
$$\omega H = \frac{\frac{1}{C_{14}} + \frac{1}{C_{15}}}{2R_8}\left(1 + \sqrt{1 - \frac{4R_8}{R_7\left(2 + \frac{C_{14}}{C_{15}} + \frac{C_{15}}{C_{14}}\right)}}\right)$$

$$\omega L = \frac{\frac{1}{C_{14}} + \frac{1}{C_{15}}}{2R_8}\left(1 - \sqrt{1 - \frac{4R_8}{R_7\left(2 + \frac{C_{14}}{C_{15}} + \frac{C_{15}}{C_{14}}\right)}}\right)$$

For example cut-off frequency is f_H = 3.6 kHz, f_L = 650 Hz under the condition of R_7 = 10 kΩ, R_8 = 18 kΩ, C_{14} = 0.047μF and C_{15} = 2200 pF.

3. Example of using (19), (20) Additional Amp.

$$\frac{Vout'}{Vin'} = \frac{\frac{1}{C_x R_{x1}} S}{S^2 - \frac{2}{C_x R_{x2}} S + \frac{1}{C_x R_x 1 R_{x2}}}$$



The resonance frequency; ω_0, the band width; B and the Q are shown below

$$\omega_0 = \frac{1}{C_x\sqrt{R_{x1}R_{x2}}},\ BW = \frac{\omega_0}{Q} = \frac{2}{C_x R_{x2}},$$

$$Q = \frac{1}{2}\sqrt{\frac{R_{x2}}{R_{x1}}}$$

The gain under the condition of the resonance frequency; ω_0 is shown below.

$$\left|\frac{Vout'}{Vin'}\right|_{s=j\omega_0} = \frac{R_{x2}}{2R_{x1}}$$

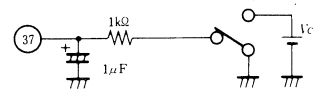
For example, the following constant can be set to construct the resoance filter under the condition of ω_0 = 1 kHz.

C_x = 0.0015 μF R_{x1} = 10 kΩ R_{x2} = 1 MΩ

Q = 5 RW = 200 Hz G_v (f = 1 kΩ) = 50

4. When controlling (32), (33), (34), (35), (36) and (37) pin, Put the time constant circuit to avoid pop noise.

(For Example)



Select the time constant according to application

5. Power block is designed with our Power transistor 2SD468, 2SB562C grade. Use the power transistor which has small deviation of V_{BE} to reduce the deviation of idling current.

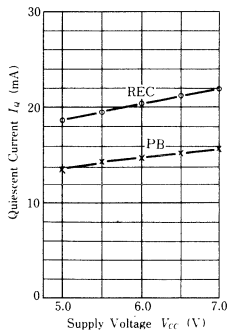
■EXTERNAL COMPONENT

Part No.	Standard Value	Feature	Influence	
			Standard Value or less	Standard Value or more
C1	1μF	DC CUT	–	–
C2				
C3	1μF	DC CUT	–	–
C4				
C5	22μF	Ripple Filter	Ripple Rejection Ratio becomes worse	–
C6	1μF	DC CUT	–	–
C7	1μF	DC CUT	–	–
C8	22μF	DC CUT	Frequency Characteristics become worse	Rising of AGC becomes slow
C9	1000pF	Oscillation Stop	ALC Circuit Oscillation	Frequency characteristics become worse
C10	0.01μF	High Cut-off Frequency	Small Cut-off Frequency	Large Cut-off Frequency
C11	10μF	Low Cut-off Frequency	Large Cut-off Frequency	Small Cut-off Frequency
C12	4.7μF	DC CUT	Breaking off when attacking	–
C13	47μF	ALC Time Constant	Distortion ratio becomes worse	Long attack recovery time
C14	0.047μF	Filter Time Constant	See Note.	
C15	2200pF			
C16	4.7μF	DC CUT	–	–
C17	0.33μF	Detection Circuit	Unstability of comparator operating	Delay of comparator response
C18	100μF	DC CUT	Frequency characteristics become worse	–
C19	2.2μF	Phase compensation	Power Amp Oscillation	Frequency characteristics become worse
C20	Missing number			
C21	10μF	Low Cut-off Frequency	Small cut-off frequency	Large cut-off frequency
C22	220μF	Supply voltage ripple rejection	Ripple rejection ratio becomes worse	–
C23	0.022μF	DC CUT	Small cut frequency	–
C24	Missing number			
C25	220μF	Ripple filter	Ripple rejection ratio becomes worse	–
C26	220μF	Supply voltage ripple rejection	Ripple rejection ratio becomes worse	–
C27	560pF	Stop of oscillation	Power oscillation	Small cut-off frequency

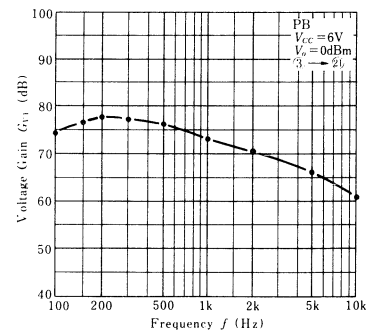
■EXTERNAL COMPONENT (Cont'd)

Part No.	Standard Value	Function	Influence	
			Standard Value or less	Standard Value or more
R1	Missing Number			
R2	100kΩ	PB Gv	Small Gv	Large offset value of pin (31)
R3	12k	PB Gv	Small Gv	Large Gv
R4	180	Pre. amp. Gv	Large Gv	Small Gv
R5	12k	REC Gv	Small Gv	Large Gv
R6	150k	ALC Time Constant	Short attack recovery time	Long attack recovery time
R7	10k	Filter Amp Gv	Small Gv	Large Gv
R8	18k	Filter Amp Gv	Small Gv	Large off-set voltage of pin (21)
R9-11	Missing Number			
R12	470k	Detection Circuit	Unstability of comparator operating	Delay of comparator response
R13,15	2.2Ω	External Tr idling current	Large idling current	Small power output
R14	22k	Power Gv	Small Gv	Large off-cut
R16	2.2k	REC Power Gv	Large Gv	Small Gv
R17	680	PB Power Gv	Large Gv	Small Gv

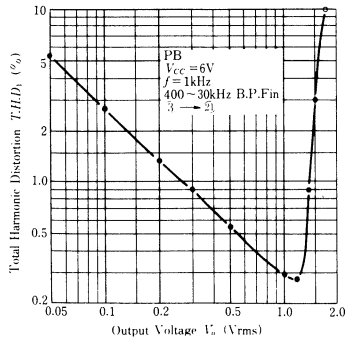
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



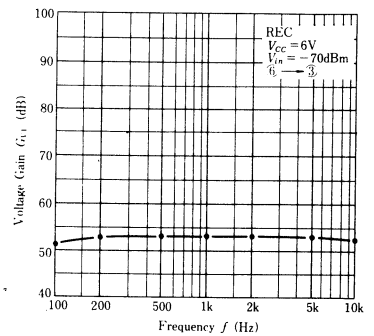
POWER GAIN vs. FREQUENCY (PB)



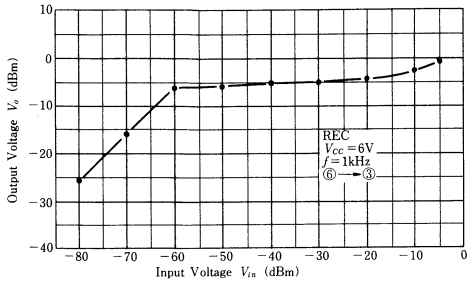
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE (PB)



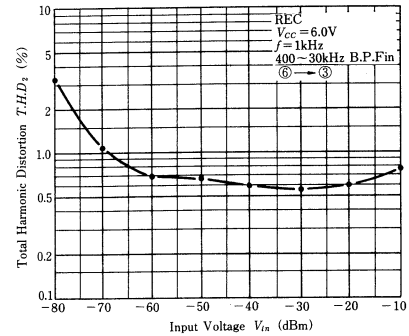
VOLTAGE GAIN vs. FREQUENCY (REC)



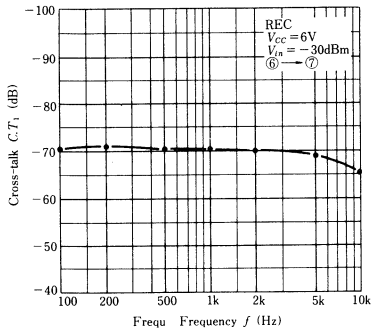
OUTPUT VOLTAGE VS. INPUT VOLTAGE (REC)



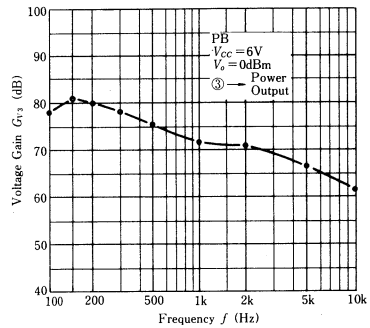
TOTAL HARMONIC DISTORTION VS. INPUT VOLTAGE (REC)



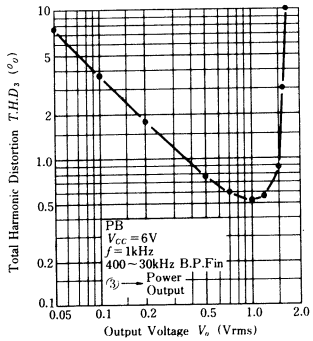
CROSS-TALK VS. FREQUENCY (REC)



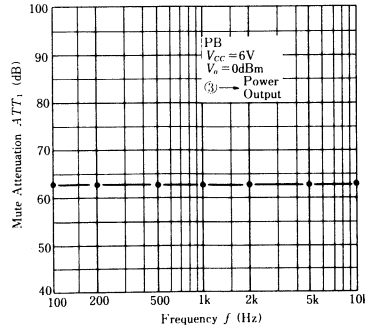
VOLTAGE GAIN VS. FREQUENCY (PB)



TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE (PB)



MUTE ATTENUATION VS. FREQUENCY



HA16802PS, HA16804PS, HA16805PS

Preliminary

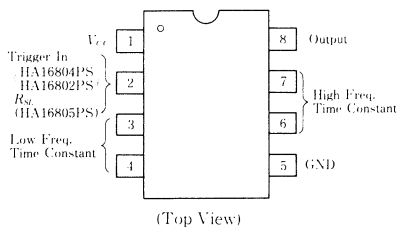
Tone Ringer IC for Telephone

The HA16802PS, HA16804PS and HA16805PS are tone ringer monolithic IC's for telephone. These IC's have a built-in regulator power supply and occur electronic sound by directly driving external magnetic speaker or piezo-electric buzzer when call signal is detected. The HA16802PS, HA16804PS and HA16805PS each have different additional functions and control the functions by control terminal.

■FEATURES

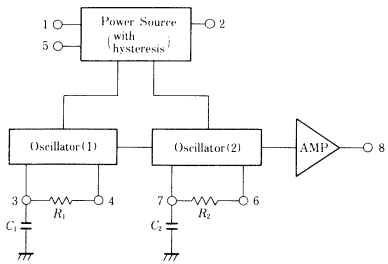
- Output frequency is variable.
- Power dissipation is low.
- As it has a regulator power source with hysteresis, it can prevent a resonance which occurs in case of parallel connection (branch) of telephone.
- 2 levels of supply initiation voltage can be selected (HA16802PS).
- Supply initiation voltage is variable. (HA16804PS)
- Supply initiation current is variable. (HA16805PS)

■PIN ARRANGEMENT



(Top View)

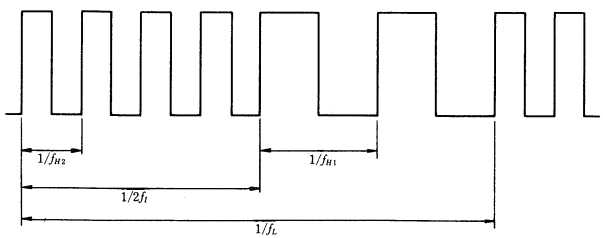
■BLOCK DIAGRAM



Note: R_1, R_2, C_1, C_2 are external parts

- Oscillator (1) operated at about 10 Hz (f_L) and modulates the frequency of Oscillator (2) at this cycle.
- Oscillator (2) operated at a high frequency and has two oscillation frequency; f_{H1}, f_{H2} by Oscillator (1).

$f_L = 1/1.25\ R_1 C_1$ $f_{H1} = 1/1.35\ R_2 C_2$ $f_{H2} = 1.24 f_{H1}$ [Hz]



HITACHI

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_S	40	V
Output Current	I_O	12	mA
Power Dissipation	P_T	625	mW
Operating Temperature Range	Topr	−20 to +70	°C
Storage Temperature Range	Tstg	−55 to +125	°C

■ELECTRICAL CHARACTERISTICS (Ta=25°C)

●HA16802PS

Item	Symbol	Condition	min.	typ.	max.	Unit	Remarks
Supply Initiation Voltage	Vsi	The contents within ( ) are the value at the time of changing (Trigger in=GND)	17 (21)	19 (23)	21 (25)	V	Selectable
Supply Initiation Current	Isi		0.6	1.2	2.5	mA	
Sustaining Voltage	Vsus		9	11	–	V	
Sustaining Current	Isus	V_S=15V	0.5	1.0	2.0	mA	
Output "H" Voltage	V_{OH}	V_S=24V, I_{OH}=−10mA	20	21.5	22.5	V	
Output "L" Voltage	V_{OL}	V_S=24V, I_{OL}=10mA	0	1.0	2.0	V	
Output Frequency	f_L	C_1=0.47μF, R_1=160kΩ	9.3	10.4	11.5	Hz	
	f_{H1}	C_2=6800pF	495	–	606	Hz	
	f_{H2}	R_2=200kΩ	610	–	752	Hz	

●HA16804PS

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply Initiation Voltage	Vsi		17	19	21	V
Supply Initiation Current	Isi		1.5	3.1	6.2	mA
Sustaining Voltage	Vsus		9	11	–	V
Sustaining Current	Isus	V_S=15V	0.5	1.0	2.0	mA
Output "H" Voltage	V_{OH}	V_S=24V, I_{OH}=−10mA	20	21.5	22.5	V
Output "L" Voltage	V_{OL}	V_S=24V, I_{OL}=10mA	0	1.0	2.0	V
Output Frequency	f_L	C_1=0.47μF, R_1=160kΩ	9.3	10.4	11.5	Hz
	f_{H1}	C_2=6800pF	495	–	606	Hz
	f_{H2}	R_2=200kΩ	610	–	752	Hz

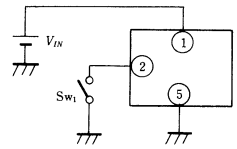
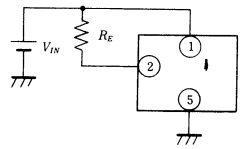
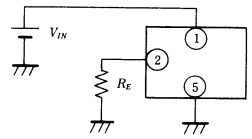
●HA16805PS

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply Initiation Voltage	Vsi	Connect with R_{SL}=20kΩ	26	28	30	V
Supply Initiation Current	Isi		0.7	1.5	3.0	mA
Sustaining Voltage	Vsus		9	11	–	V
Sustaining Current	Isus	V_S=15V, Connect with R_{SL}=20kΩ	0.5	1.0	2.0	mA
Output "H" Voltage	V_{OH}	V_S=36V, I_{OH}=−10mA	32	–	36	V
Output "L" Voltage	V_{OL}	V_S=36V, I_{OL}=10mA	0	1.0	2.0	V
Output Frequency	f_L	C_1=0.47μF, R_1=160kΩ	9.3	10.4	11.5	Hz
	f_{H1}	C_2=6800pF	495	–	606	Hz
	f_{H2}	R_2=200kΩ	610	–	752	Hz

■PIN ARRANGEMENT

Pin No.	Pin Name	Function	
1	Vcc	Positive Power Supply	
2	TRIGGER IN	HA 16802 HA 16804	Shown below
	R_{SL}	HA 16805	
3 4	LOW FREQ. TIME CONSTANT	Low Frequency Time Constant Setting	
5	GND	Negative Power Supply	
6 7	HIGH FREQ. TIME CONSTANT	High Frequency Time Constant Setting	
8	OUTPUT	Tone Output	

TRIGGER IN TERMINAL
R_{SL} } **② Pin Function Description**

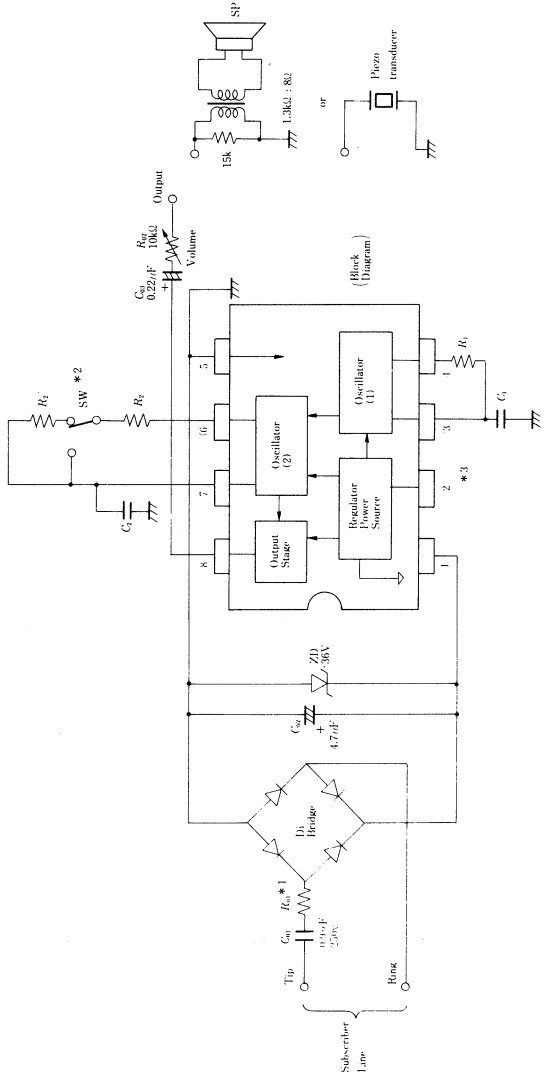
Type Name	Function	Description
HA16802PS	Supply Initiation Voltage Variable (Vsi)	
HA16804PS	Supply Initiation Voltage Variable	
HA16805PS	Supply Initiation Current Variable (Isi)	

② Pin Condition	Vsi
Open (Sel : OFF)	19V typ.
GND (Swl : ON)	23V typ.

R_E	Vsi
Open	19V typ.
1MΩ	17V typ.
500kΩ	15V typ.

R_E	Isi
6.3k	3.2mA typ.
13k	2mA typ.
20k	1.2mA typ.

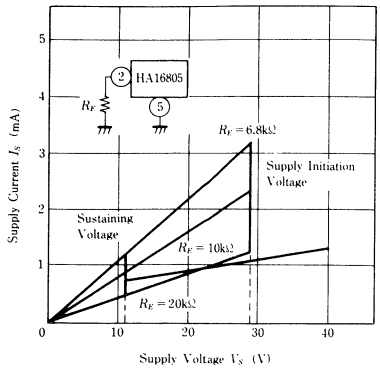
■APPLICATION



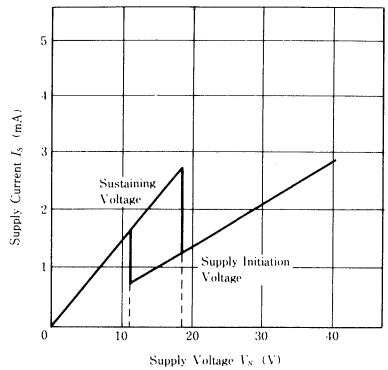
Note *1 HA16802PS, HA16805PS : 10kΩ
HA16804PS : 2kΩ
*2 Possible timbre adjustment by changing the resistance value of R_2
*3 Additional function control terminal

Tone Ringer Application Circuit Example

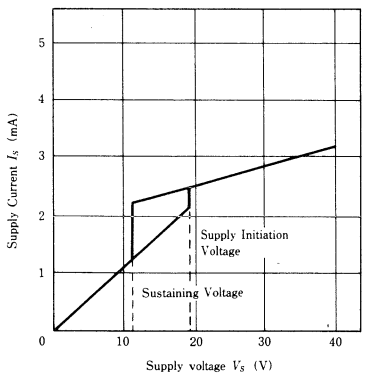
HA16805 Supply Voltage vs. Supply Current Characteristic.



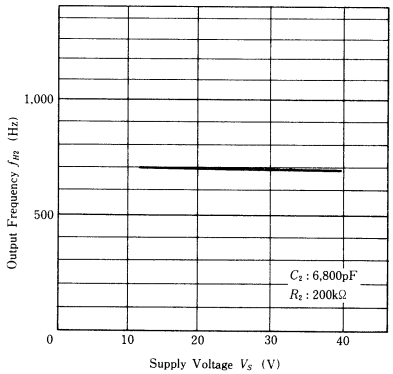
HA16804 (at Pin 2 Open) Supply Voltage vs. Supply Current Characteristic



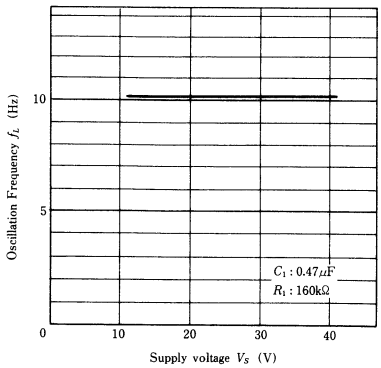
HA16802 (at Pin 2 Open) Supply Voltage vs. Supply Current Characteristic



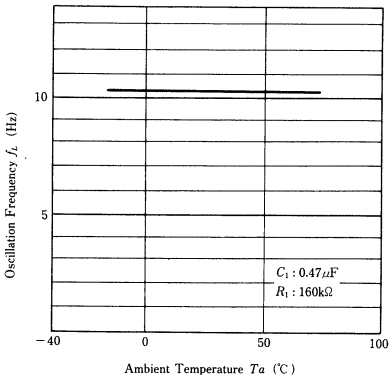
Output Frequency vs. Supply Voltage Characteristic



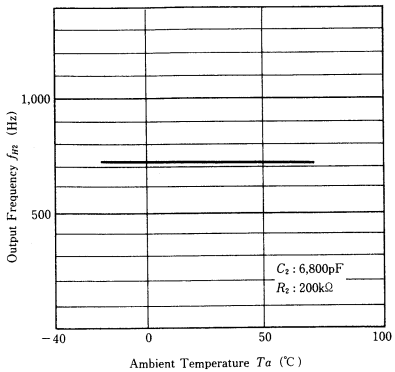
Oscillation Frequency vs. Supply Voltage Characteristic



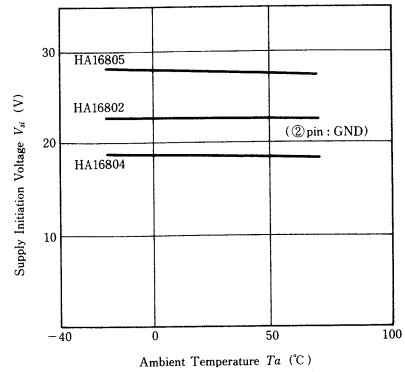
Oscillation Frequency vs. Ambient Temperature Characteristic



Output Frequency vs. Ambient Temperature Characteristic



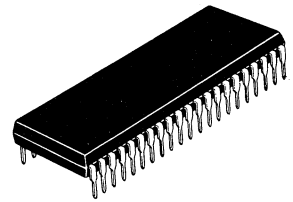
Supply Initiation Voltage vs. Ambient Temperature Characteristic



HA16808NT — Under Development

Telephone Speech Circuit with Tone Ringer

The device is a single chip monolithic IC containing Telephone Speech Network, Tone Ringer, Speaker Amp and others.



(DP-42SA)

■FEATURES

- Capable of low voltage operation . . . 1.8V typ.
- Automatic Gain control to compensate for line attenuation.
- DTMF interface with Muting (V_{DD}, MUTE, MF Amp).
- Speaker Amp.
- Noise Suppression.
- Interface for melody in holding (V_{DD}, Holding Tone Amp).
- Variable Oscillation Frequency for Tone Ringer.
- Prevent resonance due to telephone branching.
- Low Power Dissipation.

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Line Voltage *	V_L	20	V
Line Current	I_L	120	mA
Tone Ringer Input Voltage	V_{RIN}	30	V
Power Dissipation	P_T	950	mW
Operating Temperature	Topr	−20 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C

* 3ms Pulse duration

■ELECTRICAL CHARACTERISTICS

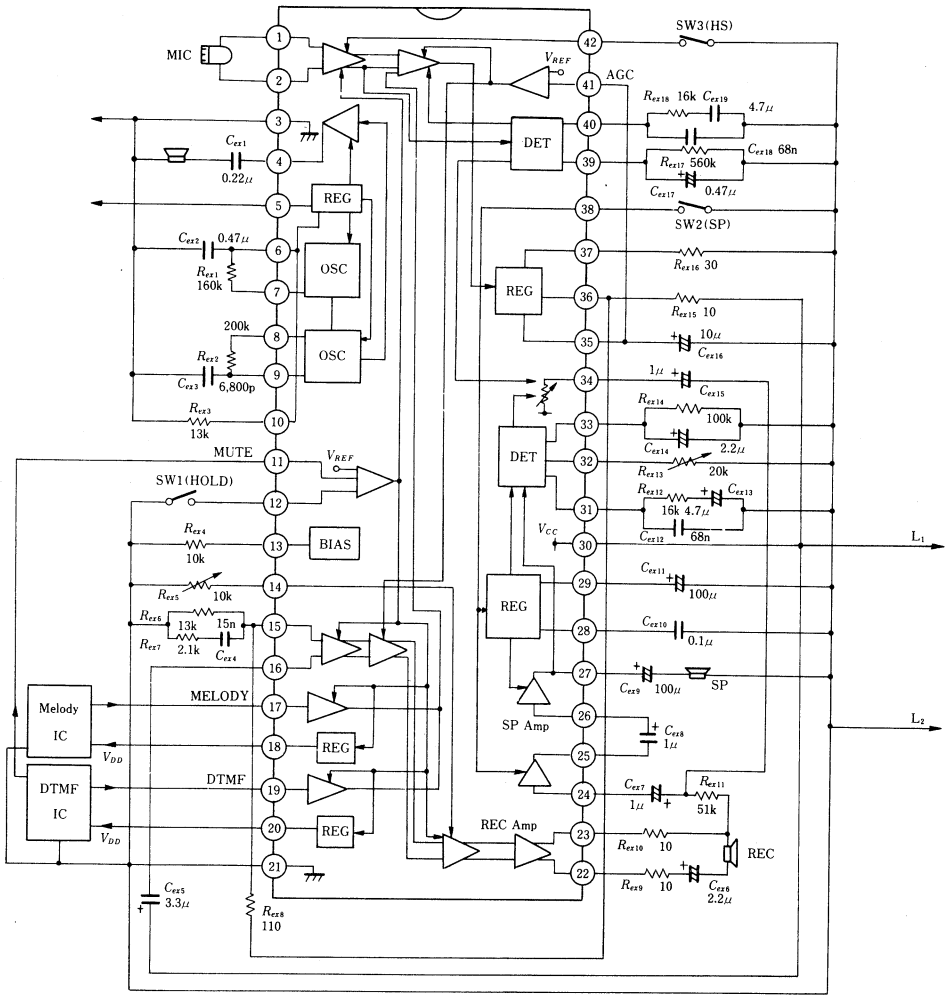
●Speech Circuit Section

Item	Symbol	Condition	min	typ	max	Unit
Line Voltage	V_L	I_L=10mA	−	1.8	−	V
		I_L=20mA	2.3	−	2.8	V
		I_L=50mA	−	5.6	−	V
Transmitting Gain	Gs	I_L=30mA	49	51	53	dB
		I_L=80mA	43	45	47	dB
Microphone Input Impedance	Z_{MIN}		40	−	−	kΩ
Receiving Gain	G_R	I_L=30mA	−7	−5	−3	dB
		I_L=80mA	−13	−11	−9	dB
Side Tone	SDT		−	−	36	dB
Line Matching Impedance	Z_L	f=1kHz	500	600	700	Ω
Speaker Amp Gain	Gsp	I_L=30mA	5	−	12	dB

●Tone Ringer Section

Item	Symbol	Condition	min	typ	max	Unit
Threshold Voltage	Vth		17	19	21	V
Voltage to keep on ringing	Vs		9	11	−	V
"L"Output Voltage	V_{OL}	I_{OL}=−10mA V_{IN}=24V	−	−	2	V
"H" Output Voltage	V_{OH}	I_{OH}=10mA V_{IN}=24V	20	−	−	V
Average Output Frequency	f avg	R_1=165kΩ C_1=0.47μF R_2=190kΩ C_2=6800pF	−	625	−	Hz

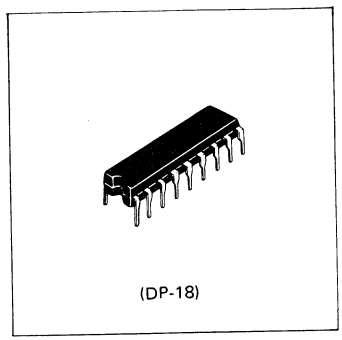
■BLOCK DIAGRAM



Unit R : Ω
C : F

HD61825A/B

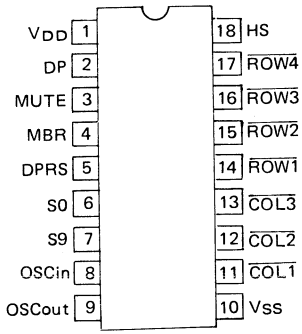
Pulse Dialer with Redial



■ FEATURES

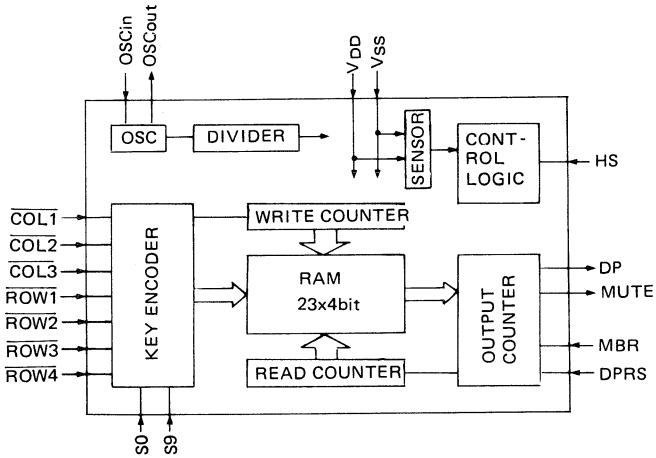
- Direct telephone-line operation.
- Low power and low voltage operation by CMOS process.
- Uses either a standard 2-of-7 keyboard or the inexpensive matrix keyboard
- Stable operation by using ceramic resonator.
- Make/Break ratio pin-selectable
- 10 pps/20 pps pin-selectable
- Redial function (# key)
- Pause input (# key)
- Selectable of mute output
  - Mute (continuous) HD61825A
  - Mute (each digit) HD61825B
- 0 dialing in inhibition pin
  9 dialing in inhibition pin
- 23-digit dial memory
- Dial memory overflow protection (inhibit redial)
- On chip power supply voltage sense circuit
  - Reset voltage
  - Memory clear voltage

■ PIN ASSIGNMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Vss= 0V)

Item	Symbol	Value	Unit
Power supply voltage	V_{DD}	5.5	V
Terminal voltage	V_T	V_{SS} −0.3 to V_{DD} + 0.3	V
Operating temperature	Topr	−20 to +75	°C
Storage tmperature	Tstg	−55 to +125	°C

▪ ELECTRICAL CHARACTERISTICS

• DC Characteristics (Vss = 0V, V_{DD} = 2.0 to 5.0V, Ta = −20 to +75°C)

Item	Symbol	Test condition	min.	typ.*1	max.	Unit
Operating voltage	V_{DD}		1.7	–	5.0	V
Reset voltage	V_{DR}		–	1.5	–	V
Memory clear voltage	V_{DC}		–	1.15	–	V
Operating current	I_{DD}		–	170	–	μA
Memory hold (reset) current	I_{DR}		–	0.5	–	μA
Input High voltage	V_{IH}	except HS pin	80%V_{DD}	–	–	V
Input High voltage	V_{IH}	HS pin V_{DD} = 3.0 to 5.0V	90%V_{DD}	–	–	V
Input High voltage	V_{IH}	HS pin V_{DD} = 2.0 to 3.0V	V_{DD}−0.1	–	–	V
Input Low voltage	V_{IL}	HS pin V_{DD} = 2.0 to 5.0V	–	–	20%V_{DD}	V
Input Low voltage	V_{IL}		–	–	20%V_{DD}	V
Input leak current	$\|I_{IN}\|$	Pull up MOS off, V_{IN}=0 to V_{DD}	–	–	1	μA
Input Pull up MOS current	$-I_P$	V_{IN} = 0, ($\overline{MBR}$ $\overline{DPRS}$ S0 S9 $\overline{ROW}$, $\overline{COW}$, HS)	–	10	–	μA
Output High voltage	V_{OH}	$-I_{OH}$ = 0.1 mA (DP, MUTE)	V_{DD}−0.5	–	–	V
Output Low voltage	V_{OL}	I_{OL} = 0.1 mA ($\overline{ROW}$, $\overline{COL}$)	–	–	0.3	V
Open drain output leak current	I_{OL}	V_{IN} = V_{DD} (DP, MUTE)	–	–	1	μA

• AC CHARACTERISTICS (Vss = 0V, V_{DD} = 2.0 to 5.0V, Ta = −20 to +75°C)

Item	Symbol	Test condition	min.	typ.*1	max.	Unit
Oscillation frequency	fosc		396	400	404	kHz
Oscillation start up time	t_{str}		–	5	–	ms

*1 Typ. value is the design value (the standard value at V_{DD} = 2.5V and Ta = 25°C)

▪ DESCRIPTION

HD61825 is a CMOS IC for button telephone and converts keyboard inputs into the dial pulse signal. Using low-voltage and low-power consumption CMOS process, it can operate directly from the telephone line and interfaces with the telephone line by loop-disconnect signal (DP output). Besides, it has MUTE output to mute the receiver during the sending pulses. In the HD61825, ON HOOK/OFF HOOK is detected by the HS pin.

Further, while the supply voltage is less than reset voltage, even if the HS is OFF HOOK, the HD61825 will be ON HOOK state of inhibition key input. When the power supply voltage is less than memory clear voltage, the internal memory data is cleared.

While the telephone is OFF-HOOK and the supply voltage is more than the reset voltage, the oscillator starts up with a key input and this key input is implemented with the key debounce circuit. In this case, if the first key after the reset (note 1) is other than # and * (note 2), the internal memory data is cleared, and then this input key is encoded and stored into the memory. Then the following keys are stored ordinal into the memory, and also at the same time these keys are converted into the output pulse.

The key input speed is same as that of DTMF telephone because the input data is stored in the memory. The internal memory capacity is 23 digits. When key input are more than 23 digits, the completed key code are cleared (FIFO type memory) and then the new keys are stored into the memory. However, considering the capacity, in the moment while the stored data reach 23 digits, the key input is temporarily neglected.

After dialing, once the HD61825 is reset (note 1) and then is redial mode with the first # key. However, if the 24 or more keys has been dialled previously or the memory has already cleared, it cannot be redial mode. During the redial, any key input is not accepted but after that it can be used as a usual dialer.

The pulse output (DP output) stops with the pause during the redial and the redial starts again with # key. # key is used to insert the pause data in the memory. In the normal dial mode, # key does not influence the output of pulse but is stored in the memory as one digit.

NOTES

1. In the HD61825, the reset means the clearing all logic (counter, etc.) except RAM. HD61825 is reset when the

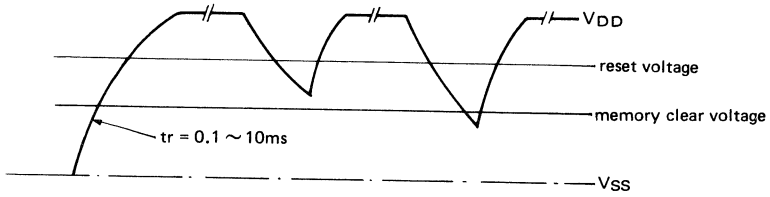
telephone is ON-HOOK or the supply voltage is less than the reset voltage.

2. *key is not used and always neglected in HD61825.

▪ PIN FUNCTIONS

• VDD (Pin 1)

This is a positive voltage supply pin which applies voltage on a basis of the VSS pin. HD61825 provides the internal sense circuit for the supply voltage. To make this circuit operate stable, the following rising time is necessary.

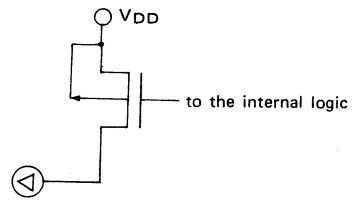


• DP (Pin 2) Dial Pulse

This is a pulse signal output pin for Loop Disconnect. Output circuit is P-Channel MOS open drain.

Break . . . . . High level
Make . . . . . Low level

While reset, the output voltage is held to the low level.



P-Channel MOS open drain output

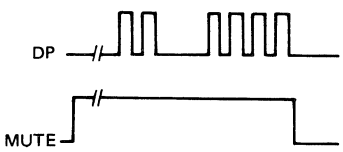
• MUTE (Pin 3)

This is a pin which mute the receiver. Output circuit is P-Channel MOS open drain.

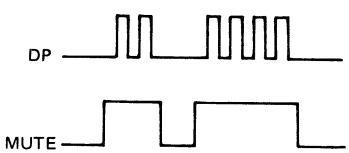
Mute . . . . . High level

While reset, the output voltage is held to the low level. In the HD61825, the following two kinds of MUTE – continuous MUTE and each digit MUTE are selectable. (IC's are different.)

• Continuous MUTE (HD61825A)



• Each digit MUTE (HD61825B)



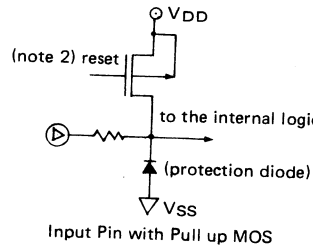
• MBR (Pin 4) Make/Break Ratio

This is a input pin with the pull up MOS to change the Make/Break ratio of DP output. To realize the low power dissipation on reset, the pull up MOS is turned off at the reset. (note 1)

MBR terminal	DP output	
	Make	Break
High (to V_{DD}) or open	33%	67%
Low (to V_{SS})	40%	60%

NOTES:

1. The input pins with the pull up MOS which is turned OFF at the reset, can be applied to MBR, DPRS, S0, S9 and HS.
2. The logic is positive. P MOS is ON with the low voltage and OFF with the high voltage.



Input Pin with Pull up MOS

- **DPRS (Pin 5) Dial Pulse Rate Selection**

This is a input pin to decide the pulse output speed (dial rate). It has a pull up MOS which is turned OFF at the reset.

DPRS terminal	Dial rate
High (to V_{DD}) or open	10 pps
Low (to V_{SS})	20 pps

- **S0, S9 (Pin 6, 7) Selection**

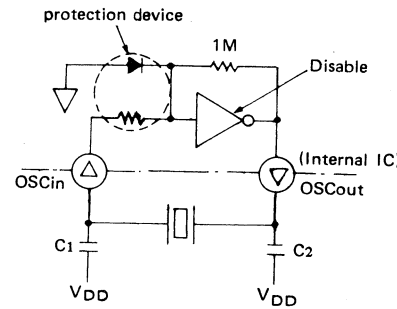
These are input pins to select functions and has pull up MOS which is turned OFF at the reset. The function of this terminal is to prevent the 0 dialing in and the 9 dialing in. When 0 or 9 is pushed after the reset, all the key inputs including the 0 or 9 key become invalid after then. In other words, the signals are not output to DP and MUTE. The telephone is initialized by the reset.

S0 terminal	S9 terminal	Function
High (to V_{DD}) or open	High (to V_{DD}) or open	Normal dialing mode
High (to V_{DD}) or open	Low (to V_{SS})	9 dialing in prevention mode
Low (to V_{SS})	High (to V_{DD}) or open	0 dialing in prevention mode
Low (to V_{SS})	Low (to V_{SS})	Test mode (for testing IC, Do not use.)

- **OSCin, OSCout (Pin 8, 9) Oscillation Input, Output**

These are input pins for the oscillator and constructs the inverter (with disable function to stop the oscillation). Using the ceramic resonator, the frequency is stable in the circuit. Moreover, the oscillator section needs two output capacitors externally. The ceramic oscillator should be 400 kHz and High Q.

Recommended ceramic oscillator . . . . .
Kyoto Ceramic Co., Ltd.
KBR-400H
ex. ceramic oscillator KBR-400H
C_1 = 100 pF
C_2 = 470 pF



Oscillation Circuit

- **V_{SS} (Pin 10)**

Negative power supply pin

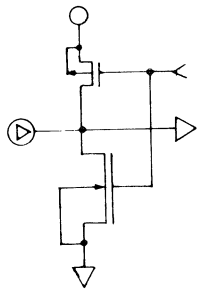
- **$\overline{COL1}$ to $\overline{COL3}$ (Pin 11 to 13) Column Input**
  $\overline{ROW1}$ to $\overline{ROW4}$ (Pin 14 to 17) Row Input

These are input/output pins for a key board which consists of PMOS pull up and NMOS driver. (As a matter of form, they are CMOS.)

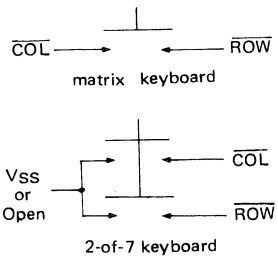
As the signals scan in Row side and Column side alternately, HD61825 can be connected both to the matrix-type keyboard and the 2-of-7 keyboard. While waiting the key input, Row is High level and Column is Low level. And in the reset condition, both Row and Column are Low level.

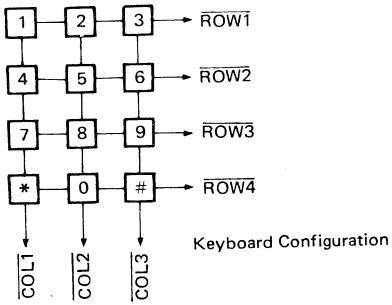
The hold time of the key should be more than 10 ms. (When the oscillation stops, the period for starting oscillation should be added.) (note 1)
The key debounce time is 20 ms.

NOTE:
1. The oscillation stops in HD61825;
   1. After the reset
   2. After the completion of DP output.
   3. On Pause



I/O Circuit for Keyboard Input/Output Pins





Keyboard Configuration

When two keys are pushed at the same time, the key of smaller number of ROW and COL is given priority and is input.

Ex. When typing 2 and 5 at the same time, 2 is input.

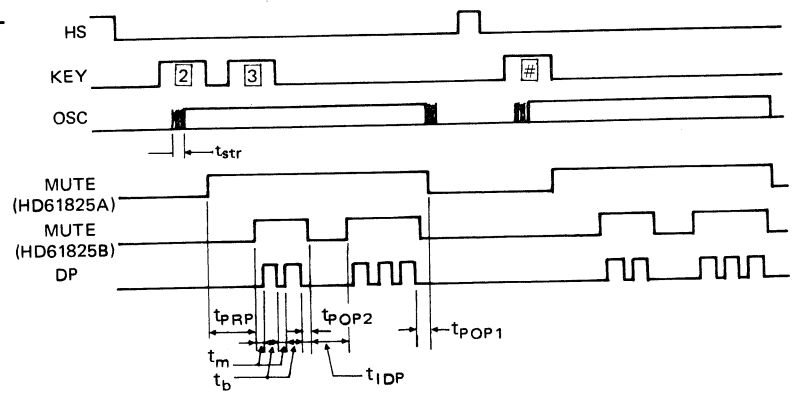
- **HS (PIN 18) HOOK SWITCH**

This is an input pin for detecting ON-HOOK/OFF-HOOK switch. It has a pull up MOS which is turned OFF at the reset.

ON HOOK . . . . . High (to V_{DD}) or open
OFF HOOK . . . . . Low (to Vss)

HD61825 is reset by making the HS terminal High level. If HS terminal is fixed to Low level, HD61825 is reset when the supply voltage falls less than the reset voltage. So, in this case, the HS pin is not used and the HD61825 controls the operation mode by the monitor of the supply voltage. However, as the pull up MOS is turned OFF with the reset signal, the current does not icnrease on reset.
An external capacitor must be provided between the HS pin and Vss to prevent the noise from the switch.

▪ TIMING CHART



Item	Symbol	MBR	DPRS	min	typ	max	Unit
Pre-Digital pause	t_{PRP}	–	–	–	800	–	ms
Make time	t_m	33%	10PPS	–	33.3	–	ms
		40%	10PPS	–	39.7	–	ms
		33%	20PPS	–	16.6	–	ms
		40%	20PPS	–	20.5	–	ms
Breka time	t_b	33%	10PPS	–	66.7	–	ms
		40%	10PPS	–	60.2	–	ms
		33%	20PPS	–	33.3	–	ms
		40%	20PPS	–	29.4	–	ms
Inter-Digit Pause	t_{IDP}	–	10PPS	–	767	–	ms
		–	20PPS	–	500	–	ms
Post-Digital Pause	t_{POP1}	–	–	–	36	–	ms
	t_{POP2}	–	–	–	33	–	ms

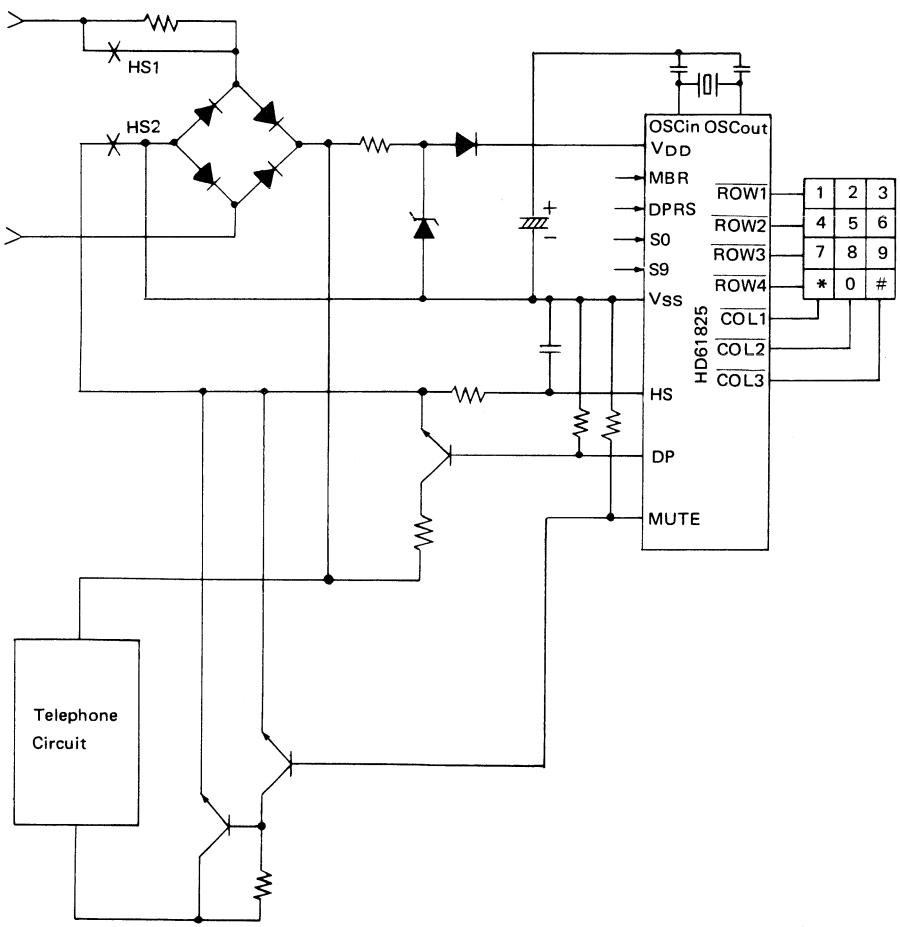
▪ AN EXAMPLE OF KEY OPERATION

	HOOK	KEY	DP
Normal Dial	ON OFF	[0] [1] [2] [3] [4]	0–1–2–3–4
Dial after Pause		[5] [6]	5–6
Redial	ON OFF	[#]	0–1–2–3–4–5–6
Dial after Redial		[7] [8]	7–8
Redial	ON OFF	[#]	0–1–2–3–4–5–6–7–8
Normal Dial	ON OFF	[9] [#] [1] [2]	9–1–2
(Pause Entry)	ON		
Redial	OFF	[#]	9
(Including Pause)		[#]	1–2
Dial of 24 digits or more	ON OFF	[1] [1] . . . . . [1] 24 times	1–1 . . . . . –1 24 times
Prevention of Over Flow	ON OFF	[#] [0] [1]	0–1

	HOOK	KEY	DP
(0 dialing in prevention mode with S0 = Low and S9 = High.)			
	ON OFF	[1] [2] [3] [0]	1–2–3–0
	ON OFF	[0] [4] [5] [6] [7]	
	ON OFF	[#]	1–2–3–0

NOTE:
After the output of pulse which corresponds to the each key operation are finished, Mute (also in HD61825A) is Low.

■ APPLICATION CIRCUIT

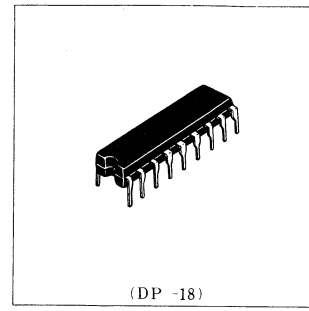


HD61826

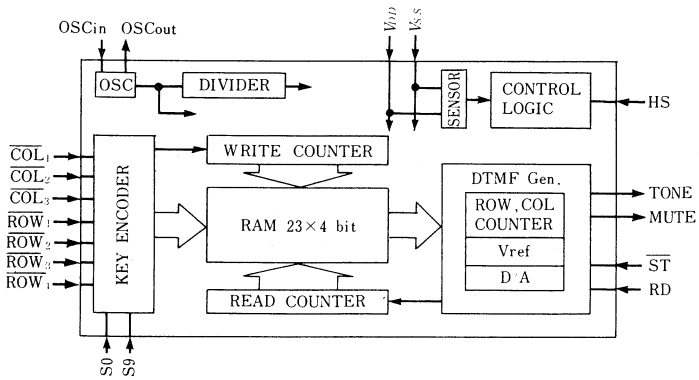
Tone Generator with Redial

■ FEATURES

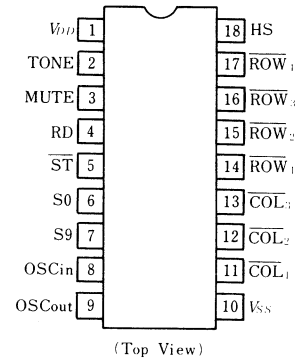
- Direct telephone-line operation
- CMOS process for low-power and low-voltage operation
- Uses either a standard 2-of-7 keyboard or the inexpensive matrix keyboard
- Stable operation by using ceramic resonator
- Redial function (# key)
- Pause input (# key)
- 0 or 9 dialing in inhibition pins for PABX system
- 23-digit redial memory
- Redial memory overflow protection (inhibit redial)
- On chip power supply voltage sense circuit
  - Memory clear voltage
  - Reset voltage
- Internal voltage reference circuit for stable Tone output
- Tone output with low distortion



■ BLOCK DIAGRAM



■ PIN ASSIGNMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

Item	Symbol	Value	Unit
Power supply voltage	V_{DD}	6.0	V
Terminal voltage	V_T	V_{SS} −0.3 to V_{DD} +0.3	V
Operating temperature	T_{opr}	−20 to +75	°C
Storage temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

● **DC Characteristics** (V_{SS} = 0V, V_{DD} = 2.0 to 5.5V, T_a = −20 to +75°C)

Item	Symbol	Test Condition	min.	typ. *1	max.	Unit
Operating voltage (1)	V_{DD}	Tone Out Mode	2.5	–	5.5	V
Operating voltage (2)	V_{DD}	Non Tone Out Mode	1.7	–	5.5	V
Reset voltage	V_{DR}		–	1.5	–	V
Memory clear voltage	V_{DC}		–	1.15	–	V
Operating current	I_{DD}	Tone Out Mode, no load	–	300	–	μA
Memory retention (reset) current	I_{DR}		–	0.5	–	μA
Input High voltage	V_{IH}	except HS pin	80% V_{DD}	–	–	V
		HS pin V_{DD} = 3.0 to 5.5V	90% V_{DD}	–	–	
		HS pin V_{DD} = 2.0 to 3.0V	V_{DD}-0.1	–	–	
Input Low voltage	V_{IL}		–	–	20% V_{DD}	V
Input leak current	$\|I_{LI}\|$	Pull-up MOS off, V_{IN} = 0 to V_{DD}	–	–	1	μA
Input Pull-up MOS current	$-I_P$	V_{IN} = 0 (RD, ST, S0, S9, ROW, COL, HS)	–	10	–	μA
Output High voltage	V_{OH}	$-I_{OH}$ = 0.1mA (MUTE)	V_{DD}-0.5	–	–	V
Output Low voltage	V_{OL}	I_{OL} = 0.1mA (ROW, COL)	–	–	0.3	V
Output leak current	$\|I_{LO}\|$	Output MOS off, V_{IN} = 0 to V_{DD} (TONE MUTE)	–	–	1	μA

● **AC Characteristics** (V_{SS} = 0V, V_{DD} = 2.0 to 5.5V, T_a = −20 to +75°C)

Item		Symbol	Test Condition	min.	typ.*1	max.	Unit
Oscillation frequency		f_{osc}		–	400	–	kHz
Oscillation start up time		t_{str}		–	5	–	ms
Tone Out	ROW TONE	V_{OR}	Single Tone Mode, 600Ω to V_{SS}	200	245	290	mVrms
	COLUM TONE	V_{OC}	V_{DD} = 2.5 to 5.5V, T_a = 25°C	270	310	360	mVrms
Tone Out	ROW TONE	V_{OR}	Single Tone Mode, 10kΩ to V_{SS}	245	270	300	mVrms
	COLUM TONE	V_{OC}	V_{DD} = 2.5 to 5.5V, T_a = 25°C	310	340	370	mVrms
ROW/COLUM Tone Out ratio		dB_{CR}	V_{DD} = 2.5 to 5.5V	–	2	–	dB
Output distortion		D_{IS}	10kΩ to V_{SS}, V_{DD} = 2.5 to 5.5V	–	5	7	%

*1 Typ. value is the design value (the standard value at V_{DD} = 2.5V and T_a = 25°C)

■ Description

The HD61826 is specifically designed IC to implement a DTMF (Dual-Tone Multi Frequency) telephone dialing system. With low voltage and low-power consumption CMOS process, it can be operated directly from the telephone line. This IC generates each DTMF signal by digitally synthesizing the sinusoidal waveform for the individual frequencies, using a 400 kHz ceramic oscillation as frequency reference. The last dial numbers can be redialed by the simple key operation using an internal redial memory. The HD61826 can also be used as a normal DTMF dialer without the redial memory by mode select input.

In the HD61826, ON HOOK/OFF HOOK is detected by the HS pin. When the supply voltage is lower than reset voltage, the HD61826 does not accept any key inputs independent of the HS pin. When the power supply voltage is lower than memory clear voltage, the internal memory data is cleared.

While the telephone is in the OFF HOOK and the supply voltage is higher than the reset voltage, the oscillator is enabled by a key input and then this key input is implemented with the key debounce circuit, In this case, if the first key after the reset (note 1) is other than # and *, the internal memory data is cleared, and then this input key is encoded and stored into the memory. The following keys are in turn stored into the memory and converted into DTMF signal outputs. (note 2)

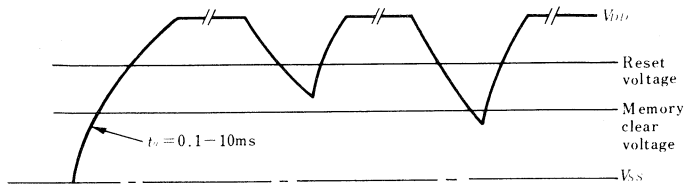
When the HD61826 is reset after dialing, it will be in the redial mode with the first # key. However, if the 24 or more keys have been dialed previously or the memory has already been cleared, it cannot be in the redial mode. During the redial mode, any key input is not accepted, but after the completion of redial, the HD61826 can be used as a usual dialer. The signal output will stop with the pause during the redial and the redial starts again with # key. # key is used to insert the pause data in the memory. In this case, # key does not influence the output of signal but is stored in the memory as one digit.

NOTES:
1. In the HD61826, the reset means the clearing of all logic (counter, etc.) except RAM. HD61826 is reset when the telephone is in the ON HOOK or the supply voltage is lower than the reset voltage.
2. While the key is pushed, the DTMF signal is kept generating.

■ PIN FUNCTION

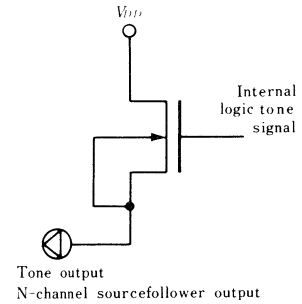
• V_{DD} (Pin 1)

This is a positive voltage supply pin which applies voltage to the basis of the V_{SS} pin. HD61826 provides the internal sense circuit for the supply voltage. To make this circuit operate stable, the following rising time is necessary.

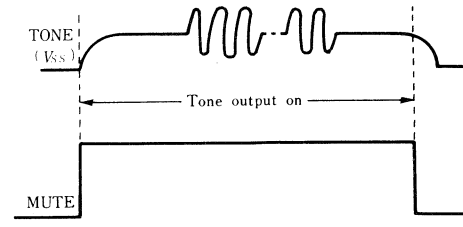


• TONE (Pin 2)

This is a Tone output (DTMF signal output) pin. Output circuit is N-Channel MOS source-follower and the resistor to Vss is necessary. Further, to realize low power consumption in the standby mode, TONE output MOS and internal V_{ref} circuit are turned off after tone output completed. And this is synchronous with MUTE signal. DTMF signal is digitally synthesized by using the 400 kHz oscillation as frequency reference. Tone output frequency of HD61826 and its deviation from standard DTMF are as follows:



		Standard DTMF (Hz)	Tone Output Frequency Using 400 kHz Oscillation	% Deviation from Standard
ROW	f_1	697	694,44	–0.37
	f_2	770	769,23	–0.10
	f_3	852	851,06	–0.11
	f_4	941	938,97	–0.22
COL	f_5	1209	1212,12	0.26
	f_6	1336	1333,33	–0.20
	f_7	1477	1481,48	0.30



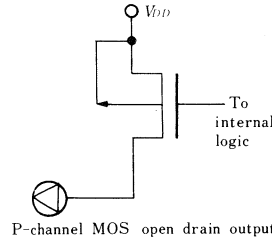
As the HD61826 contains an voltage reference (V_{ref}) circuit, it always generates stable Tone output amplitude even if supply voltage and temperature change.

• MUTE (Pin 3)

This is a pin which mutes the receiver and the transmitter. Output circuit is P-Channel MOS open drain.

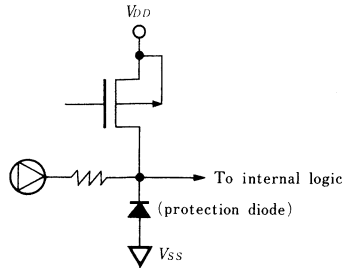
MUTE . . . High level

While reset, the output voltage is held to Low level.



- **RD (Pin 4) Redial Operation**

This is an input pin which selects HD61826 operations: a tone dialer with redial providing memory function, and a simple tone dialer in which only normal key input is converted into tone output. This pin is implemented with the pull-up MOS, and to realize the low power dissipation on reset, the pull-up MOS is turned off at the reset. (note 1)



RD pin	Operation Mode	Redial	Operation
High (to V_{DD}) or open	Tone Dialer with Redial	available	• no Tone out with * or # • Redial/Pause with #
Low (to V_{SS})	Simple Tone Dialer	not available	• Tone out with * or #

NOTES:
1. The input pins, with pull-up MOS which is turned off at the reset, can be applied to RD, $\overline{ST}$, S0, S9, HS.
2. The logic is positive. PMOS is ON with the low voltage and OFF with the high voltage.

- **$\overline{ST}$ (Pin 5) Single Tone Test**

This is an input pin to put HD61826 in the single tone mode for tone output test. This pin is implemented with the pull-up MOS which is turned off at the reset. Further, in the single tone mode, digital signal for test is output on MUTE. Usually $\overline{ST}$ pin should be fixed to High level or open.

$\overline{ST}$ pin	S0 pin	S9 pin	Operation Mode	Tone Output
High (to V_{DD}) or open	–	–	Dual Tone	DTMF Tone out
Low (to V_{SS})	Low	High	Single Tone	to ROW Single tone out
	High	Low		to COL Single tone out

NOTE: S0 and S9 pins should not be Low level at the same time.

- **S0, S9 (Pin 6, 7) Selection**

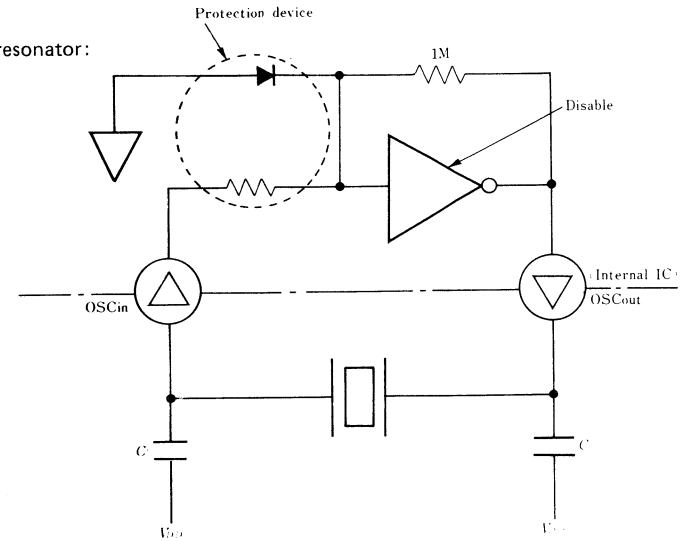
These are input pins to select functions and each of them has pull-up MOS which is turned OFF at the reset. The function of this terminal is to prevent the 0 dialing in and 9 dialing in, which is applied to the telephone subset under the PBX system. When the first key input after the reset is 0 or 9, all the key inputs including the 0 or 9 key become invalid after then. In other words, the signals are not output to TONE and MUTE. Then the telephone is initialized by the reset.

S0 Pin	S9 Pin	Function
High (to V_{DD}) or open	High (to V_{DD}) or open	Normal dialing mode
High (to V_{DD}) or open	Low (to V_{SS})	9 dialing in inhibition mode
Low (to V_{SS})	High (to V_{DD}) or open	0 dialing in inhibition mode
Low (to V_{SS})	Low (to V_{SS})	Test mode (for testing IC. Not use.)

- **OSCin, OSCout (Pin 8, 9) Oscillation Input, Output**

These are the input pins for the oscillator and construct the inverter (with disable function to stop the oscillation). The frequency is stable in the circuit by using the ceramic resonator. Then the oscillator section needs two external capacitors. The ceramic resonator should be 400 kHz and High Q.

Recommended ceramic resonator:
KYOCERA CO.
KBR-400H
ex. ceramic oscillation
C_1 = 100 pF
C_2 = 470 pF



Oscillation Circuit

When OSCout is open, a 400 kHz external pulse can be applied to OSCin.

- **V_{SS} (Pin 10)**

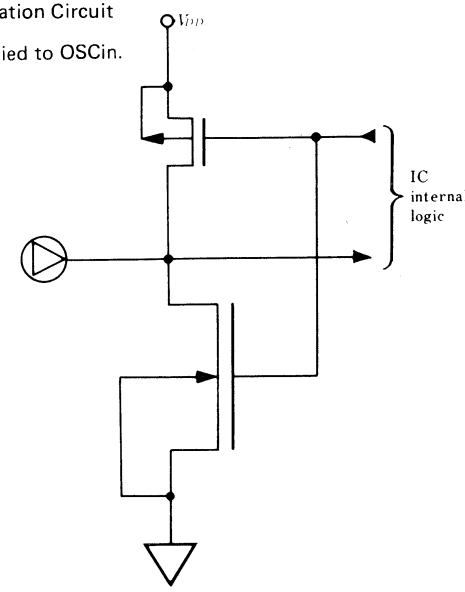
This is a negative power supply pin.

- **$\overline{COL_1}$ to $\overline{COL_3}$ (Pin 11 to 13) Colum Input**
  $\overline{ROW_1}$ to $\overline{ROW_4}$ (Pin 14 to 17) Row Input

These are input/output pins for a key board which consist of PMOS pull-up and NMOS driver. (As a matter of form, these are CMOS.)

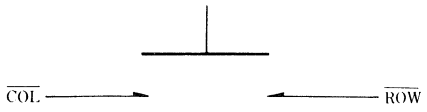
As the row and column are alternately scanned, the HD61826 can be connected both to the matrix-type keyboard and the 2-of-7 keyboard. While waiting for the key input, Rows are High level and Columns are Low level. And in the reset mode, both Row and Column are Low level.

The hold time of the key should be more than 10 ms. (While the oscillation stops, the period for starting oscillation should be added.) (note 1) The key debounce time is 20 ms. Tone is remaining while pushing the key (precisely speaking, after key operation, tone continues during the debounce time). But the key operation should meet the DTMF receiver specification.

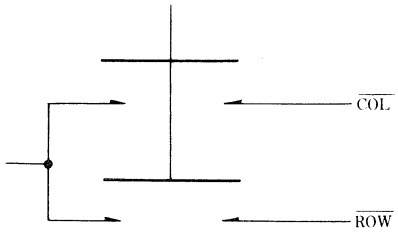


I/O Circuit for Keyboard

NOTES:
1. The oscillation stops in HD61826;
   1. After the reset
   2. After the completkon of Tone output
   3. On Pause



Matrix Keyboard



2–of–7 Keyboard

When two keys are pushed at the same time, the key of the smaller number of ROW and COL is given priority and is entered.

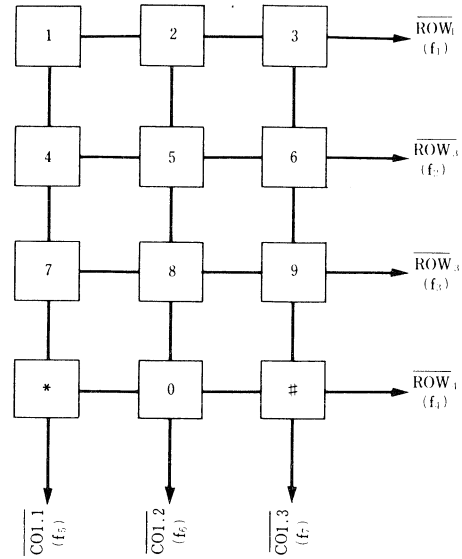
Ex. When 2 and 5 are pushed at the same time, 2 is accepted.

- **HS (Pin 18) Hook Switch**

This is an input pin for detecting ON-HOOK/OFF-HOOK switch. It has a pull-up MOS which is turned off at the reset.

ON HOOK . . . . High (to V_{DD}) or open

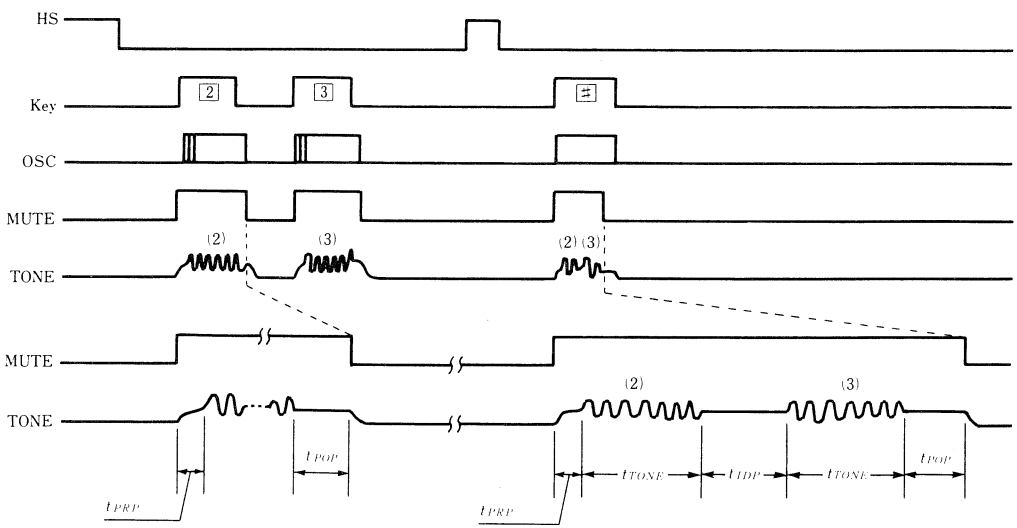
OFF HOOK . . . Low (to V_{SS})



Keyboard Configuration

HD61826 is reset by setting the HS terminal High level. Even if the HS terminal is fixed to Low level, the HD61826 is reset when supply voltage is lower than reset voltage. So without using the HS pin the HD61826 can control the operation mode by the monitor of supply voltage. Then, as the pull-up MOS is turned off with the reset signal, the current does not increase on reset. An external capacitor must be provided between the HS pin and V_{SS} to prevent the switch from chattering.

■ TIMING CHART



Mode	Item	Symbol	min.	typ.	max.	Unit
Normal Dial	Pre-Digital Pause	t_{PRP}	–	5	–	ms
	Post-Digital Pause	t_{POP}	–	44	–	ms
Redial	Pre-Digital Pause	t_{PRP}	–	5	–	ms
	Tone Output time	t_{TONE}	–	133	–	ms
	Inter-Digital Pause	t_{IDP}	–	87	–	ms
	Post-Digital Pause	t_{POP}	–	44	–	ms

■ AN EXAMPLE OF KEY OPERATION (RD = High)

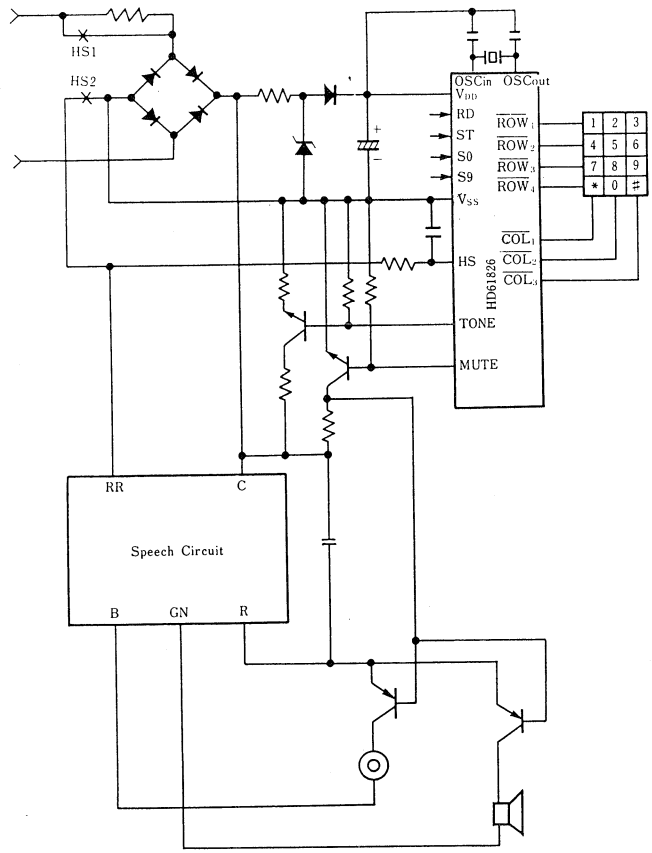
	HOOK	KEY	TONE
	ON		
Normal Dial	OFF	0 1 2 3 4 5 6	0, 1, 2, 3, 4, 5, 6, (note)
	ON		
Redial	OFF	=	0 1 2 3 4 5 6 (note)
Dial after Redial		7 8	7, 8,
	ON		
Redial	OFF	=	0 1 2 3 4 5 6 7 8
	ON		
Normal Dial	OFF	9 = 1 2	9, 1, 2,
(Pause Entry)	ON		
Redial	OFF	=	9,
(including Pause)		=	1 2,
	ON		
Dial of 24 digits or more	OFF	1 1 . . . . . 1 24 times	1, 1, ... 1, 24 times
	ON		
Prevention of Over Flow	OFF	= 0 1	0, 1

(0 dialing in inhibition mode with S0 = Low and S9 = High)

	ON	
	OFF	1 2 3 0
	ON	
	OFF	0 4 5 6 7 =
	ON	
	OFF	= 1 2 3 0,

NOTE: , shows that after tone output Mute is Low level and - shows that Mute is High level.

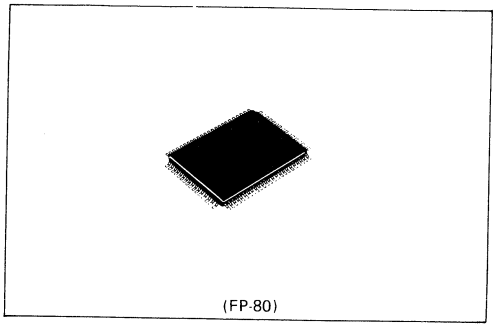
■ APPLICATION CIRCUIT



HD61827

Single-chip Microprocessor with Tone Generator

HD61827 is a microprocessor for telephone subset which has powerful and efficient architecture of HMCS400 family. This microprocessor includes a high-precision DTMF (Dual Tone Multi-Frequency) circuit, a 16-digit LCD driver and a 32 kHz oscillator for a watch. The CMOS process realizes low power dissipation, which allows the operation from telephone line.



(FP-80)

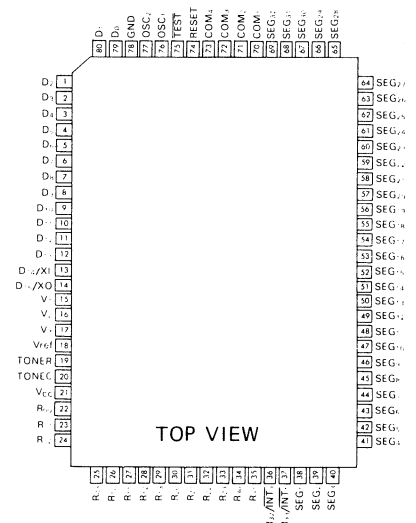
■ HARDWARE FEATURES

- 4-bit Architecture
- 2048-words x 10-bit ROM
- 256 Digits x 4-bit RAM
- 32 I/O Pins
- On-Chip DTMF Generator
- 16-Digit LCD Driver (1/3 Bias, 1/4 Duty)
- Two Timer/Counters, Watch Timer
  - 11-bit Prescaler
  - 8-bit Free Running Timer
  - 8-bit Auto-Reload Timer/Event Counter
  - Watch Timer (from 32 kHz Crystal Oscillator)
- Active LCD Display on Stand-by or Stop Mode Using 32 kHz Crystal
- Five Interrupt Sources
  - External 2
  - Timer/Counter 2
  - Watch Timer 1
- Subroutine Stack . . . Up to 16 Levels Including Interrupts
- Instruction Cycle Time 10 μs
- Two Low Power Dissipation Modes
  - Standby – Stop instruction execution while keeping clock oscillation and interrupt functions in operation
  - Stop – Stop instruction execution and system clock oscillation and active interrupt of watch timer
- On-Chip Oscillator
  - System Clock – Ceramic Resonator (Internal Rf Register)
  - Watch Timer – Crystal
- Automatic Display of the RAM Data in Special Address
- Package – FP-80

■ SOFTWARE FEATURES

- Same Instruction Set with HMCS400 Series; 99 Instructions
- High-Programming Efficiency with 10-Bit ROM/Word; 79 Instructions Are Single Word Instructions.
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area
- Subroutine Nesting Up to 16 Levels Including Interrupts
- Binary and BCD Arithmetic Operation
- Powerful Logical Arithmetic Operation
- Pattern Generation – Table Lock Up Capability –
- Bit Manipulation for Both RAM and I/O
- Blanking LCD Display by the Display Register

■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	1, 2
Terminal Voltage	V_T	−0.3 to V_{CC} + 0.3	V	1
Total Allowance of Input Current	ΣIo	45	mA	
Total Allowance of Output Currents	$-\Sigma Io$	45	mA	
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

(Note 1) All voltage are with respect to GND.

(Note 2) Keep $V_{CC} \geq V1 \geq V2 \geq V3 \geq GND$ and $V_{CC} \geq Vref \geq GND$.

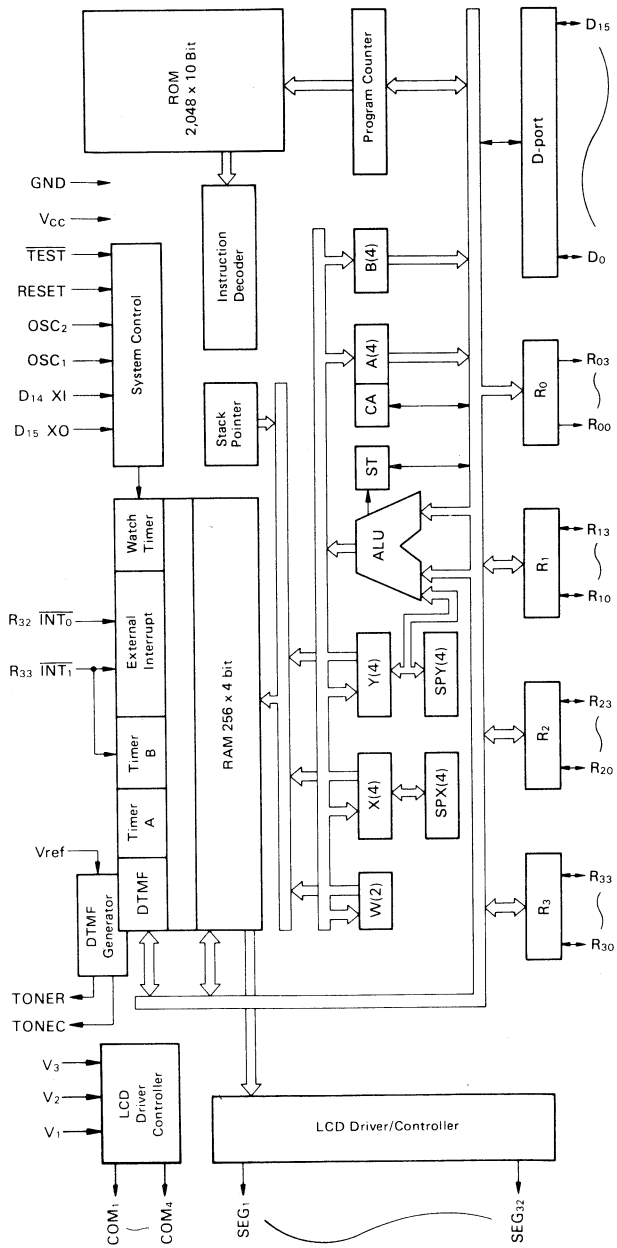


Fig. 1 BLOCK DIAGRAM

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 2.5 to 5.5V, Ta = −20 to +75°C, unless otherwise specified.)

Item	Symbol	Test Condition	Value			Unit	Pins	Note
			min	typ	max			
Input "High" Voltage	V_{IH}		0.8 V_{CC}	–	–	V	R10 to R33 D0 to D15	
		V_{CC} = 3.0 to 5.5V	0.8V_{CC}	–	–	V	Schmitt input pin, RESET, $\overline{INT0}$, $\overline{INT1}$	
		V_{CC} = 2.5 to 3.0V	V_{CC} −0.1	–	–	V		
Input "Low" Voltage	V_{IL}		–	–	0.2V_{CC}	V	R01 to R33 D0 to D15 RESET, $\overline{INT0}$, $\overline{INT1}$	
Output "High" Voltage	V_{OH}	$-I_{OH}$ = 0.1 mA	V_{CC} −0.4	–	–	V		2
Output "Low" Voltage	V_{OL}	I_{OL} = 0.4 mA	–	–	0.4	V	R00 to R33	
Input/Output Leakage Current	$\lvert I_{IL} \rvert$	V_{in} = 0V to V_{CC}	–	–	1	μA	D0 to D15	3
Pull-up MOS Current	$-I_P$	V_{CC} = 3V, V_{in} = 0V	–	50	–	μA		4
Segment Driver Voltage Drop	Vds	V_{CC} = 3V, Id = 0.01 mA	–	–	0.5	V	SEG1 to SEG32	5
Common Driver Voltage Drop	V_{dc}	V_{CC} = 3V, Id = 0.04 mA	–	–	0.5	V	COM1 to COM4	5
LCD power Supply Dividing Resistance	Rwell		30	100	300	kΩ		
LCD Frame Frequency	f_F	32 kHz oscillation: F = 32768 System clock : F = 25000	–	$\frac{F}{256}$	–	Hz		
Stop Mode Hold Voltage (1)	$V_{stop\ 1}$	RAM Data Retention	1.5	–	–	V	V_{CC}	
Stop Mode Hold Voltage (2)	$V_{stop\ 2}$	32 kHz Oscillation	2.5	–	–	V	V_{CC}	
Current Dissipation in Active Mode	I_{CC1}	V_{CC} = 3V DTMF : not active	–	210	500	μA	V_{CC}	6
	I_{CC2}	V_{CC} = 3V DTMF : active	–	500	1,100	μA	V_{CC}	6
Current Dissipation in Standby Mode	I_{stby}	V_{CC} = 3V DTMF : not active	–	160	350	μA	V_{CC}	6, 7
Current Dissipation in Stop Mode (1)	$I_{stop\ 1}$	V_{CC} = 3V LCD : ON	–	15	50	μA	V_{CC}	6, 8
Current Dissipation in Stop Mode (2)	$I_{stop\ 2}$	V_{CC} = 3V LCD : OFF	–	–	2	μA	V_{CC}	6, 9

(Note 1) The typ. is design value under Ta = 25°C, V_{CC} = 3.0V condition.

(Note 2) Applied to I/O pins with "CMOS" output selected by mask option.

(Note 3) Pull-up MOS current and output buffer current are excluded.

(Note 4) Applied to I/O pins "with Pull-up MOS" selected by mask option.

(Note 5) Voltage drop between power supply pins V_{CC}, V1, V2, V3 and each segment pin/common pin.

(Note 6) The current flowing through the input/output circuit is excluded.

(Note 7) The current dissipation in the Standby mode into which the system is put by the Standby instruction after reset.

(Note 8) Current dissipation in Stop mode (1): In the case when the crystal oscillation for timer is selected by the mask option. (Includes liquid crystal power supply current.)

(Note 9) Current dissipation in Stop Mode (2): In the case when the system clock is selected (Port is selected for D14 and D15) by the mask option.

- AC CHARACTERISTICS (V_{CC} = 2.5 to 5.5V, Ta = −20 to +75°C, unless otherwise specified.)

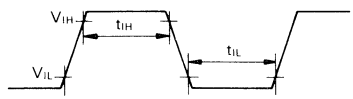
Item		Symbol	Test Condition	Value min	Value typ	Value max	Unit	Pins	Note
System Clock Oscillation Frequency		f_{cp1}		–	400	–	kHz		2
System Clock Oscillation Stabilization Time		t_{RC1}		–	2	–	ms		2
Instruction Cycle Time		t_{cyc}		–	10	–	μs		
Timer Clock Oscillation Frequency		f_{cp2}		–	32.768	–	kHz		3
Timer Clock Oscillation Stabilization Time		t_{RC2}		–	–	1	s		3
$\overline{INT0}$, $\overline{INT1}$ "High" Level Width		t_{IH}		2	–	–	t_{cyc}		4
$\overline{INT0}$, $\overline{INT1}$ "Low" Level Width		t_{IL}		2	–	–	t_{cyc}		4
RESET "High" Level Width		t_{RSTH}		2	–	–	t_{cyc}		5
Internal Vref	TONE Output Voltage (1)	V_{OR}	R_L = 100 kΩ	500	570	690	mVrms	TONER	6, 7
	TONE Output Voltage (2)	V_{OC}	R_L = 100 kΩ	520	600	720	mVrms	TONEC	6, 7
External Vref	TONE Output Voltage (1)	V_{OR}	V_{CC}−Vref = 2.0V R_L = 100 kΩ	–	670	–	mVrms	TONER	6, 7
	TONE Output Voltage (2)	V_{OC}	V_{CC}−Vref = 2.0V R_L = 100 kΩ	–	690	–	mVrms	TONEC	6, 7
TONE Output Distortion		%DIS	Short Circuit between TONER and TONEC R_L = 100 kΩ	–	3	7	%		8
TONE Output Ratio		dB_{CR}	Short circuit between TONER and TONEC R_L = 100 kΩ	–	2	–	dB		8
Column Compensation	Output Level Ratio C3/C4	C_{34}	R_L = 100 kΩ	–	−0.75	–	dB		6, 9
	Output Level Ratio C2/C4	C_{24}	R_L = 100 kΩ	–	−1.35	–	dB		6,9
	Output Level Ratio C1/C4	C_{14}	R_L = 100 kΩ	–	−2.1	–	dB		6,9

(Note 1) The typ. is design value under Ta = 25°C, V_{CC} = 3.0V condition.

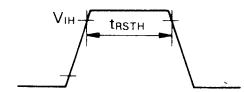
(Note 2) Applied when a ceramic resonator is used. System Clock Oscillation Stabilization Time t_{RC1} is the time until the oscillator stabilizes after V_{CC} reaches 2.5V at power-ON in the recommended oscillation circuit.

(Note 3) Applied when a crystal resonator is used. Timer Clock Oscillation Stabilization Time t_{RC2} is the time until the oscillator stabilizes after V_{CC} reaches 2.5V at power-ON in the recommended oscillation circuit.

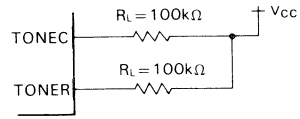
(Note 4) $\overline{INT0}$, $\overline{INT1}$



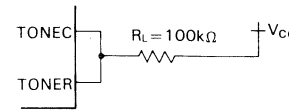
(Note 5) RESET



(Note 6) TONE Output Load Circuit



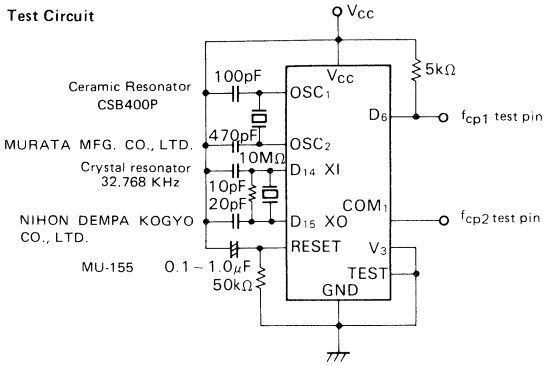
(Note 8) Distortion dB_{CR} Load Circuit

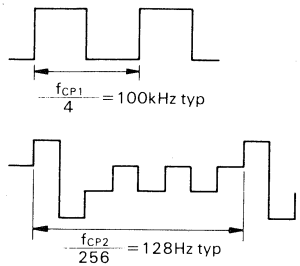


(Note 7) Use the standard value of internal/external Vref selected by the mask option.

(Note 9) The values of Column Compensation are applied when the compensation is specified in the mask option. They are represented with the ratio between the Column output levels (C_1, C_2, C_3) and the C_4 output level.

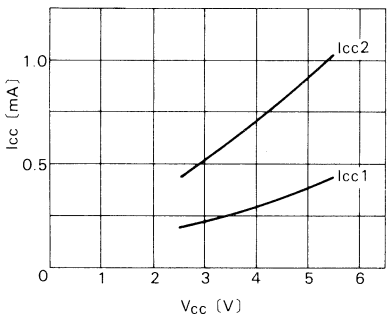
Test Circuit



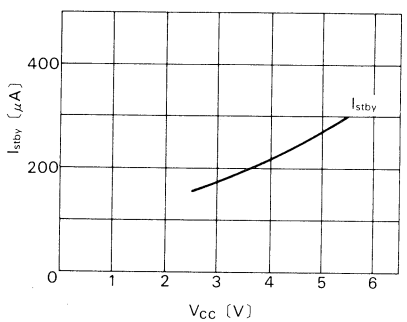


*When the 32 kHz timer oscillation is not selected by the mask option, the D14/XI and D15/XO are open and the output frequency through COM1 pin is $\frac{f_{cp1}}{4096}$ = 97.6 Hz typ.

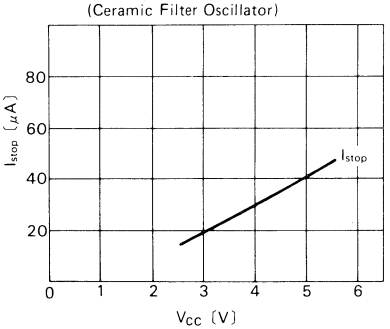
■ CHARACTERISTICS CURVE (REFERENCE DATA)



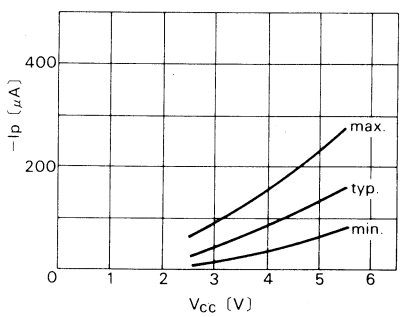
I_{CC1}, I_{CC2} vs. V_{CC} Characteristics (Ceramic Filter Oscillator)



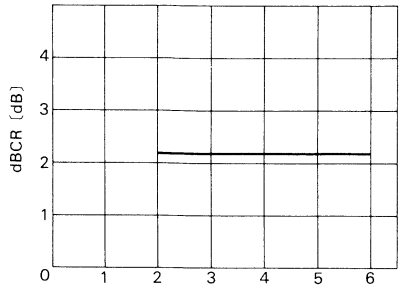
I_{stby} vs. V_{CC} Characteristics (Ceramic Filter Oscillator)



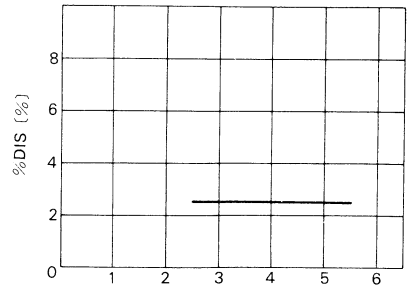
I_{stop} vs. V_{CC} Characteristics (32 kHz Crystal Oscillation)



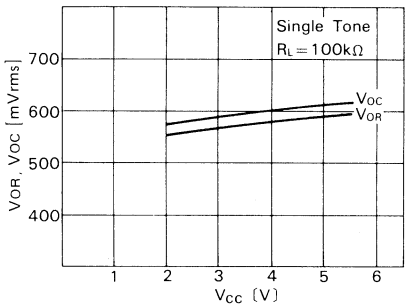
−Ip vs. V_{CC} Characteristics



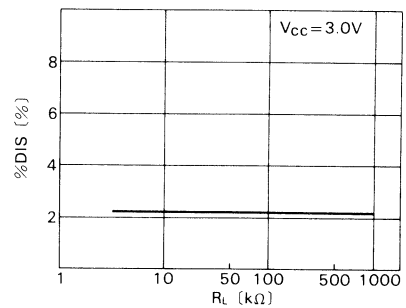
dBCR vs. V_{CC} Characteristics



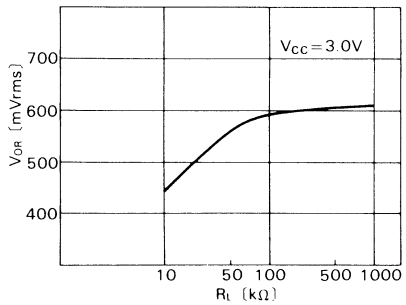
%DIS vs. V_{CC} Characteristics



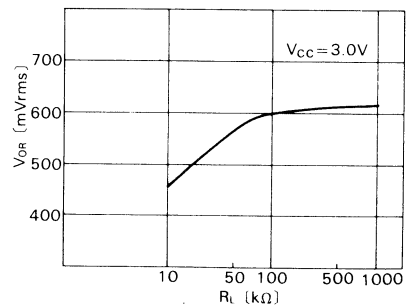
V_{OR}, V_{OC} vs. V_{CC} Characteristics (Internal Vref)



%DIS vs. R_L Characteristics (Internal Vref)



V_{OR} vs. R_L Characteristics (Internal Vref)



V_{OC} vs. R_L Characteristics (Internal Vref)

1. DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

- **GND, V_{CC}**

  There are power supply pins. Connect GND pin to earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin.

- **$\overline{\text{TEST}}$**

  $\overline{\text{TEST}}$ pin is not for user's application. $\overline{\text{TEST}}$ must be connected to V_{CC}.

- **RESET**

  RESET pin is used to reset MCU. For details, see "RESET".

- **OSC1, OSC2**

  These are input pins to the internal oscillator circuit. They can be connected to 400 kHz ceramic filter resonator. For details, see "INTERNAL OSCILLATION CIRCUIT."

- **D-Port (D0 to D13, D14/XI, D15/XO)**

  D-Port is a 1-bit Input Output common port. Each pin has the mask option to select the circuit type. For details, see "INPUT/OUTPUT."

- **D14/XI, D15/XO**

These are input pins to the internal timer clock oscillator. They can be connected to 32 kHz crystal filter resonator. When selecting D-port with mask option, D14 and D15 ports are used as XI and XO. For details, see "INTERNAL OSCILLATOR CIRCUIT."

- **R-Port (R0 to R3)**

R-port are 4-bit Input Output ports. R0 is output port and R1 to R3 are Input Output common ports. Each pins has the mask option to select its circuit type. R32 and R33 are also available as $\overline{INT0}$ and $\overline{INT1}$ respectively. For details, see "INPUT OUTPUT."

- **$\overline{INT0}$, $\overline{INT1}$**

These are the input pins to interrupt MCU operation externally. $\overline{INT1}$ can be used as an external event input pin for TIMER-B. $\overline{INT0}$ and $\overline{INT1}$ are also available as R32 and R33 respectively. For details, see "INTERRUPT."

- **V1, V2, V3**

These are power supply pins for LCD driver. As the dividing register for LCD are provided internally, any line should not be connected to these pins. The voltage on each pin are $V_{CC} \geq V1 \geq V2 \geq V3 \geq GND$. For details, see "LIQUID CRYSTAL DISPLAY."

- **COM1 to COM4**

These are common signal output pins for LCD display. For details, see "LIQUID CRYSTAL DISPLAY."

- **SEG1 to SEG32**

These are segment signal output pins for LCD display. For details, see "LIQUID CRYSTAL DISPLAY."

- **TONER, TONEC, V_{REF}**

These are DTMF signal output pins. Signals for each ROW and COLUMN are output through TONER and TONEC respectively. V_{REF} is a reference voltage of DTMF signals and the external E_{REF} can be applied with the mask option. ($V_{CC} \geq V_{REF} \geq GND$). For details, see "DTMF OUTPUT."

2. INTERNAL RESOURCES AND THEIR FUNCTIONS

■ ROM MEMORY MAP

MCU includes 2048 words x 10-bit ROM. ROM memory map is illustrated in Fig. 2-1 and described in the following paragraph.

- **Vector Address Area** . . . . . **$0000 to $000F**

When MCU is reset or an interrupt is serviced, the program is executed from the vector address. Program the JMPL instructions branching to the starting addresses of reset routine or of interrupt routines.

- **Zero-Page Subroutine Area** . . . . . **$0000 to $003F**

CAL instruction allows to branch to the subroutine in $0000 to $003F.

- **Pattern Area** . . . . . **$0000 to $07FF**

P instruction allows referring to the ROM data in $0000 to $07FF as a pattern.

- **Program Area** . . . . . **$0000 to $07FF**

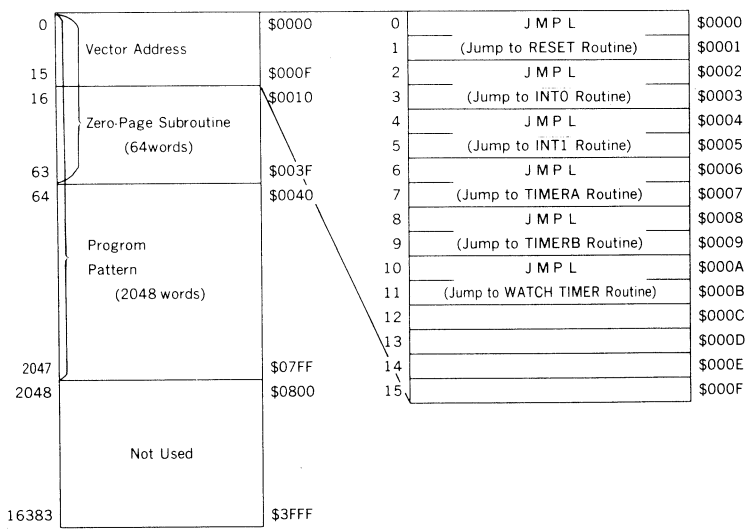


Fig. 2-1 ROM MEMORY MAP

■ RAM MEMORY MAP

MCU includes 256 digits x 4 bits RAM as the data area and stack area. In addition to these area, interrupt control bits and special registers are also mapped on the RAM memory space. RAM memory map is illustrated in Fig. 2-2 and described in the following paragraph.

- **Interrupt Control Bit Area . . . . . $000 to $003**
  This area is used for interrupt controls, and is illustrated in Fig. 2-3. It is accessible only by RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. RSP bit is used only for reset of the stack pointers.

- **Special Register Area . . . . . $004 to $00E**
  Special register is a mode or a data register for the external interrupt, DTMF, LCD and the timer/counter. These registers are classified into 3 types; Write-only, Read-only and Read/Write as shown in Fig. 2-2. These registers cannot be accessed by RAM bit manipulation instruction.

- **Data Area . . . . . $020 to $0DF**
  16 digits of $020 to $02F are called memory register(MR) and accessible by LAMR and XMRA instructions.

- **LCD Data Area . . . . . $030 to $04F**
  When LCD data is stored into this area, the data is automatically output to the segments and displayed on the LCD panel. LCD is illuminated with '1', and faden with '0'. Fig. 2-5 shows the configuration of LCD data area.

- **Stack Area . . . . . $3C0 to $3FF**
  Stack area is used for LIFO stacks with the contents of the program counter(PC), status(ST) and carry(CA) when processing subroutine call (CAL and CALL instructions) and interrupt.
  As 1 level requires 4 digits, this stack is nested to 16 level-stack max. The data pushed in the stack and LIFO stack state are shown in Fig. 2-4. The program counter is restored by RTN and RTNI instructions. Status and Carry are restored only by RTNI instruction. The area, not used for stacking, is available as a data area.

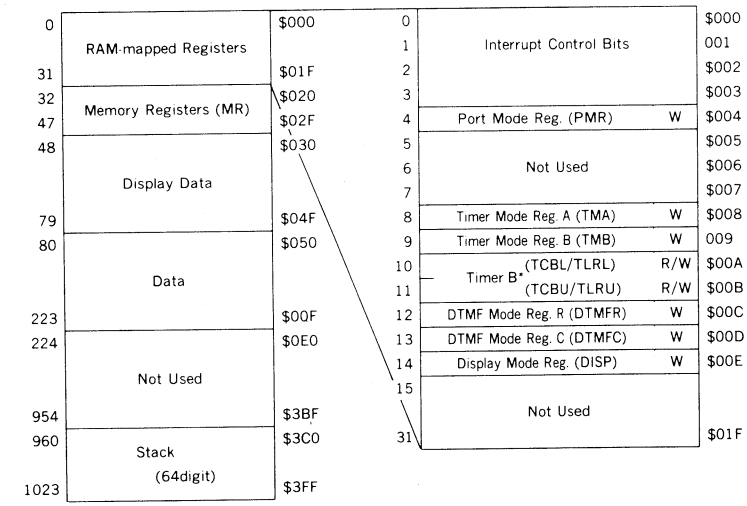


Fig. 2-2 RAM MEMORY MAP

	bit 3	bit 2	bit 1	bit 0	
0	IM0 (IM of $\overline{INT0}$)	IF0 (IF of $\overline{INT0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag	$000
1	IMTA (IM of TIMER-A)	IFTA (F of TIMER-A)	IM1 (Im of $\overline{INT1}$)	IF1 (IF of $\overline{INT1}$)	$001
2	IMWT (IM of WATCH TIMER)	IFWT (IF of WATCH TIMER)	IMTB (IM of TIMER-B)	IFTB (IF of TIMER-B)	$002
3	Not Used	Not Used	Not Used	Not Used	$003

Fig. 2-3 Configuration of Interrupt Control Bit Area

IF : Interrupt Request Flag
IM : Interrupt Mask
I/E : Interrupt Enable Flag
SP : Stack Pointer

(Note) Each bit in Interrupt Control Bits Area is set by SEM/SEMD instruction, is reset by REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, Interrupt Request Flag is not affected by SEM/SEMD instruction. The contents of Status becomes invalid when "Not Used" bit is tested.

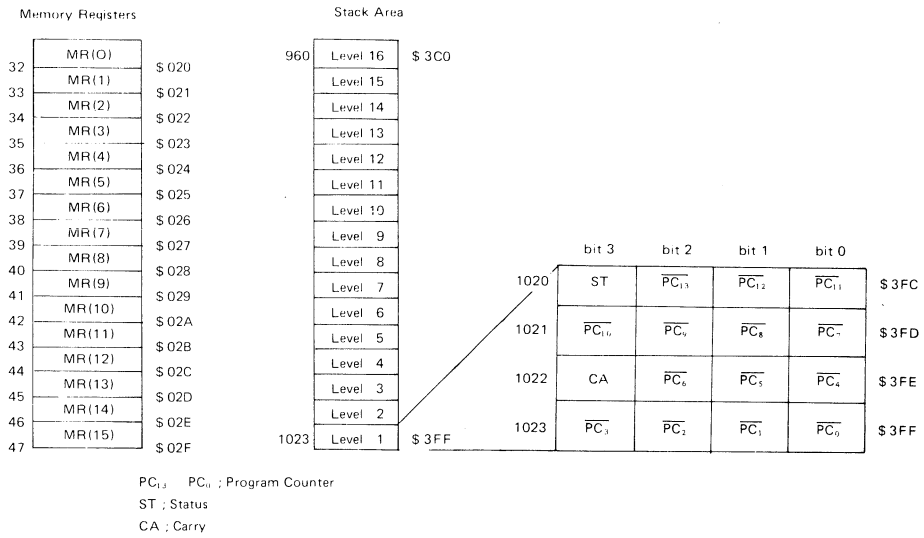


Fig. 2-4 Configuration of Memory Register, Stack Area and Stack Position

	BIT 3	BIT 2	BIT 1	BIT 0	
48	SEG 1	SEG 1	SEG 1	SEG 1	$030
49	SEG 2	SEG 2	SEG 2	SEG 2	$031
50	SEG 3	SEG 3	SEG 3	SEG 3	$032
51	SEG 4	SEG 4	SEG 4	SEG 4	$033
52	SEG 5	SEG 5	SEG 5	SEG 5	$034
53	SEG 6	SEG 6	SEG 6	SEG 6	$035
54	SEG 7	SEG 7	SEG 7	SEG 7	$036
55	SEG 8	SEG 8	SEG 8	SEG 8	$037
56	SEG 9	SEG 9	SEG 9	SEG 9	$038
57	SEG10	SEG10	SEG10	SEG10	$039
58	SEG11	SEG11	SEG11	SEG11	$03A
59	SEG12	SEG12	SEG12	SEG12	$03B
60	SEG13	SEG13	SEG13	SEG13	$03C
61	SEG14	SEG14	SEG14	SEG14	$03D
62	SEG15	SEG15	SEG15	SEG15	$03E
63	SEG16	SEG16	SEG16	SEG16	$03F
	COM 4	COM 3	COM 2	COM 1	

	BIT 3	BIT 2	BIT 1	BIT 0	
64	SEG17	SEG17	SEG17	SEG17	$040
65	SEG18	SEG18	SEG18	SEG18	$041
66	SEG19	SEG19	SEG19	SEG19	$042
67	SEG20	SEG20	SEG20	SEG20	$043
68	SEG21	SEG21	SEG21	SEG21	$044
69	SEG22	SEG22	SEG22	SEG22	$045
70	SEG23	SEG23	SEG23	SEG23	$046
71	SEG24	SEG24	SEG24	SEG24	$047
72	SEG25	SEG25	SEG25	SEG25	$048
73	SEG26	SEG26	SEG26	SEG26	$049
74	SEG27	SEG27	SEG27	SEG27	$04A
75	SEG28	SEG28	SEG28	SEG28	$04B
76	SEG29	SEG29	SEG29	SEG29	$04C
77	SEG30	SEG30	SEG30	SEG30	$04D
78	SEG31	SEG31	SEG31	SEG31	$04E
79	SEG32	SEG32	SEG32	SEG32	$04F
	COM 4	COM 3	COM 2	COM 1	

Fig 2-5 Configuration of Display Data Area for LCD

■ REGISTER AND FLAG

The MCU has nine registers and two flags for the CPU operation. They are illustrated in the following paragraphs.

• Accumulator(A), B Register(B)

Accumulator and B Register are 4-bit registers used to hold the results of Arithmetic Logic Unit (ALU), and to transfer data to/from memories, I/O and other registers.

• W Register(W), X Register(X), Y Register(Y)

W register is 2-bit, and X and Y registers are 4-bit registers used for indirect addressing of RAM. Y register is also used for D-port addressing. W register is write-only and cannot be read.

• SPX Register(SPX), SPY Register(SPY)

SPX and SPY registers are 4-bit registers used to assist X and Y registers respectively.

• Carry(CA)

Carry(CA) stores the overflow of ALU generated by the arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, Carry is pushed onto or recovered from the stack by RTNI instruction. (It's not affected by RTN instruction.)

• Status(ST)

Status(ST) holds the ALU overflow, ALU non-zero and the results of bit test instruction for the arithmetic or compare instruction. It is used for a branch condition of BR, BRL, CAL or CALL instructions. The value of the Status remains unchanged until the next arithmetic, compare or bit test instruction is executed. Status goes to "1" after the BR, BRL, CAL or CALL instruction has been executed (irrespective of its execution/skip). During the interrupt servicing, Status is pushed onto or recovered from the stack by RTNI instruction. (It's not affected by RTN instruction.)

• Program Counter(PC)

Program Counter is a 14-bit binary counter for ROM addressing.

• Stack Pointer(SP)

Stack pointer is used to point the address of the next stacking area up to 16 levels. The stack pointer is initialized to locate S3FF on the RAM address, and is decremented by 4 as data is pushed into the stack, and incremented by 4 as data is recovered from the stack. The upper 4 bits of the stack pointer is fixed to "1111", so 16 nesting levels max. are allowed.

There are two methods to initialize the stack pointer to S3FF: MCU reset as described above, and the reset of RSP bit by REM and REMD.

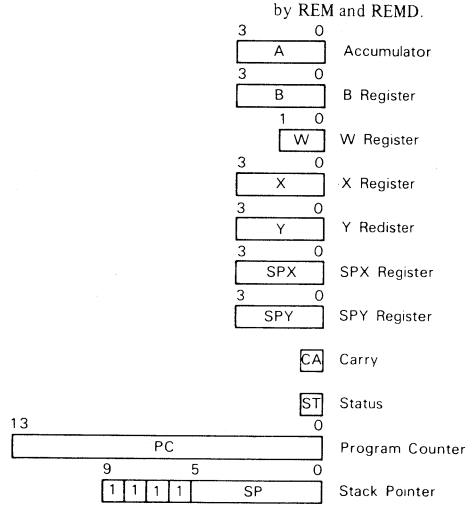


Fig. 2-6 Register and Flags

■ INTERRUPT

The MCU can be interrupted by five different factors; the external signals ($\overline{INT0}$, $\overline{INT1}$), timer/counter (TIMER-A, TIMER-B), and watch timer (WATCH-T). In each factor, the Interrupt Request Flag, Interrupt Mask and interrupt vector address will be used to control and maintain the interrupt request. The Interrupt Enable Flag is also used to control the total interrupt operations.

• Interrupt Control Bit and Interrupt Service

The interrupt control bit is mapped on S000 to S003 of the RAM address and can be accessed by RAM bit manipulation instruction. (The Interrupt Request Flag (IF) cannot be set by software.) The Interrupt Enable Flag (I/E) and Interrupt Request Flag (IF) are set to "0" and the Interrupt Mask (IM) is set to "1" at the initialization by MCU reset.

Fig. 2-7 shows the interrupt block diagram. Table 2-1 shows the interrupt priority and vector addresses, and Table 2-2 shows the conditions that the interrupt service is executed by one of the five interrupt factors.

The interrupt request is generated when the Interrupt Request Flag is set to "1" and the Interrupt Mask is "0". If the Interrupt Enable Flag is "1", then the interrupt will be activated and vector addresses will be generated from the priority PLA correspoinding to the five interrupt factors.

Fig. 2-8 shows the interrupt service sequence, and Fig. 2-9 shows the interrupt flowchart. If the interrupt is requested, the instruction finishes its execution in the first cycle. The Interrupt Enable Flag is reset in the second cycle. In the second and third cycles, the Carry, Status and Program Counter are pushed onto the stack. In the third cycle, the instruction is executed again after jumping to the vector address.

In each vector address, program JMPL instruction to branch to a starting address of the interrupt routine. The Interrupt Request Flag which caused the interrupt service must be reset by software in the interrupt routine.

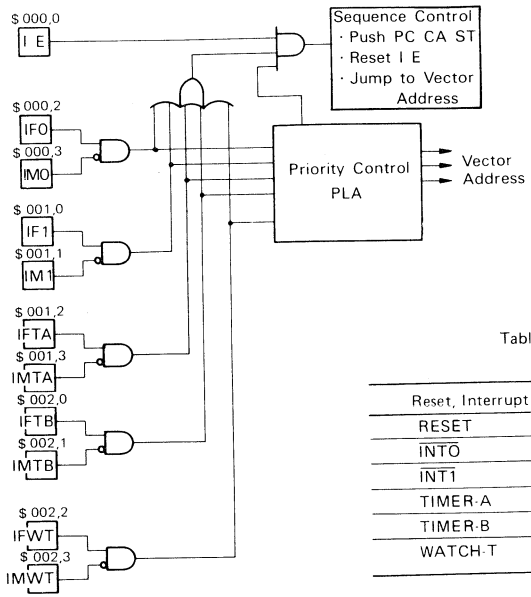


Fig. 2-7 Interrupt Circuit Block Diagram

Table 2-1 Vector Address and Interrupt Priority

Reset, Interrupt	Priority	Vector Addresses
RESET	–	$0000
$\overline{\text{INT0}}$	1	$0002
$\overline{\text{INT1}}$	2	$0004
TIMER-A	3	$0006
TIMER-B	4	$0008
WATCH-T	5	$000A

Table 2-2 Conditions of Interrupt Service

Interrupt condition bits \ Interrupt factor	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	TIMER-A	TIMER-B	WATCH-T
I/E	1	1	1	1	1
IF0·$\overline{\text{IM0}}$	1	0	0	0	0
IF1·$\overline{\text{IM1}}$	*	1	0	0	0
IFTA·$\overline{\text{IMTA}}$	*	*	1	0	0
IFTB·$\overline{\text{IMTB}}$	*	*	*	1	0
IFWT·$\overline{\text{IMWT}}$	*	*	*	*	1

*Don't care.

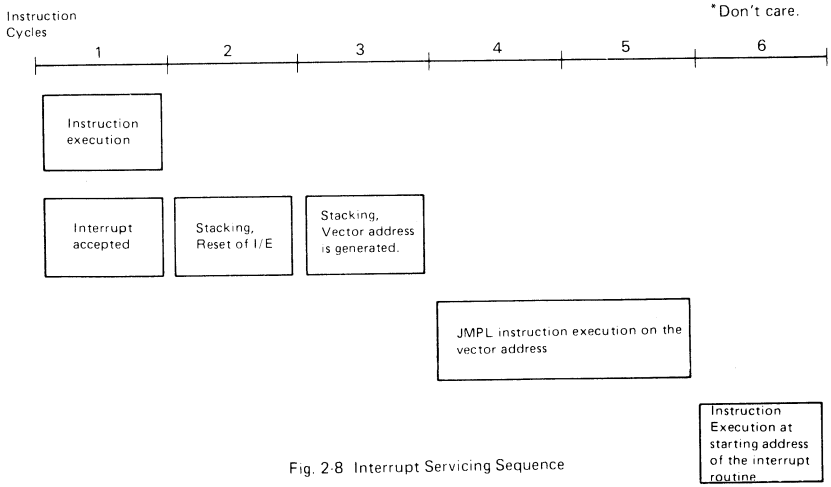


Fig. 2-8 Interrupt Servicing Sequence

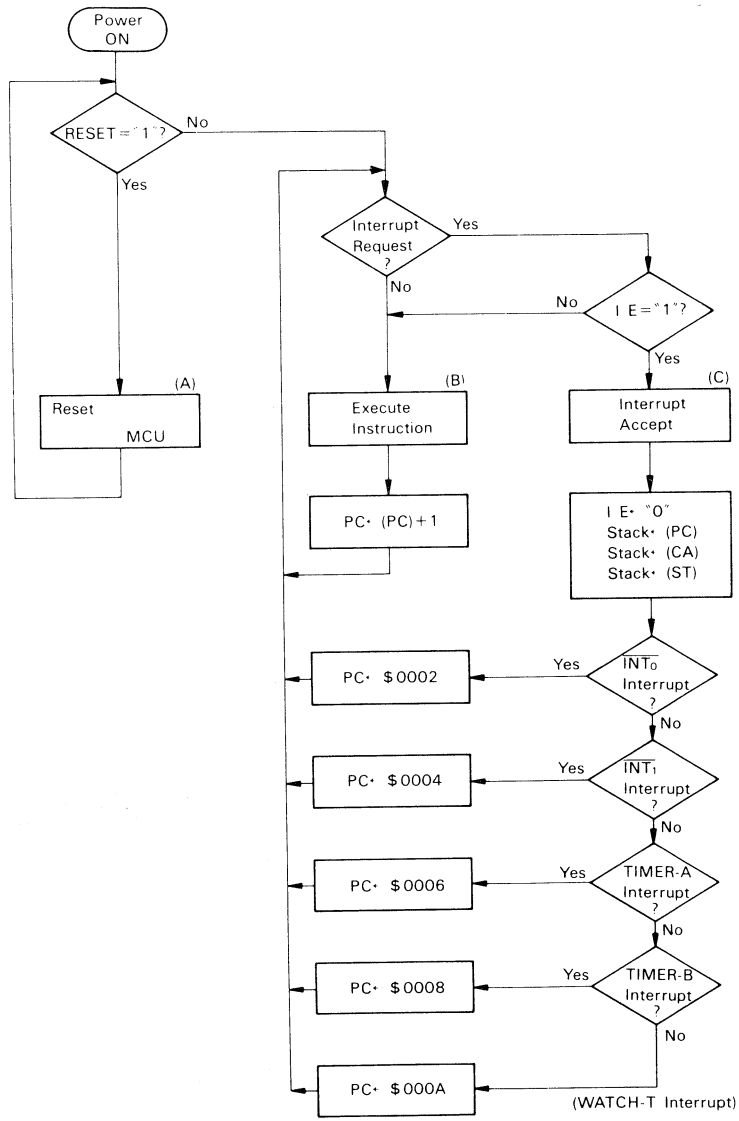


Fig. 2-9 Interrupt Servicing Flowchart

- **Interrupt Enable Flag (I/E : $000,0)**

The Interrupt Enable Flag controls enable/disable of all interrupt requests as shown in Table 2-3. The Interrupt Enable Flag is reset by the interrupt servicing and set by RTNI instruction.

Table 2-3 Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

- **External Interrupt ($\overline{INT0}$, $\overline{INT1}$)**

To use external interrupt, select R32/$\overline{INT0}$, R33/$\overline{INT1}$ port for $\overline{INT0}$, $\overline{INT1}$ mode by setting the Port Mode Register (PMR: $004).

The External Interrupt Request Flag (IF0, IF1) are set at the falling edge of $\overline{INT0}$, $\overline{INT1}$ inputs.

$\overline{INT1}$ input can be used as a clock signal input of TIMER-B. Then, TIMER-B counts up at each falling edge of input. When using $\overline{INT1}$ as TIMER-B external event, an External Interrupt Mask (IM1) has to be set so that the interrupt request by $\overline{INT1}$ will not be accepted.

Table 2-4 External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 2-5 External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

- **External Interrupt Request Flag (IF0 : $000, 2, IF1 : $001,0)**

The External Interrupt Request Flags (IF0, IF1) are set at the falling edge of $\overline{INT0}$, $\overline{INT1}$ inputs respectively.

- **External Interrupt Mask (IM0 : $000, 3, IM1 : $001, 1)**

The External Interrupt Mask is used to mask the external interrupt requests.

- **Port Mode Register (PMR : $004)**

The Port Mode Register is a 4-bit write-only register which controls the R32/$\overline{INT0}$ pin and R33/$\overline{INT1}$ pin as shown in Table 2-6. The Port Mode Register will be initialized to S0 by MCU reset, so that all these pins are set to a port mode.

Table 2-6 Port Mode Register

PMR bit 3	R33/$\overline{INT1}$ pin
0	Used as R33 port input/output pin
1	Used as $\overline{INT1}$ input pin

PMR bit 2	R32/$\overline{INT0}$ pin
0	Used as R32 port input/output pin
1	Used as $\overline{INT0}$ input pin

■ TIMER

The MCU contains a prescaler and two timer/counters (TIMER-A, TIMER-B). Fig. 2-10 shows the block diagram. The prescaler is an 11-bit binary counter. TIMER-A is an 8-bit free-running timer. TIMER-B is an 8-bit auto-reload timer/event counter.

- **Prescaler**

The input to the prescaler is a system clock signal. The prescaler is initialized to S000 by MCU reset, and the prescaler starts to count up the system clock signal as soon as RESET input goes to logic "0". The prescaler stops counting only by MCU reset and stop mode. The prescaler provides clock signals to TIMER-A and TIMER-B. The prescaler divide ratio of the clock signals are selected according to the contents of the mode registers such as Timer Mode Register A (TMA) and Timer Mode Register B (TMB).

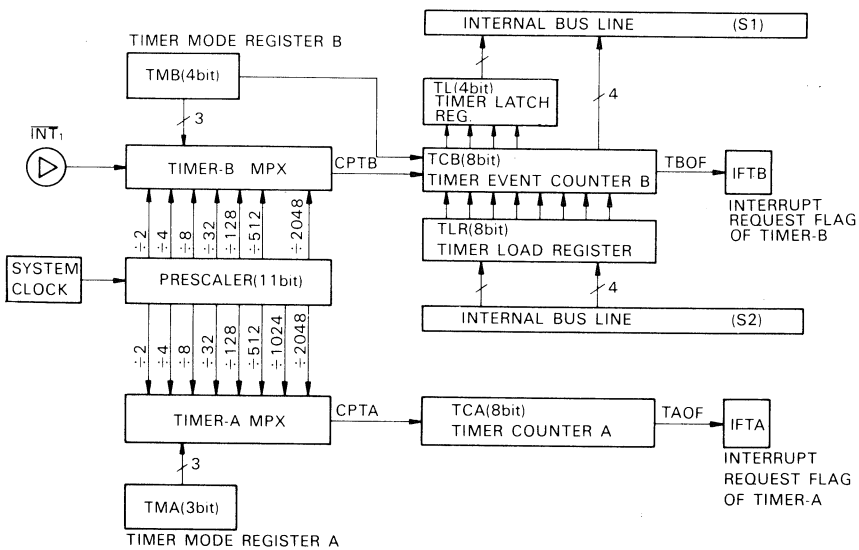


Fig. 2-10 Timer/Counter Block Diagram

- **TIMER-A Operation**

After TIMER-A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after TIMER-A is counted up to $FF, TIMER-A is set to $00 again, generating overflow output. This leads to setting TIMER-A interrupt Request Flag (IFTA ; $001, 2) to "1". Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to TIMER-A are selected by the Timer Mode Register A (TMA : $008).

- **TIMER-B Operation**

Timer Mode Register B (TMB : $009) is used to select the auto-reload function and the prescaler divide ratio of TIMER-B as the input clock source. When the external event input is used as an input clock signal to TIMER-B, select the R33/$\overline{INT1}$ as $\overline{INT1}$ and set the External Interrupt Mask (IM1) to "1" to prevent the external interrupt request from occurring.

TIMER-B is initialized according to the value written into the Timer Load Register by software. TIMER-B counts up at every clock input signal. When the next clock signal is applied to TIMER-B after TIMER-B is set to $FF, TIMER-B will be initialized again generating overflow output. In this case, if the auto-reload function is selected, TIMER-B is initialized according to the value of the Timer Load Register. If the auto-reload function is not selected, TIMER-B goes to $00. TIMER-B Interrupt Request Flag (IFTB : $002.0) will be set at this overflow output.

- **Timer Mode Register A (TMA : $008)**

The Timer Mode Register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of TIMER-A clock input, as shown in Table 2-11.

The Timer Mode Register A is initialized to $0 by MCU reset.

Table 2-11 Timer Mode Register A

TMA			Prescaler Divide Ratio
Bit 2	Bit 1	Bit 0	
0	0	0	÷ 2,048
0	0	1	÷ 1,024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

- **Timer Mode Register B (TMB : $009)**

The Timer Mode Register B is a 4-bit write-only register. The Timer Mode Register B controls the selection of the auto-reload function of TIMER-B and the prescaler divide ratio, and the source of the clock input signal, as shown in Table 2-12.

The Timer Mode Register B is initialized to $0 by MCU reset.

The operation mode of TIMER-B is changed at the second instruction cycles after writing into the Timer Mode Register B.

Therefore, it is necessary to program the write instruction to TLRU after the changed contents of TMB is enabled.

Table 2-12 Timer Mode Register B

TMB	Auto-reload Function
Bit 3	
0	No
1	Yes

TMB			Prescaler Divide Ratio Clock Input Source
Bit 2	Bit 1	Bit 0	
0	0	0	÷2,048
0	0	1	÷ 512
0	0	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT1}$ (External Event Input)

Table 2-13 Timer-A Interrupt Request Flag

TIMER-A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 2-14 Timer-A Interrupt Mask

Timer-A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

- **TIMER-B TCBL : $00A, TCBU : $00B**
  TLRL : $00A, TLRU : $00B

TIMER-B consists of an 8-bit write-only Timer Load Register, and an 8-bit read-only Timer Event Counter. Each of them has a low-order digit (TCBL : $00A, TLRL : $00A) and a high order digit (TCBU : $00B, TLRU : $00B).

The Timer Event Counter can be initialized by writing data into the Timer Load Register. In this case, write the low-order digit first, and then the high-order digit. The Timer Event Counter is initialized at the time when the high-order digit is written. The Timer Load Register will be initialized to $00 by the MCU reset.

The counter value of TIMER-B can be obtained by reading the Timer Event Counter. In this case, read the high-order digit first, and then the low-order digit. The count value of low-order digit is latched at the time when the high-order digit is read.

- **TIMER-A Interrupt Request Flag (IFTA : $001, 2)**

The TIMER-R Interrupt Request Flag is set by the overflow output of TIMER-A.

- **TIMER-A Interrupt Mask (IMTA : $001, 3)**

TIMER-A Interrupt Mask prevents an interrupt request generated by TIMER-A Interrupt Request Flag.

- **TIMER-B Interrupt Request Flag (IFTB : $002, 0)**

The TIMER-B Interrupt Request Flag is set by the overflow output of TIMER-B.

- **TIMER-B Interrupt Mask (IMTB : $002, 1)**

TIMER-B Interrupt Mask prevents an interrupt request generated by TIMER-B Interrupt Request Flag.

Table 2-15 TIMER-B Interrupt Request Flag

TIMER-B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 2-16 TIMER B Interrupt Mask

TIMER B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

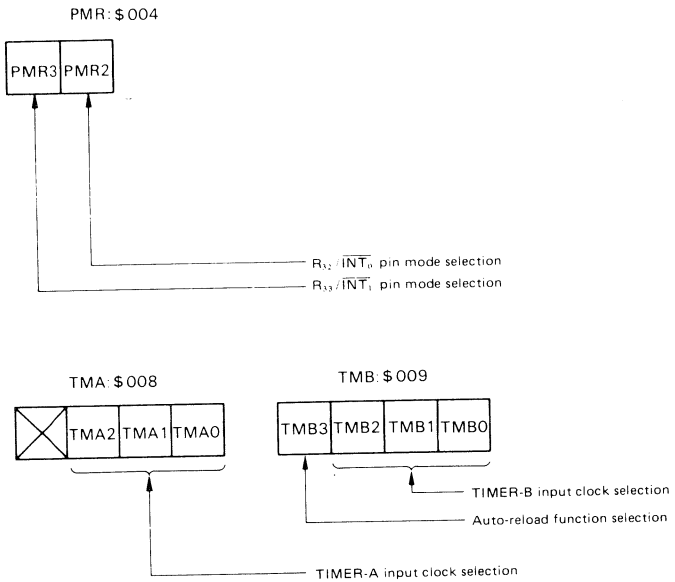


Fig. 2-11 Mode Register Configuration and Function

■ WATCH TIMER

The MCU has a watch timer as shown in Fig. 2-12 block diagram. It consists of a 6-bit divider and an 8-bit prescaler. The overflow occurred in the prescaler functions as the watch timer interrupt request flag (IFWT : S002, 2). The clock input to the divider is selectable with mask option as described below. Specify the clock input in "HD61827 MASK OPTION LIST" on the last page when ordering ROM.

The 32-kHz crystal oscillation for timer is useful to realize a function of watch easily because the correct time can be known by the timer.

(1) When Selecting System Clock (Instruction Frequency/4)

When selecting system clock as input to the divider, the watch timer interrupt request flag (IFWT : S002, 2) is set every cycle of the prescaler output (system clock cycle $\times 2^{16}$). Therefore, the watch timer is active in the active mode and the stand-by mode in which the system clock operates.

When not used, set the watch timer interrupt mask bit (IMWT : S002, 3). ($t_{cyc} \times 2^{16} = 10\ \mu s \times 2^{16} \doteqdot 655.4$ ms)

(2) When Selecting 32 kHz Crystal Oscillation (For Timer)

The HD61827 provides a 32 kHz crystal oscillator between D14 and D15 pins. The 32 kHz clocks are input to the 6-bit divider. The overflow is occurred in the prescaler every 500 ms (2Hz), which sets the watch timer interrupt request flag (IFWT : S002, 2). In this case, the hatched parts in the block diagram do not stop operation even in the stop mode. Therefore, the watch timer is active in the active mode, stand-by mode and stop mode.

The system clock oscillator is halted in the stop mode, and is activated by the prescaler overflow signals. However, as the oscillator takes some period to stabilize, the system is placed from the stop mode into the stand-by mode at the same time when the system clock oscillation circuit is started by the system start-up signal. The system clock oscillation circuit is started about 7.9 ms (fixed) before the output of the clock timer interrupt signal. Therefore, the stable timer clock interrupt routine is executed with starting the system clock oscillation previously, even if the interrupt occurs from the stop mode.

Using this function allows the intermittent timer operation; the necessary program is executed every 500 ms (2Hz) and the system is placed into the stop mode by an instruction after the completion of program execution.

As mentioned above, the timer operation time is reduced by using this functions, thereby the power consumption is lowered.

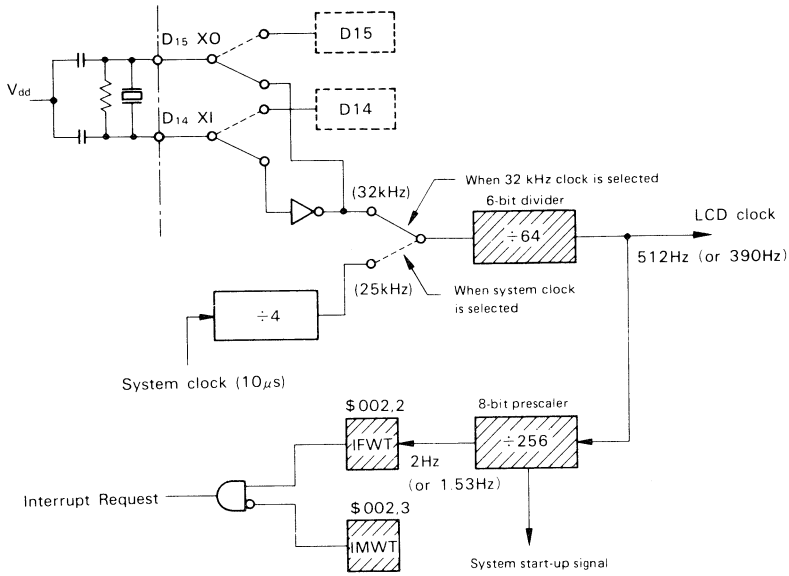


Fig. 2-12 Watch Timer Block Diagram

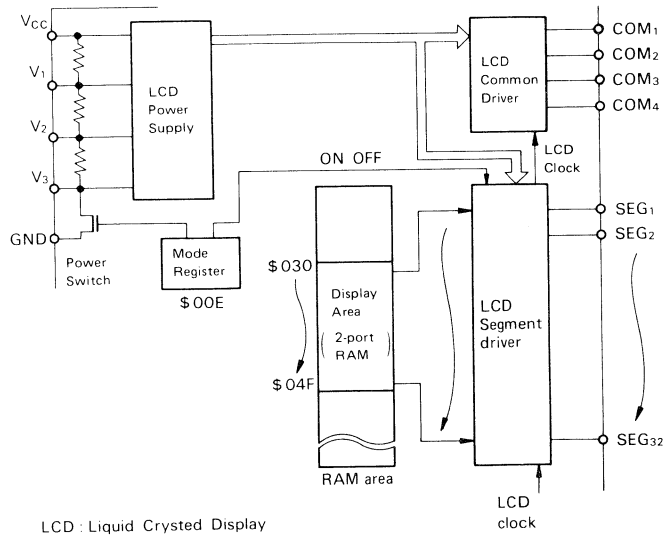
■ LIQUID CRYSTAL DISPLAY

The MCU contains the LCD driver which drive the LCD panel with 16 digits of 7 segments. Fig. 2-13 shows the LCD driver configuration. It consists of display data RAM, display control register and LCD drivers.

4 common signal pins, 32 segment signal pins and also 3 LCD power supply dividing resistors are provided for a 1/3-bias, 1/4-duty driving method. The display data RAM is 2-port accessible and read out data is automatically transferred to the driver without instruction. All these operations are synchronous with LCD clock (about 512 Hz). However, the system allows the LCD display even in the stop mode in which the system clock oscillator is halted, if 32 kHz clock oscillation is selected.

• LCD Mode Register (DISP : $00E)

A LCD mode register is 2-bit write only register. It controls ON/OFF of LCD power supply dividing resistors and the specification of LCD blanking as shown in Table 2-17. The LCD mode register is cleared to S0 by MCU reset. Table 2-18 describes the liquid crystal driving frame frequency and active/non active of the LCD in each mode.



LCD : Liquid Crysted Display

Fig. 2-13 LCD Driver Configuration

Table 2-17 Liquid Crystal Display Mode Register

DISP bit 3	LCD power switch
0	OFF
1	ON V3 goes to GND level.

DISP bit 2	Blanking
0	LCD RAM data is output as segment signal
1	Segment signal is inactive independently of the LCD RAM data.

Table 2-18 Display and Liquid Crystal Driving Frame Frequency in Each Mode

MCU Mode / OSC (Mask Option)	Active Mode	Stand-by Mode	Stop Mode
32 kHz Clock Timer	Atcive (128 Hz)	Active (128 Hz)	Active (128 Hz)
System Clock	Active (97 Hz)	Active (97 Hz)	Non Active (–)*

The number in the parenthesis indicates the liquid crystal driving frame frequency.
*If the system clock is selected, the display stop in the stop mode.

■ DTMF GENERATION CIRCUIT

The MCU provides an internal DTMF (Dual Tone Multi-Frequency) generation circuit. DTMF signal consists of two kinds of sine waves which is accessed to the switching system. Fig. 2-14 shows DTMF keypad and frequencies. Pressing one of the keys generates tones of two corresponding frequencies.

Fig. 2-15 shows a block diagram of DTMF circuit.

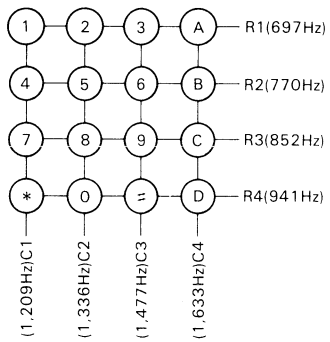


Fig. 2-14 DTMF Keypad and Frequencies

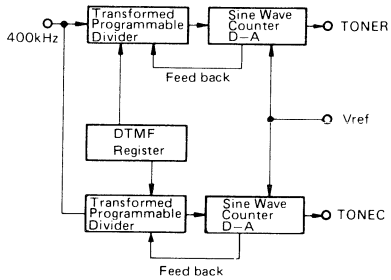


Fig. 2-15 Block Diagram of DTMF Circuit

The HD61827 uses oscillation frequency reduced to 400 kHz, a eighth of conventional one, to realize a low power consumption. In this case, the problem is a frequency deviation. The HD61827 provides transformed programmable dividers in addition to sine wave counters and a control register to reduce a frequency deviation.

The DTMF generation circuit is controlled by the following two registers.

- **DTMFR register (DTMFR : $00C)**

The DTMFR register is a 4-bit write-only register. It controls output frequencies as listed in Table 2-19, and is cleared to S0 by a MCU reset.

- **DTMFC register (DTMFC : $00D)**

The DTMFC register is a 3-bit write-only register. It controls start/stop of DTMF signal output as listed in Table 2-20, and is cleared to S0 by a MCU reset.

Table 2-19 DTMFR Register

DTMFR bit3	DTMFR bit2	DTMFR bit1	DTMFR bit0	Output Frequencies	
Option (TONER output is not affected.)		0	0	fR1 (: 967 Hz)	Output through TONER pin
		0	1	fR2 (: 770 Hz)	
		1	0	fR3 (: 852 Hz)	
		1	1	fR4 (: 941 Hz)	
0	0	Option (TONEC output is not affected.)		fC1 (: 1,209 Hz)	Output through TONEC pin.
0	1			fC2 (: 1,336 Hz)	
1	0			fC3 (: 1,477 Hz)	
1	1			fC4 (: 1,633 Hz)	

Table 2-20 DTMFC Register

DTMFC bit 3	TONEC Output Control
0	STOP
1	START (Active)

DTMFC bit 1	DTMF Enable Bit
0	DTMF Disable
1	DTMF Enable

DTMFC bit 2	TONER Output Control
0	STOP
1	START (Active)

- **DTMF Output**

The sine waves of low-group and high-group tones are output through DTMF output pins (TONER, TONEC). Before output, they are digital-to-analog converted in the D/A conversion circuit with high precision ladder resistance. Fig. 2-16 shows the TONE output equivalent circuit. Fig. 2-17 shows the output waveform. This waveform is stable with little distortion, as a cycle of the wave consists of 32 slots.

Table 2-21 details the frequency deviation of the HD61827 from standard DTMF signals.

- **COL Output Compensation**

The digitally controlled pre-emphasis can be given to COL output of the HD61827 by changing the output impedance with mask option depending on the frequencies. The COL output of the high-group frequencies attenuate when the CR filter of slow attenuation is attached to the DTMF output. In the HD61827, the output of high-group frequencies are pre-emphasized by lowering the output impedance of the low-group frequencies to compensate this attenuation. Fig. 2-18 shows the output levels of COL signals after the process of pre-emphasis.

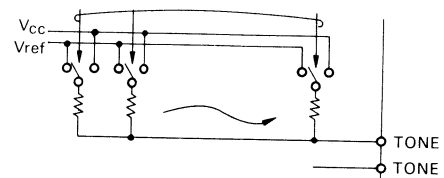


Fig. 2-16 Tone Output Equivalent Circuit

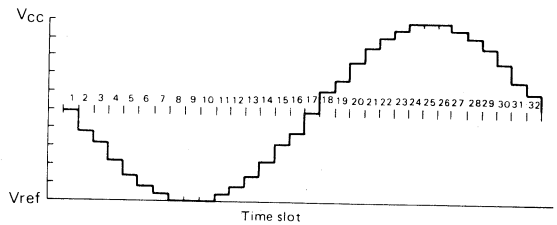


Fig. 2-17 Wave Form of Tone Output

Table 2-21 Frequency Deviation of the HD61827 from Standard

	Standard DTMF (Hz)	HD61827 (Hz)	Deviation from Standard (%)
R1	697	694.44	−0.37
R2	770	769.23	−0.10
R3	852	851.06	−0.11
R4	941	938.97	−0.22
C1	1,209	1,212.12	0.26
C2	1,336	1,333.33	−0.20
C3	1,477	1,481.48	0.30
C4	1,633	1,639.34	0.39

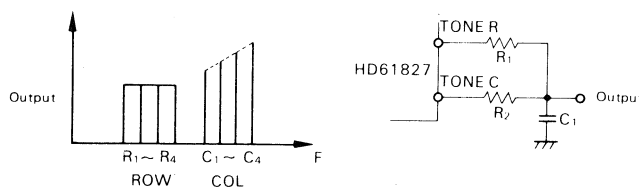


Fig. 2-18 Output Levels After COL Compensation and Peripheral Circuit

■ INPUT/OUTPUT

The MCU provides 32 Input/Output pins. Each pin may have one of three mask options: (A) "Without pull-up MOS (NMOS open drain)", (B) "With pull-up MOS", or (C) "CMOS".

When any Input/Output common pin is used as input pin, it is necessary to select the mask option and output data as shown in Table 2-22.

• D-port

D-port is 1-bit I/O port and it has 16 Input/Output common pins. It can be set/reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD and TDD instructions. Table 2-23 shows the classification of pins and the Input/Output pins circuit types. The mask option in Fig. 2-19 is available for D14/XI and D15/XO pins.

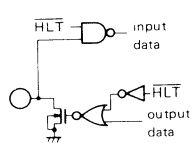
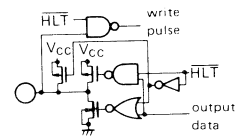
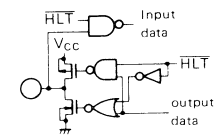
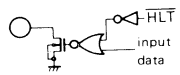
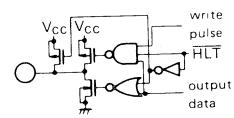
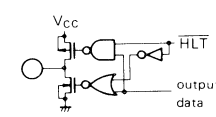
• R-port

R-port is 4-bit I/O port. It provides 12 input/output common pins and 4 output-only pins. Data input is processed using the LAR and LBR instructions and data output is processed using the LRA and LRB instructions. The MCU will not be affected by writing into non-existing ports, invalid data will be read by reading from the output-only and/or non-existing ports.

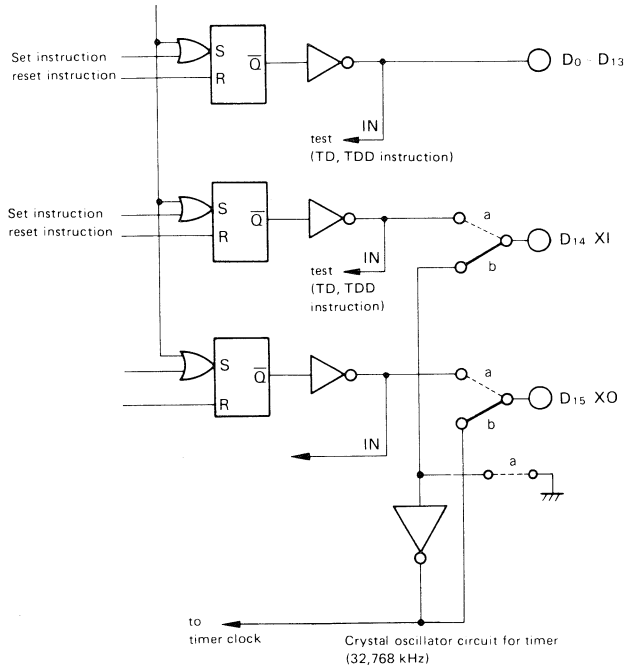
The R32 and R33 pins are also used as the $\overline{INT0}$ and $\overline{INT1}$ respectively. Table 2-23 shows the classification of pins and Input/Output pins circuit types.

Table 2-22 Data Input from Input/Output Common Pins

I/O Pin Circuit Type	Possibility of Input	Available Pin Condition for Input
CMOS	No	–
Without pull-up MOS (NMOS Open Drain)	Yes	"1"
With Pull-up MOS	Yes	"1"

	Without Pull-up MOS (NMOS Open Drain) (A)	With Pull-up MOS (B)	CMOS (C)	Applied pins
I/O Common Pins				D0 ~ D15 R10 ~ R33
Output Pins				R00 ~ R03

(Note) In the stop mode, $\overline{HLT}$ signal is "0" and I/O pins are in high impedance state.



Mask Option		ⓐ	ⓑ	Function of D14/XI, D15/XO	D14, D15 Function of Latch
①	Selects system clock. (No Crystal Oscillation for timer.)	Short	Open	Discrete I/O Common Pins	Output Latch
②	Selects crystal oscillation for Timer. (32.768 kHz)	Open	Short	Connecting Pin to Crystal Circuit	1-bit General Register

(Note) Specify this mask option in "HD61827 MASK OPTION LIST" when ordering ROM.

Fig. 2-19 Mask Option of D14/XI, D15/XO Pins

● **RESET**

The MCU is reset by setting RESET pin to "1". At power ON or recovering from stop mode, apply RESET input more than t to obtain the necessary time for oscillator stabilization. In other cases, the MCU reset requires at least two instructions cycle time of RESET input.

Table 2-24 shows initialized items by MCU reset and each status after reset.

Table 2-24 Initial Value by MCU Reset

Item			Initial value by MCU reset	Contents
Program counter (PC)			$0000	Execute program from the top of ROM address.
Status (ST)			"1"	Enable to branch with conditional branch instruction.
Stack pointer (SP)			$3FF	Stack level is 0.
I/O pin output register	D0 R10 ~ D15 R33	(A) Without pull-up MOS	"1"	Enable to input.
		(B) With pull-up MOS	"1"	Enable to input.
		(C) CMOS	"1"	—
	R00 ~ R03	(A) Without pull-up MOS	"1"	—
		(B) With pull-up MOS	"1"	—
		(C) CMOS	"1"	—
Interrupt flag	Interrupt Enable Flag (I/E)		"0"	Inhibit all interrupts.
	Interrupt Request Flag (IF)		"0"	No interrupt request.
	Interrupt Mask (IM)		"1"	Mask interrupt request.
Mode register	Port Mode Register (PMR)		"0000"	See Item "Port Mode Register".
	Timer Mode Register A (TMA)		"000"	See Item "Timer Mode Register A".
	Timer Mode Register B (TMB)		"0000"	See Item "Timer Mode Register B".
	DTMF Register	(DTMFR)	"0000"	See Item "DTMFR Register"/ "DTMFC Register".
		(DTMFC)	"0000"	
	LCD Mode Register (DISP)		"0000"	See Item "LCD Mode Register".
Clock timer	6-bit Divider		$00	—
	8-bit Prescaler		$00	—
Timer/Counter	Prescaler		$000	—
	Timer/Counter A (TCA)		$00	—
	Timer/Event Counter B (TCB)		$00	—
	Timer Load Register (TLR)		$00	—

(Note) MCU reset affects to the reset of registers as follows:

	After recovering from STOP mode by MCU reset or clock timer interrupt.	After MCU reset except for the left condition.
Carry (CA)	The contents of the items before MCU reset/clock timer interrupt are not retained. It is necessary to initialize them by software again.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.
Accumulator (A)		
B Register (B)		
W Register (W)		
X/SPX Register (X/SPX)		
Y/SPY Register (Y/SPY)		
RAM	The contents of RAM before MCU reset/clock timer interrupt (just before STOP instruction) are retained.	Same as above.

■ **Low Power Dissipation Mode**

The MCU provides two low power dissipation modes, that is, a Standby mode and a Stop mode. Table 2-25 shows the function of the low power dissipation mode, and Fig. 2-20 shows the diagram of the mode transition.

Table 2-25 Low Power Dissipation Mode Function

Mode		Setting Method	Recovering Method	Condition							Current Dissipation
				Oscillator Circuit	Instruction Execution	Input/Output Pin	LCD driver	DTMF	RAM	Register	
Standby		SBY Instruction	*Interrupt request *RESET imput	Active	Stop	Retained	Active	Active	Retained	Retained	Low
Stop	System Clock	Stop Introduction	RESET input	Stop	Stop	High	Stop	Stop	Retained	Cleared	Lowest
	32kHz		*Timer interrupt *RESET input	Active only 32kHz		impedance	Active				Lowest (LCD is available)

(Note) 1. The MCU recovers from STOP mode by RESET input or timer interrupt.
See Table 2-24 for the contents of the flags and registers after the recover from STOP mode by RESET input or timer interrupt.
In the latter case, the timer clock, the LCD mode register (DISP) and the interrupt flag are not initialized.

2. When selecting the system clock with the mask option, the switch of LCD power dividing register is turned OFF (V3~GND is open) independently of LCD mode register.

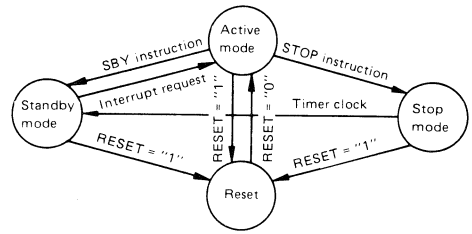


Fig. 2-20 MCU Operation Mode Transition

- **Standby Mode**

The SBY instruction puts the MCU into the Standby mode. In the Standby mode, the oscillator circuit is active and timer counter continues working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and Input/Output pins retain the state they had just before going into the Standby mode.

The Standby mode is cancelled by the interrupt request. When canceled by the interrupt request, the MCU becomes an active mode and executes the instruction next to the SBY instruction. At this time, if the Interrupt Enable Flag is "1", the interrupt is executed. If the Interrupt Enable Flag is "0", the interrupt request is held on and the normal instruction execution continues.

Fig. 2-21 shows the flowchart of the Standby Mode.

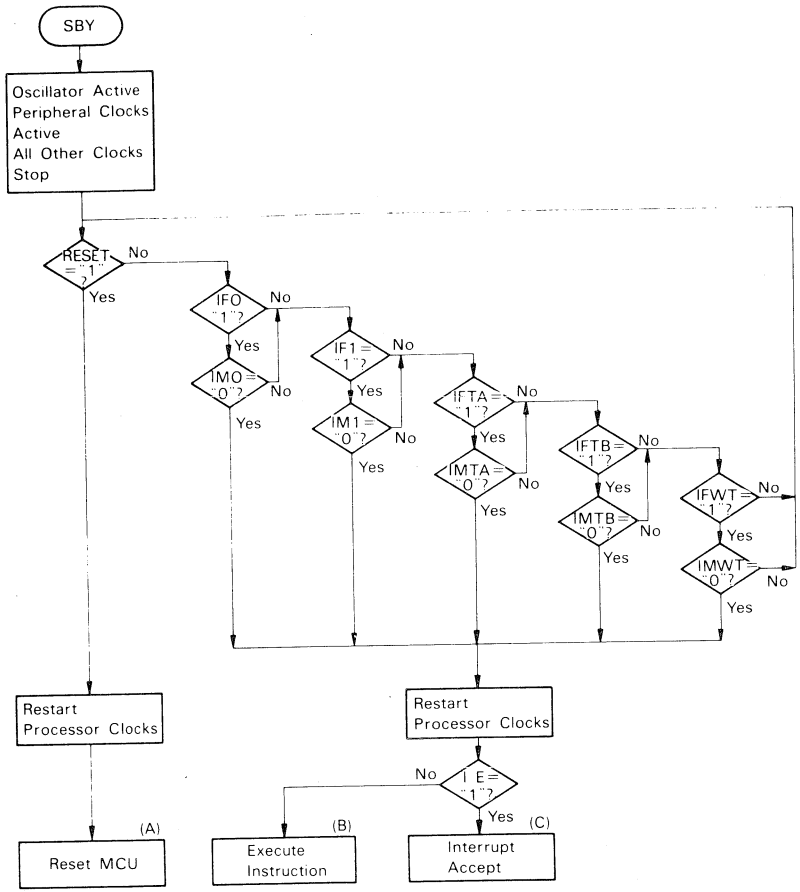


Fig. 2-21 MCU Operation Flowchart

• Stop Mode

The MCU is placed into the stop mode by the execution of STOP instruction.

In the stop mode, the system clock oscillator stops and all functions of the MCU are halted. The MCU leaves the stop mode by RESET input or timer interrupt. RESET should be input for more than oscillator stabilization time (t_{RC}) (usually 20 ~ 100 ms).

The contents of RAM before entering the stop mode is unaffected by the stop mode, while those of the accumulator, B register, W register, X, SPX register and Y, SPY register are affected.

■ INTERNAL OSCILLATION CIRCUIT

The internal oscillation circuit consists of the 400 kHz system clock ceramic oscillation circuit and the 32 kHz watch timer X'tal oscillation circuit (mask option).

In general, the oscillation circuit is considerably affected by the external noise. Therefore, the shortest possible wiring is necessary between the oscillation pins (OSC_1, OSC_2, XI, XO) and the resonator/the external parts to prevent the crossing with other wires.

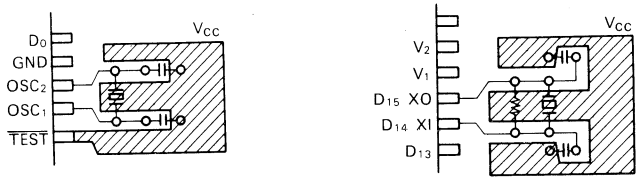


Fig. 2-22 Examples of Oscillation Circuit Configuration

3. INSTRUCTIONS

The HD61827 has the same architecture with the HMCS400 series and is software compatible with them except STS instruction for serial I/O which is not implemented.

■ RAM ADDRESSING MODE

As shown in Fig. 3-1, the MCU provides three RAM addressing modes; Register Indirect Addressing, Direct Addressing and Memory Register Addressing.

● Register Indirect Addressing

The combined 10-bit contents of W Register, X Register and Y Register is used as the RAM address in this mode.

● Direct Addressing

The direct addressing instruction consists of two words and the second word (10 bits) following Op-code (the first word) is used as the RAM address.

● Memory Register Addressing

The Memory Register Addressing can access 16 digits (Memory Register: MR) from S020 to S02F by using the LAMR and XMRA instructions.

■ ROM ADDRESSING MODE AND P INSTRUCTION

The MCU has four kinds of ROM addressing modes as shown in Fig. 3-2.

● Direct Addressing Mode

The program can branch to any addresses in the ROM memory space by using JMPL, BRL or CALL insturciton. These instructions replace 14-bit program counter (PC_{13} to PC_0) with 14-bit immediate data.

● Current Page Addressing Mode

ROM memory space is divided into 256 words in each page starting from S0000. The program branches to the address in the same page using BR instruction. This instruction replaces the low-order eight bits of program counter (PC_7 to PC_0) with 8-bit immediate data. The branch destination by BR instruction on the boundary between pages is in the next page. Refer to Fig. 3-4.

● Zero Page Addressing Mode

The program branches to the zero page subroutine area, which is located on the address from S0000 to S003F, using CAL instruction. When CAL instruction is executed, 6-bit immediate data is placed in low-order six bits of program counter (PC_5 to PC_0) and "0"s are placed in high-order eight bits (PC_{13} to PC_6).

Table Data Addressing

The program branches to the address determined by the contents of the 4-bit immediate data, accumulator and B register, using TBR instruction.

● P Instruction

The P instruction refers ROM data addressed by Table Data Addressing. ROM data addressed also determine its destination. When bit 8 in referred ROM data is "1", 8 bits of referred ROM data are written into the accumulator and B Register. When bit 9 is "1", 8 bits of referred ROM data are written into the R1 and R2 port output register. When both bit 8 and 9 are "1", ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

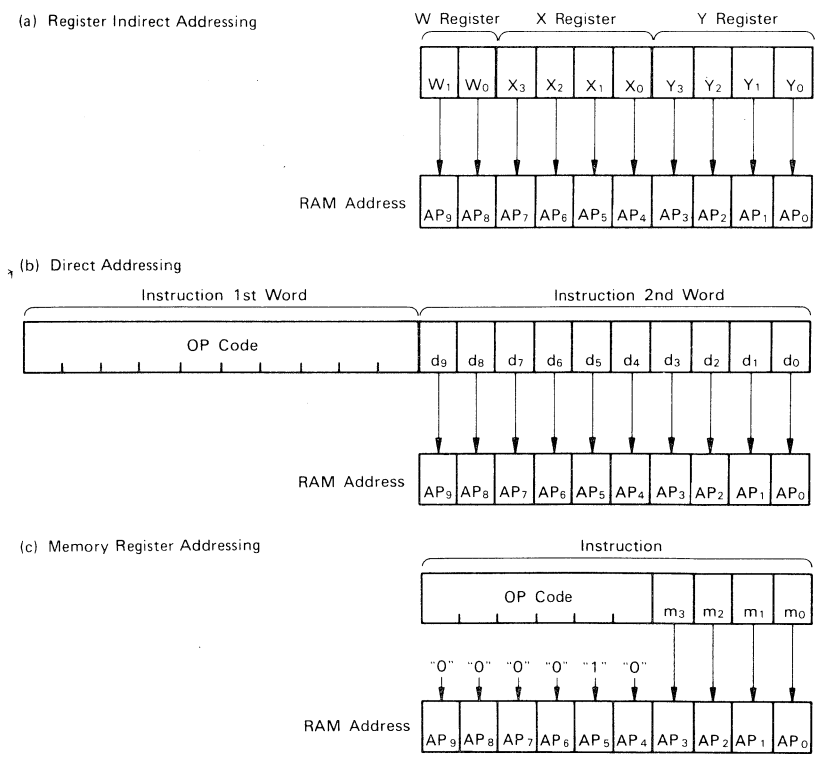
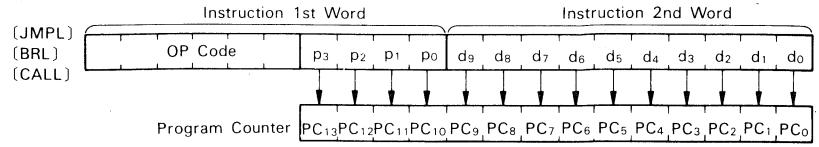
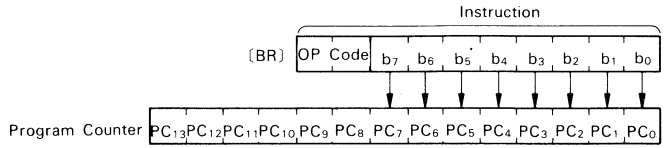


Fig. 3-1 RAM Addressing Mode

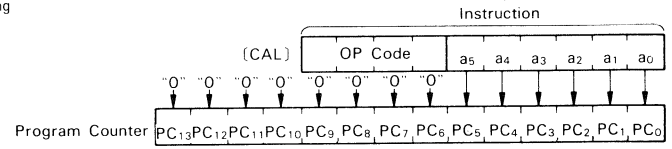
(a) Direct Addressing



(b) Current Page Addressing



(c) Zero Page Addressing



(d) Table Data Addressing

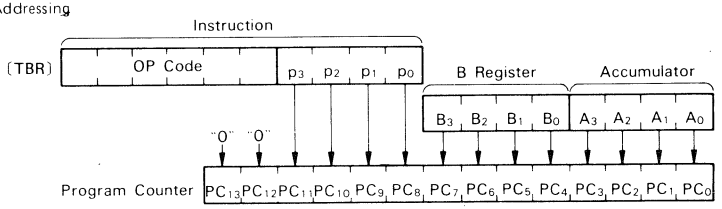
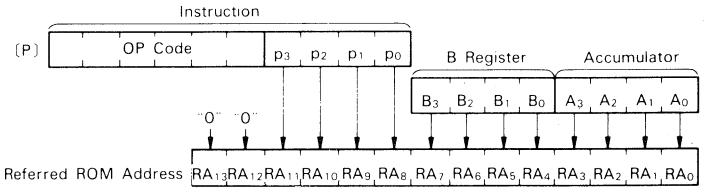
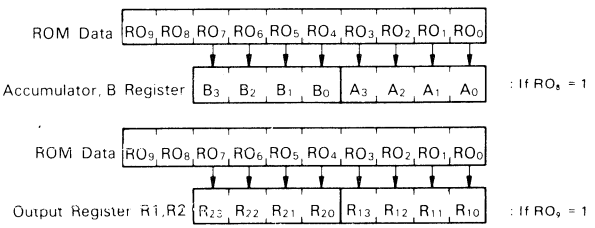


Fig. 3-2 ROM Addressing Mode



(a) Address Designation



(b) Pattern Output

Fig. 3-3 P Instruction

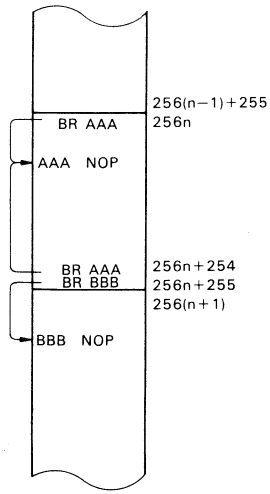


Fig. 3-4 The Branch Destination by BR Instruction on the Boundary Between Pages

- **Description of the Branch Destination on Page Boundary**

When BR is on page boundary (256n + 255), BR instruction transfers the contents of PC to the next page with hardware architecture. Therefore, the program branches to the next page when using BR on page boundary. The HMCS400 series cross macro assembler has automatic paging facility for ROM page.

■ INSTRUCTION SET

The HMCS400 series provides 99 instructions. These instructions are classified into 10 groups as follows:

(1) Immediate Instruction
(2) Register-to-Register Instruction
(3) RAM Address Instruction
(4) RAM Register Instruction
(5) Arithmetic Instruction
(6) Compare Instruction
(7) RAM Bit Manipulation Instruction
(8) ROM Address Instruction
(9) Input/Output Instruction
(10) Control Instruction

Table 3-1 Immediate Instruction

Operation	Mnemonic	Operation Code	Function	Status	WORD / CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i→A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i→B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i→M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i→M, Y+1→Y	NZ	1/1

Table 3-2 Register-to-Register Instruction

Operation	Mnemonic	Operation Code	Function	Status	WORD / CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B→A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A→B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y→A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX→A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY→A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m)→A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m)←→A		1/1

Table 3-3 RAM Address Instruction

Operation	Mnemonic	Operation Code	Function	Status	WORD / CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	i→W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	i→X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	i→Y		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A→X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A→Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y + 1→Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y - 1→Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y + A→Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y - A→Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X←→SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y←→SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X←→SPX, Y←→SPY		1/1

Table 3-4 RAM Register Instruction

Operation	Mnemonic	Operation Code	Function	Status	Word / Cycle
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, ($^{X\leftarrow\rightarrow SPX}_{Y\leftarrow\rightarrow SPY}$)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M→A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, ($^{X\leftarrow\rightarrow SPX}_{Y\leftarrow\rightarrow SPY}$		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, ($^{X\leftarrow\rightarrow SPX}_{Y\leftarrow\rightarrow SPY}$)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A→M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X←→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y-1→Y (X←→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M←→A, ($^{X\leftarrow\rightarrow SPX}_{Y\leftarrow\rightarrow SPY}$)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M←→A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M←→B, ($^{X\leftarrow\rightarrow SPX}_{Y\leftarrow\rightarrow SPY}$)		1/1

(Note) (XY) and (X) have the meaning as follows:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each. (example of LAM (XY) is given below.)

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X ←→ SPX
LAMY	1	0	Y ←→ SPY
LAMXY	1	1	X ←→ SPX, Y ←→ SPY

(2) The instructions with (X) have 2 mnemonics and 2 object codes for each. (example of LMAIY(X) is given below.)

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X ←→ SPX

Table 3-5 Arithmetic Instruction

Operation	Mnemonic	Operation Code	Function	Status	Word / Cycle
Add Immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A+i→A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1→B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B−1→B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A}$+1→A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B}$→B		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1→CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0→CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A→A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A→A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA→A OVF→CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A+CA→A OVF→CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M−A−$\overline{CA}$→A NB→CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M−A−$\overline{CA}$→A NB→CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A∪B→A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A∩M→A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A∩M→A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A∪M→A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A∪M→A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A⊕M→A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A⊕M→A	NZ	2/2

Table 3-6 Compare Instruction

Operation	Mnemonic	Operation Code	Function	Status	Word / Cycle
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≦ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≦ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≦ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≦ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≦ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≦ i	NB	1/1

Table 3-7 RAM Bit Manipulation Instruction

Operation	Mnemonic	Operation Code	Function	Status	Word / Cycle
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1→M(n)		1/1
Set Memory Bit	SEMD n, d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1→M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0→M(n)		1/1
Reset Memory Bit	REMD n, d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0→M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n, d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 3-8 ROM Address Instruction

Operation	Mnemonic	Operation Code	Function	Status	Word / Cycle
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1→I/E CA RESTORE	ST	1/3

Table 3-9 Input/Output Instruction

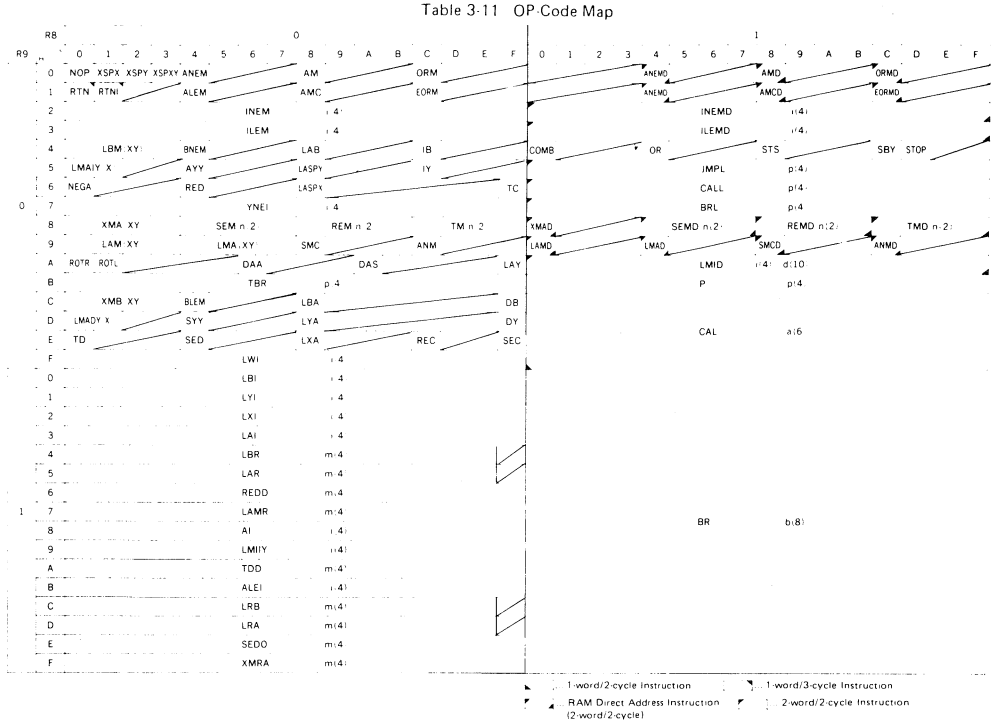
Operation	Mnemonic	Operation Code	Function	Status	Word / Cycle
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1→D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1→D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0→D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0→D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m)→A		1/1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m)→B		1/1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A→R(m)		1/1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B→R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 3-10 Control Instruction

Operation	Mnemonic	Operation Code	Function	Status	Word / Cycle
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Stand-by Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

☆ STS instruction is not used in the HD61827.

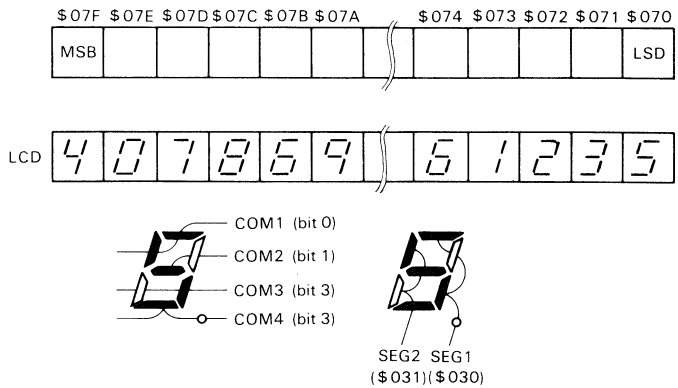
Table 3-11 OP-Code Map



4. APPLICATIONS

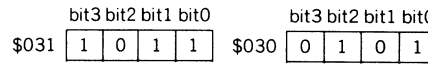
■ AN EXAMPLE OF LIQUID CRYSTAL DRIVING

The LCD driver of the HD61827 can display 16-digit BCD data of locations $070 through $07F in decimal notation. Each decimal number is displayed with 7 segments.



The data for segment display are stored in the ROM pattern area. The pattern data is loaded from this area into the accumulator and B register, and then written into the display data area (locations $030 – $04F) by pattern generation instruction .

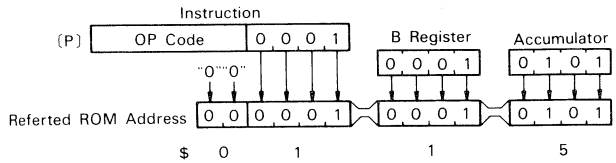
For example, let's assume that binary data $(0101)_2$ ("5" in decimal notation) is stored in location $070. The followings are segment signals which display "5" on the LCD panel.



If $115 is a pattern data address of "5", the upper signals are stored there as follows.

	Control		Data for segment display							
	r_9	r_8	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0
$115	0	1	1	0	1	1	0	1	0	1

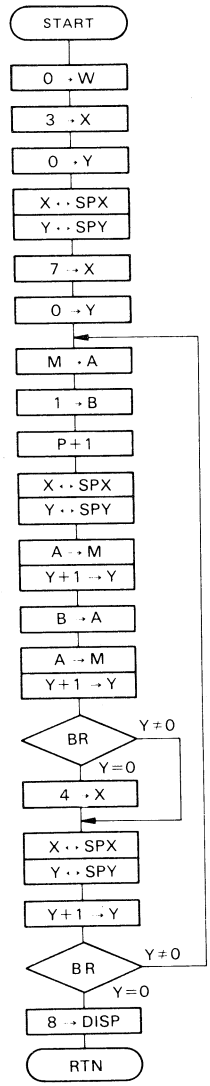
$(01)_2$ in the control part means that the pattern data r_7 through r_0 are output to the accumulator and the B register. Address $115 should be specified as shown in the following figure. The pattern address is specified using the accumulator, the B register and the direct address in the pattern generation instruction. In this case, $1 and $5 have been previously loaded into the B-register and the accumulator respectively by an instruction, and the direct address $1 in the pattern generation instruction is used to complete the pattern address.



Allocation of ROM Pattern Area

Address	Control		Segmen Data								Display Character
	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	
$110	0	1	1	1	0	1	0	1	1	1	0
111	0	1	0	0	0	0	0	1	1	0	1
2	0	1	1	1	1	0	0	0	1	1	2
3	0	1	1	0	1	0	0	1	1	1	3
4	0	1	0	0	1	1	0	1	1	0	4
5	0	1	1	0	1	1	0	1	0	1	5
6	0	1	1	1	1	1	0	1	0	0	6
7	0	1	0	0	0	0	0	1	1	1	7
8	0	1	1	1	1	1	0	1	1	1	8
9	0	1	0	0	0	1	0	1	1	1	9
A	0	1	0	0	0	0	0	0	0	0	

- **PROGRAM FLOWCHART**

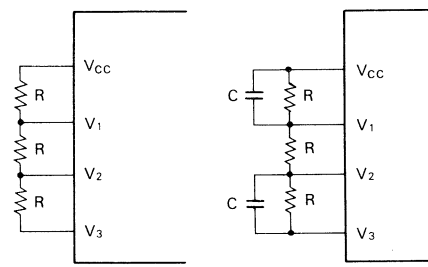



```
(Label)   (OP)     (Operand)    (Comment)
          LWI      $0
          LXI      $3
          LYI      $0
          XSPXY
          LXI      $7
          LYI      $0
IF        LAM
          LBI      $1
          P        $1
          XSPXY
          LMAIY
          LAB
          LMAIY
          BR       ID           File 3,4 side
          LXI      $4
ID        XSPXY
          IY
          BR       IF           File 7 side
          LMID     $8,00E       LCD ON
          RTN
```

■ LARGE LCD PANEL DRIVING AND DRIVING VOLTAGE (V_{LCD})

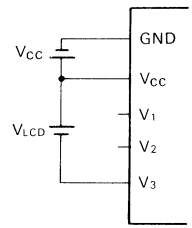
When using the large LCD panel, lower the dividing resistance by implementing the external resisters parallel to the internal dividing resistors. (See the following figure.)

Since the liquid crystal display board is of matrix configuration, the path of the charge/discharge current through the load capacitors is very complicated. Moreover, as it varies depending on display condition, a value of resistance cannot be simply determined by referring to the load capacitance of liquid



crystal display. It must be experimentally determined according to the demand for power consumption of the equipment in which the liquid crystal display is implemented. (A capacitor can be used if necessary.) In general, R is 1 kΩ ~ 10 kΩ.

The following figure shows a connection when changing the liquid crystal driving voltage (V_{LCD}). In this case, power supply switch for dividing resistor should be turned OFF. (Bit 3 of DISP resistor should be cleared.)



$V_{CC} \geqq V_{LCD} \geqq GND$

- **HD61827 MASK OPTION LIST**
- **Check the following items of selected specification with (■/X/V).**

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	HD

Pin	Input/Output	I/O Option				Pin	Input/Output	I/O Option		
		A	B	C	D			A	B	C
D_0	Input/Output					R_{00}	Output			
D_1	Input/Output					R_{01}	Output			
D_2	Input/Output					R_{02}	Output			
D_3	Input/Output					R_{03}	Output			
D_4	Input/Output					R_{10}	Input/Output			
D_5	Input/Output					R_{11}	Input/Output			
D_6	Input/Output					R_{12}	Input/Output			
D_7	Input/Output					R_{13}	Input/Output			
D_8	Input/Output					R_{20}	Input/Output			
D_9	Input/Output					R_{21}	Input/Output			
D_{10}	Input/Output					R_{22}	Input/Output			
D_{11}	Input/Output					R_{23}	Input/Output			
D_{12}	Input/Output					R_{30}	Input/Output			
D_{13}	Input/Output					R_{31}	Input/Output			
D_{14}/XI	Input/Output					R_{32}	Input/Output			
D_{15}/XO	Input/Output					R_{33}	Input/Output			

(Note 1) I/O Circuit Type
A : Without Pull-up MOS (NMOS Open Drain)
B : With Pull-up MOS
C : CMOS
D : Timer Clock (32 kHz) Oscillation Pins

(Note 2) There is no selection for hatched part.

Vref		DTMF COL Compensation		Timer Clock (32 kHz)	
Internal	External	Yes	No	Yes	No

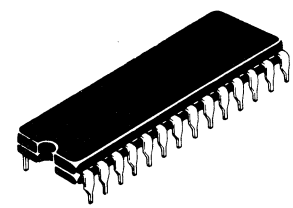
HD61885, HD61887

Single-chip Speech Synthesis LSI

To broaden the use of speech synthesizing LSIs, Hitachi has developed a single-chip CMOS speech chip, the HD61885, which utilizes PARCOR techniques.

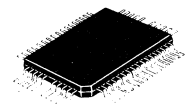
The existing three-chip PMOS LSIs consists of speech chip the HD38880, a microprocessor, and a speech synthesizing ROM (HD38881). By comparison the HD61885 has various functions particularly suited for simpler, low-power-consumption, short-speech systems. Of course, its functions are extendable, like the HD38880, when a medium- to high-class systems calls for longer speech. The HD61885 can make up a speech unit for a wide variety of systems, from the very simple to the truly sophisticated.

HD61885



(DP-28)

HD61887



(FP-54)

■PRODUCT OUTLINE

To digitally model man's vocalizing mechanism is divided into the HD61885 seven sections. A sound source, which corresponds to the vocal cords, a digital filter corresponding to the vocal path, and a ROM that memorizes how the vocal path changes with time. In addition, it incorporates an inverter a keyboard interface circuit, a microprocessor interface circuit, and an external ROM interface circuit.

The HD61885 is a single-chip CMOS LSI speech synthesizing device that is easy to use, extendable, and low power.

Incorporating a 32k-bit ROM (capable of producing vocal sound for 20 seconds maximum), the HD61885 can serve small systems in one chip. For medium and large systems, it can be extended by use of external ROM and microprocessor. With this versatility, the HD61885 is fitted for many uses, such as watches, portable calculators, toys, teaching machines, alarm devices, and guide systems.

■SYSTEM SPECIFICATIONS

Description	Specifications
Process type	PARCOR
Vocal path model	10-stage digital filter
Sampling frequency	10kHz
Bit rate	1.25 to 9.9k-bit/sec.
Bit/frame	50-bit/99-bit
Frame period	10ms/20ms
Variable vocalization speed	−25%, 0%, +25%
Vocalization time	20 sec. max. (incorporated ROM) 80 sec. max. per external ROM (HD44881) ; connectable to up to 16 ROMs
No. of words producible	63 words max. (incorporated ROM) (Extensible with microprocessor and external ROM)
Power supply	Single 5V power supply (variable between 3.6V and 5.5V)

■ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Rating	Unit	Remarks
Supply voltage	V_{CC}	−0.3 to +6.7	V	
Terminal voltage	Vt	−0.3 to V_{CC} +0.7	V	
Operating temperature (1)	Topr1	−20 to +75	°C	Vocalizable range
Operating temperature (2)	Topr2	−10 to +55	°C	CPG ± 3% guaranteed
Storage temperature	Tstg	−55 to +125	°C	

ELECTRICAL CHARACTERISTICS (Ta −20 to +75°C, Vcc +5V ± 10%)

Description	Symbol	Test Condition	min	typ	max	Unit	Remarks
Input voltage	$V_{IH}1$		Vcc − 1.0			V	
	$V_{IL}1$				1.0	V	
	$V_{IH}2$		Vcc − 1.0			V	
	$V_{IL}2$				1.0	V	
Pull up MOS	I_{PULL}	V_{IN} = Vcc	30		100	μA	RST, TEST
		V_{IN} = GND	30		100	μA	ROMA1 4, ACS, PS1−PS6
Output voltage	V_{OL}	I_{OL} = 1.6mA			0.8	V	Output other than DAO
	$V_{OH}1$	I_{OH} = −1.0mA	2.4			V	Output other than DAO
	$V_{OH}2$	I_{OH} = −0.1mA	Vcc − 0.8			V	Output other than DAO
Signal generating clock frequency	f_{CP}	CPA terminal	194	200	206	kHz	Ta = −10 to +55°C
Input leakage current	± I_{IN}	V_{IN} = 0 to Vcc			1	μA	Pull-up-free terminal
D/A output voltage	V_{OS}	R_L = 50Ω	0.25	0.5		Vp-p	
Power consumption	Pd			2.5		mW	Excluding consumption at D/A
Standby current	I_{SC}				10	μA	STRT BUSD Vcc−0.2V

CHARACTERISTIC

- Lower Power Consumption

Thanks to the CMOS process and standby mode, the HD61885 assures low power consumption. The power is supplied from a single 5V source (variable down to 3.6Vmin).

- Single-chip System

Incorporating a PARCOR-type speech synthesizer, a 9-bit D/A converter, and a 32k-bit sound data ROM vocalization time 26 sec. max.), the HD61885 LSI is capable of producing vocal sound in one chip.

- Extensibility

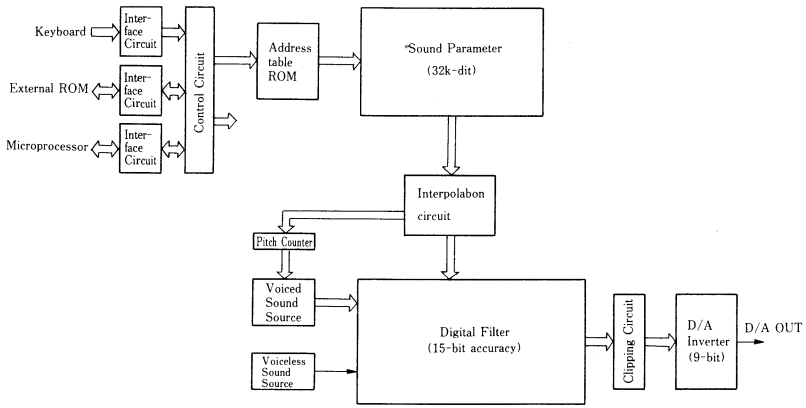
The vocalization time can be extended with ease by attaching exclusive sound ROM (HD44881: 128k-bit CMOS mask ROM). Each ROM can produce vocal sound for 100 seconds maximum, and as many as up to 16 ROMs can be connected directly. The number of words produced can be increased by using an encoder (63 words max.) or a microprocessor (limitless).

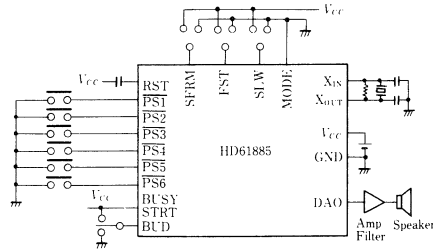
- High Sound Quality

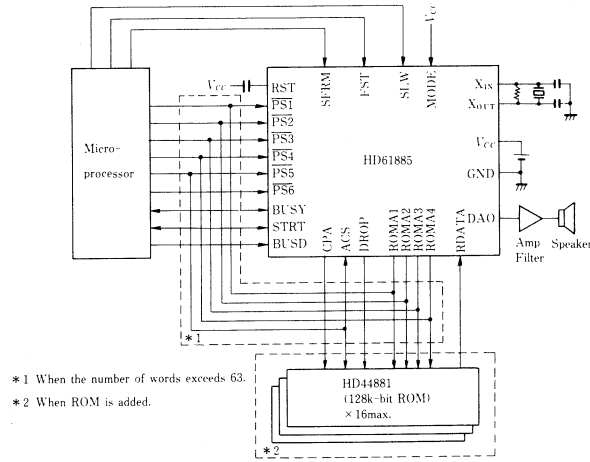
Providing a choice of different bit rates (from 1.25 to 9.9k-bit/sec.), the HD61885 can produce various levels of high-quality sound suited for different uses. Various unique sound-improving measures are introduced in the sound source, interpolator, and so on.

- Versatility

Complete with keyboard-, microprocessor- and external ROM-interface circuits, the HD61885 can be used for a wide variety of applications, from single-chip vocalization to edited vocalization employing microprocessor and external ROM. It also has a speech speed varying function and an interrupting function that enables vocalizing other phrase in the course of a speech. The HD61887, mounted on a small package (FPP-54), too is available for use in small devices.







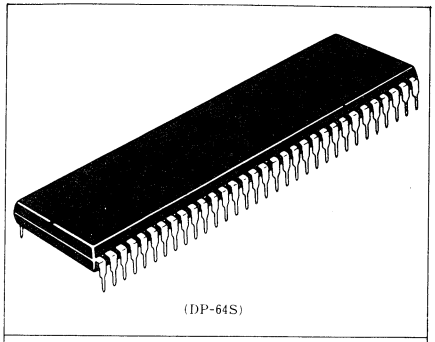
*1 When the number of words exceeds 63.

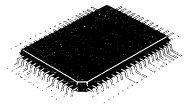
*2 When ROM is added.

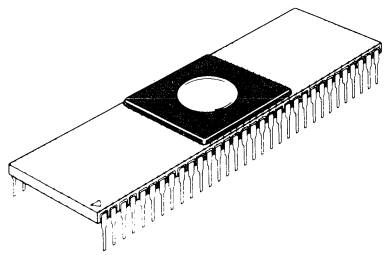
HMCS4008-ZTAT ——— Under Development

HMCS400 Series ZTAT Microcomputer

The HMCS4008-ZTAT is single chip microcomputer unit which includes 8K words of PROM and 512 digits of RAM.
On chip PROM can be programmed by the same procedure as that of 27256 (Vpp=12.5V).
The HMCS4008-ZTAT is a member of the HMCS400 series with powerful and efficient programming architecture.


(DP-64S)


(FP-64)

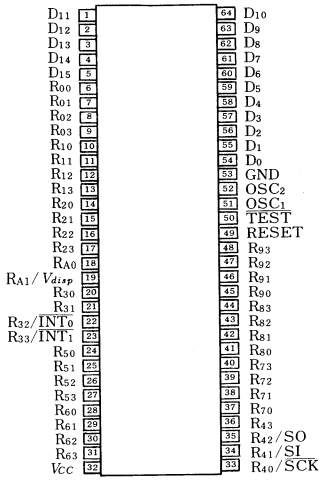

(DC-64S)

■FEATURES

- Instruction Set is compatible with HMCS402/404/408
- 8192 Words x 10 bit PROM
- 512 Digits x 4 bit RAM
- 58 I/O Pins, including 12 large current I/O pins (15 mA)
  [I/O Pin Circuit Type is all open drain]
- Two Timer/Counters
- Clock Synchronous 8 bit Serial Interface
- Five Interrupts
  - External 2
  - Internal 3
- Subroutine Stack
  - Up to 16 levels including interrupts
- Two Low Power Dissipation Modes
  - Standby Mode
  - Stop Mode
- On chip Oscillator
  - External Connection of Crystal or Ceramic Filter (externally drivable)
- Minimum Instruction Execution Time 0.89 μs
- Operation Mode
  - MCU Mode
  - PROM Mode
- Package
  - Shrink Type 64 pin Plastic DIP
  - Shrink Type 64 pin Ceramic DIP with window
  - 64 pin Flat Plastic Package

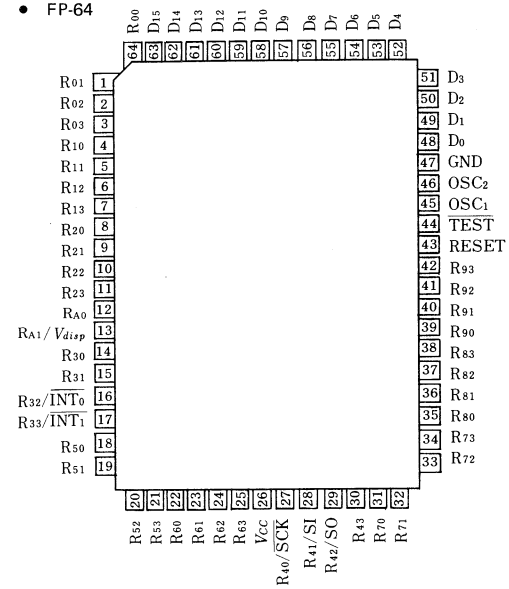
■PIN ARRANGEMENT

- DP-64S, DC-64S



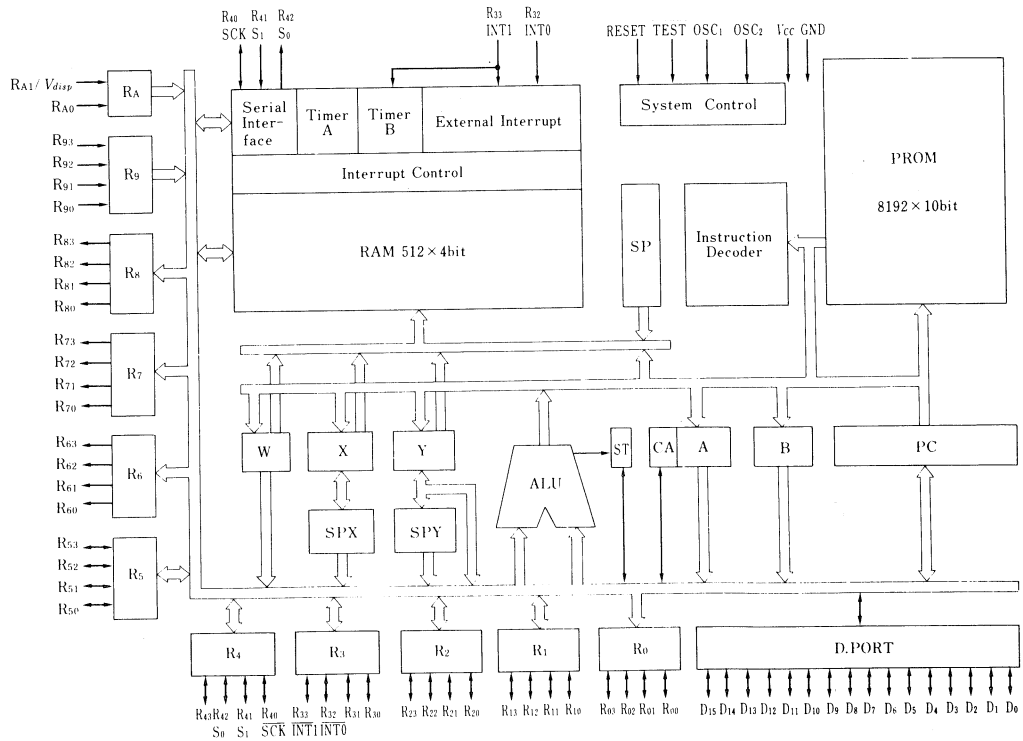
(Top View)

- FP-64



(Top View)

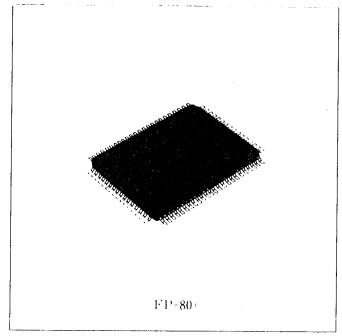
■BLOCK DIAGRAM



HMCS4608,HMCS4608-ZTAT

Under Development

4-Bit Single-chip Microcomputer with DTMF and LCD Controller/Driver



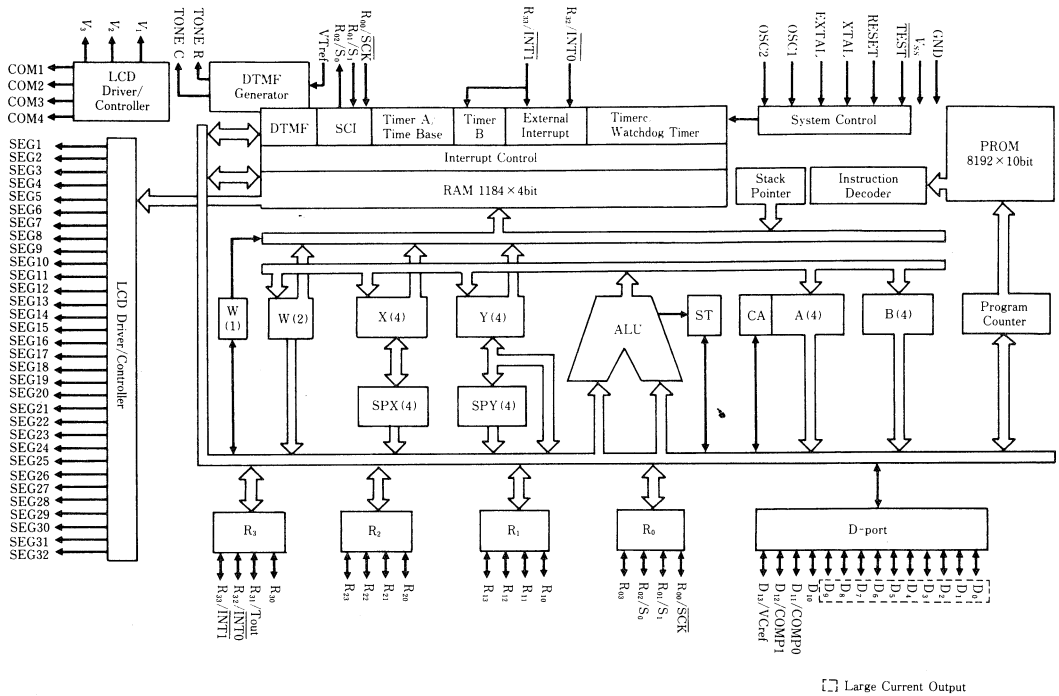
■HARDWARE FEATURES

- 4-bit Architecture
- 8,192 Words x 10-bit PROM
- 1,184 Digits x 4-bit RAM
- 30 I/O Pins
  - 26 input/output Pins, including 10 large current I/O pins (15mA)
  - 4 input pins, including 2 analog input pins which enables to change the threshold voltage
- DTMF Generation Circuits
- 16 Digits LCD Driver Circuit
  (4 COM Pins, 32 SEG Pins, Static, 1/2, 1/3, 1/4 Duty)
- Three Timer/Counters
  - 8-bit Free Running Timer/TIME BASE
  - 8-bit Auto-Reload Timer/Event Counter
  - 8-bit Auto-Reload Timer/Watch Dog Timer
- Clock Synchronous 8-bit Serial Interface
- Six Interrupts
  - External 2 ($\overline{INT_0}$, $\overline{INT_1}$)
  - Timer/Counter 3 (TIMERA/TIME BASE, TIMERB, TIMERC
  - Serial Interface 1 (SCI)
- Clock Function (32 kHz Crystal Oscillation)
- 2 channel Voltage Comparator
- Subroutine Stack
  - Up to 16 Levels Including Interrupt
- Minimum Instruction Execution Time
  - 10 μs; DTMF used
  - 2 μs; DTMF not used
- Power Voltage Range V_{CC} = 2.5 to 5.5 [V] (MASK-version only)
  (Instruction Execution Time 10 μs only)

■SOFTWARE FEATURES

- Instruction Set Similar to and More Powerful than HMCS400 Series;
  101 Instructions
- High Programming Efficiency with 10-bit ROM/Words;
  79 instructions are single-word instructions
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area (Bank Select)
- Subroutine Nesting Up to 16 Levels Incuding Interrupt
- Binary and BCD Arithmetic Operation
- Powerful Logical Arithmetic Operation
- Pattern Generation — Table Lock Up Capability —
- Bit Manipulation for Both RAM and I/O

■BLOCK DIAGRAM



Document Image Processor

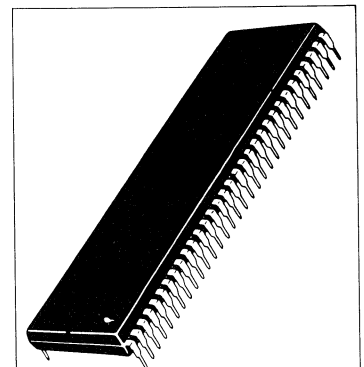
Document Image Preprocessor (DIPP)

CCD image sensors or other optical sensing devices used in the image reading block of facsimiles generate shading distortion of data. The DIPP is used to solve this problem.

During reading of image data (that is, in read(T) mode), this LSI takes analog image data via a sensing device, corrects distortion included in the data, digitizes the corrected data, and then transfers the digitized data to the MPU system. The digitized data can be reduced before transferring the data to the MPU system.

When receiving image data via MODEM (that is, in receive(R) mode), the DIPP can also perform transfer of data from the MPU system to the recorder. The data can be magnified before being transferred.

The DIPP performs the above functions in response to the user's program.



(DP-64S)

■KEY FEATURES

- High speed reading of image signals

  The DIPP can read image signals with a speed of up to 5M pels per second (when the input clock frequency is 10MHz). This speed is 5 times faster than that of the VPP.

- Highly accurate processing of image signal

  - o The peak to peak voltage of input image signals ranges from 0.1V to 2V. The highest permissible voltage of the input image signal is VDD, which is, however, clamped to 2V in the internal sample and hold circuit.
  - o The DIPP includes a peak value detection circuit with resolution of 8 bits, 7-bit successive approximation A/D and D/A converters, a 4-bit flash A/D converter, a 4-bit D/A converter and a shading wave RAM to perform highly accurate correction of distortion.
  - o The DIPP can perform distortion correction for each pel with a resolution of 1% using an external pel correction RAM.

- Various digitization modes

  The DIPP has three modes to digitize read image data: binary coding, dithered coding and 4-bit coding.

  Binary coding : Converts the read signal to 1 or 0 by using a slice level selected by the user.

  Dithered coding : Generates 16 gradations of dummy halftones by using a 4 × 4 dither pattern specified by the user.

  4-bit coding : Generates 16 gradations of real halftones in the format of 4 bits per pel.

- Wide range of programmable reduction or magnification ratios

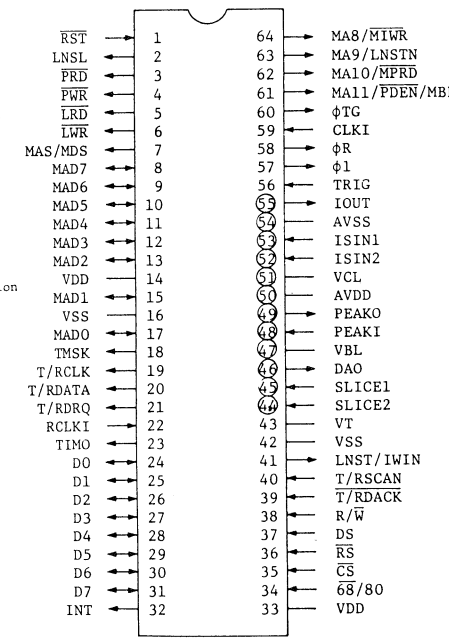
  The DIPP can reduce image data in read(T) mode. The reduction ratio is programmable in about 1000 increments from 0.125 to 1.

  The DIPP can magnify image data in receive(R) mode. The magnification ratio is programmable in about 1000 increments from 1 to 8.

- Automatic determination of vertical resolution

  The DIPP counts the amount of changing pels along a scan line or between two scan lines. The result of the counting appears in a flag bit of the internal status register. In response to the status of this flag bit,

■PIN ARRANGEMENT



(Note)

1. (44) to (55) : These are analog pins.
2. No lines should be connected to pin 43.

This data only introduces an outline of the function. Please see the user's manual for details.

the user can have the DIPP perform vertical resolution conversion, which allows shortening of the data transmit time.

- Burst DMA transfer of image data

By using the line memory, the DIPP can transfer a line of digitized data at a stretch in burst DMA mode. This function allows the DIPP to be used in ultra high speed systems.

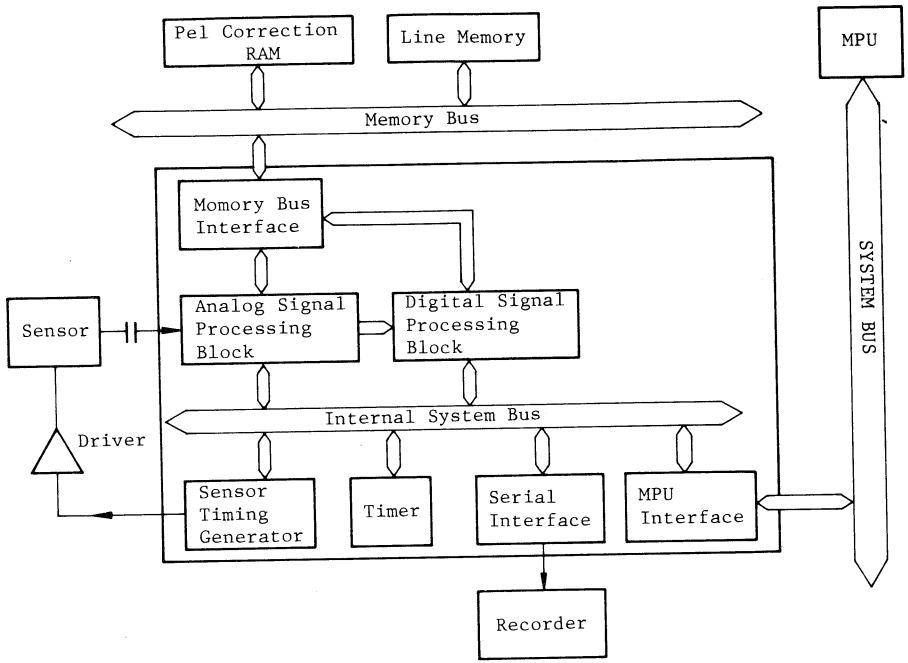
- Internal sensor interface

The DIPP incorporates a sample and hold circuit which is directly connected to the sensor via a coupling capacitor. This LSI also incorporates the sensor timing generator which generates control signals for the sensors.

■SPECIFICATIONS

Item	Specifications
Input Clock frequency	1MHz to 10MHz
Image signal reading frequency (Operating frequency)	500kHz to 5MHz
Input image signal Vp-p	0.1 to 2.0V
Shading distortion correction range	70% of signal peak
Scan line length	64 to 5,280 pels
Sensor driving frequency	8,125 clocks per image signal clock
Half tone	16 gradations
Dithered pattern	4 × 4 dithered matrix
Horizontal resolution conversion (reduction & magnification)	0.125 to 8.00 times
Maximum DMA data transfer speed	System bus ... 0.625M byte/sec Memory bus ... 5M byte/sec
Serial data transfer speed	5M-bit/sec
Interruption of MPU	o At completion of writing white image data waveform into the shading wave RAM o At completion of writing a line of image data to the external line memory
Supply voltage	5V ± 5%
Process technology	2.5μm CMOS
Power consumption	300mW (max.)
Package	Plastic shrink 64-pin DIP

■BLOCK DIAGRAM

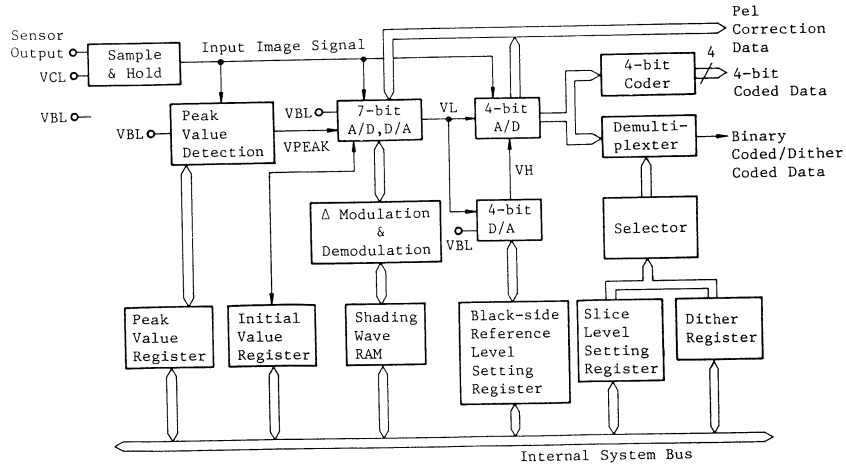


● Analog Signal Processing Block

The functions of this block are:

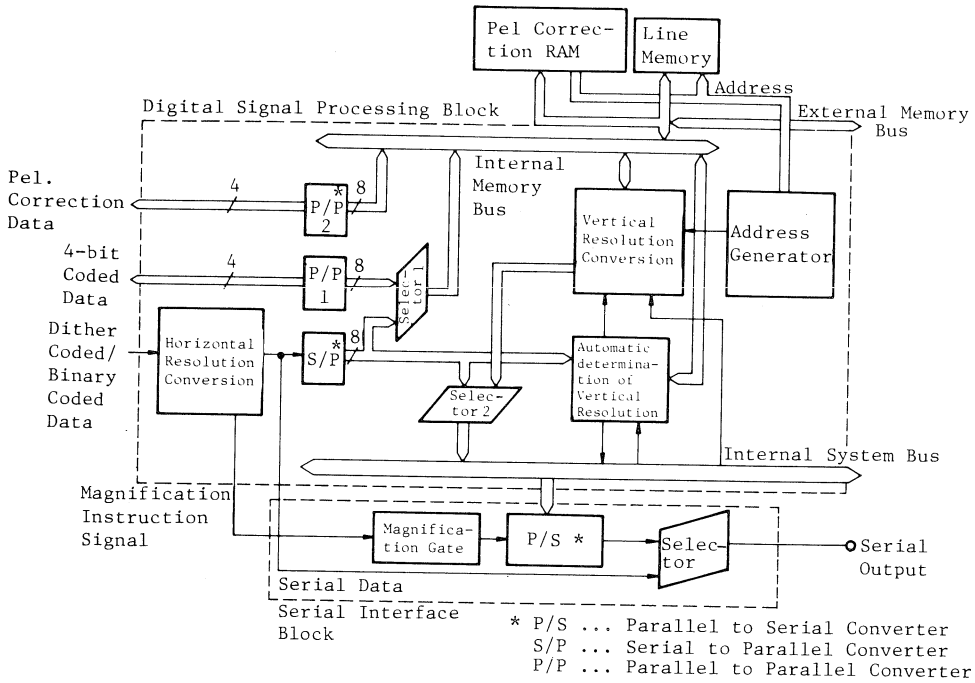
1. Correction of distortion included in the image data coming from the sensor, and

2. Digitization of the corrected data.



● Digital Signal Processing Block

The functions of this block are:



1. Horizontal resolution conversion of digitized image data,
2. Automatic judgement of vertical resolution, and
3. Vertical resolution conversion of digitized image data.

The DIPP can reduce and magnify digitized data using horizontal resolution conversion or vertical resolution conversion.

Reduction is performed only in read(T) mode. The DIPP reduces the digitized data and transfers it to the MPU system, which allows the time required for transmitting the data to be shortened.

Magnification is performed in receive(R) mode. The DIPP can magnify the reduced data which has been transmitted via the internal system bus and transfers it to the recorder.

■PIN FUNCTIONS

● Power Supply Pins

Power Supply Pins

Mnemonic	Input/Output	Pin Number
VDD	Power Supply	14, 33
VSS	Power Supply	16, 42
AVDD	Power Supply	50
AVSS	Power Supply	54
VBL	Power Supply	47
VCL	Power Supply	51
VT	Open	43

1) VDD, VSS

Power is supplied to all internal logic circuits using these two pins. VDD is power (+5V ± 5%) and AVSS is ground.

2) AVDD, AVSS

Power is supplied to all internal analog circuits using these two pins. AVDD is power (+5V ± 5%) and VSS is ground.

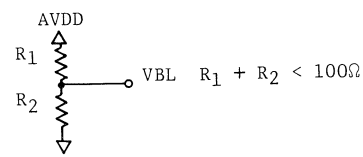
3) VBL, VCL

These pins are used to supply external voltage references for the DIPP ISIN1 and ISIN2 inputs.

VBL input is the voltage of the absolutely black level of the sensor output signals. Its recommended value is 3.5V. (The allowable range is $2.0V \leq VBL \leq AVDD$.)

VCL input is the voltage to which the sensor output signals are clamped in the sample and hold circuit. Although, strictly speaking, input voltage to VCL is VBL minus output voltage during sensor stopping, the DIPP uses VCL input voltage equal to VBL input voltage.

When the VBL voltage is generated by dividing resistance as shown below, the resistance must be 100Ω or less in order to generate stable VBL voltage which is free from the influence of noises and the like.



4) VT

No line should be connected to this pin.

● MPU Interface Pins

MPU Interface Pins

Pin Name	Mnemonic	Input/Output	Active State	Three State	Pin Number
Data Bus	D0-D7	input/output	High	yes	24 to 31
MPU Select	$\overline{68}$/80	input	(M) - Low (I) - High	no	34
Chip Select	$\overline{CS}$	input	Low	no	35
Register Select	$\overline{RS}$	input	Low	no	36
Data Strobe	DS	input	(M) - High (I) - Low	no	37
Read/Write	R/$\overline{W}$	input	(M) read-High write-Low (I) - Low	no	38
Reset	$\overline{RST}$	input	Low	no	1
Interrupt Request	INT	output	High	no	32
Read (T) Mode/ Receive (R) Mode Operation Start	$\overline{T}$/RSCAN	input	Read -- High Receive -- Low	no	40

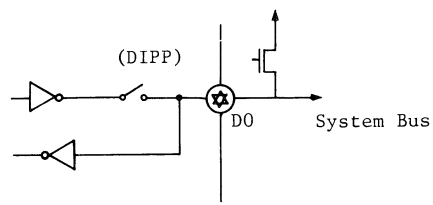
(M) ..... Motorola LSI Read ..... Read mode

(I) ..... Intel LSI Receive ... Receive mode

1) D0-D7 (input/output)

Data bus pins. These pins are connected to the system data bus to provide bidirectional data transfer between the MPU system and the DIPP. The outputs of these pins remain in high impedance state except when the MPU system reads data from the DIPP.

While the outputs are placed in high impedance state, voltage at these pins must be fixed to high or low level as shown below.



2) $\overline{68}$/80 (input)

MPU select pin. When the $\overline{68}$/80 input is low, a Motorola MPU can be interfaced with the DIPP. When the $\overline{68}$/80 input is high or open, an Intel MPU can be interfaced. This pin employs an internal pull-up resistor, which allows this pin to be left open. (This pin incorporates a pull-up resistor.)

3) $\overline{CS}$ (input)

Chip select pin. A low level on the $\overline{CS}$ input indicates that the MPU can access a DIPP internal register. When this input is high, the MPU cannot access any DIPP register regardless of the status of R/$\overline{W}$ or DS input. The $\overline{CS}$ input and the $\overline{T/RDACK}$ input must not be pulled low together.

4) $\overline{RS}$ (input)

Register select pin. This pin is used for selecting the register to be accessed by the MPU. When the $\overline{RS}$ input is low, the MPU can access the address register or the status register. When this input is high, the MPU can access the control registers.

The $\overline{RS}$ pin is usually interfaced using the least significant bit of the system address bus (A0).

5) DS (input)

Data strobe pin. The function of this pin depends on the status of the $\overline{68}$/80 input.

6) R/$\overline{W}$ (input)

Read/write pin. The function of this pin depends on the status of the $\overline{68}$/80 input.

7) $\overline{RST}$ (input)

Reset pin. When the $\overline{RST}$ input is driven low, the DIPP internal circuits are placed in the following states.

① All counters are cleared and halted.

② All registers except for internal RAMs are initialized. The contents of internal RAMs remain unchanged.

③ The current flowing through the analog comparators and the analog amplifiers is switched off.

Note that this $\overline{RST}$ pin differs from that of other peripherals in the following.

④ Even if the MPU system drives the $\overline{RST}$ input from low level to high level to release the DIPP from the reset state, the counters (described in ①) remain halted. In order to restart the counters, the MPU must write a 1 to the DIPPST bit of the R01 register.

8) INT (output)

Interrupt request pin. The DIPP drives the INT output high to send an interrupt request to the MPU if:

① the DIPP has finished writing to the internal shading wave RAM and to the external pel correction RAM *1, (WBSY bit in the status register has changed from 1 to 0

② the DIPP has finished reading a scan line of image data *2, (RBSY bit in the status register has changed from 1 to 0

The INT output is then negated low when the MPU reads the status register or the MPU drives the DIPP T/RSCAN input high.

The INT output is enabled only when INTE bit of the R01 register is 1.

9) T/RSCAN (input)

Read (T) mode or receive (R) mode operation start pin. T/RSCAN input causes the DIPP to begin read (T) mode or receive (R) mode operations. Functions of the T/RSCAN input are as sollows.

① If T/RSCAN input is asserted high in read (T) mode, the DIPP recognizes the next ϕTG cycle as a read cycle. This recognition allows assertion of the LNST signal and IWIN signal.
In addition, this input controls the RBSY flag and the INT signal.

② In receive (R) mode, T/RSCAN input begins a transfer of received data from the MPU system to the recorder (such as printers). On the negative edge of this input, the DIPP drives T/RDRQ output high to begin a DMA transfer of the received data from the MPU system to the DIPP. (See Fig. 4-5.)

● DMAC Interface Pins

DMAC Interface Pins

Pin Name	Mnemonic	Input/Output	Active State	Three State	Pin Number
DMA Request	T/RDRQ	output	High	no	21
DMA Acknowledge Input	T/RDACK	input	Low	no	39

1) T/RDRQ (output)

DMA request pin. By driving T/RDRQ output high, the DIPP can request the DMA controller (DMAC) to perform a DMA transfer of data.
The function of the T/RDRQ output depends on the status of $\overline{T}$/R bit in the R00 register and BST bit in the R01 register.

2) $\overline{T/RDACK}$

DMA acknowledge input pin. This input is a response to T/RDRQ output. When a Motorola MPU is used, the DIPP recognizes the status of R/$\overline{W}$ input reversely while the $\overline{T/RDACK}$ input is low.

● Clock Input Pins

Clock Pins

Pin Name	Mnemonic	Input/Output	Active State	Three State	Pin Number	When not used
Clock Input	CLKI	input	High	no	59	
Receive Mode Clock Input	RCLKI	input	High	no	22	*

* No lines should be connected to this pin.

1) CLKI (input)

Clock input pin. This CLKI input acts as a fundamental clock in read (T) mode. Input clock frequency should be in the range from 1MHz to 10MHz with a duty cycle of 50%.
All of the output signals except for system bus interface signals and memory bus interface signals are generated on the negative edge of the CLKI input.
In receive mode also, the above-mentioned clock should be input to this pin.

2) RCLKI (input)

Receive mode clock input pin. This RCLKI input acts as a fundamental clock in receive (R) mode. The DIPP extracts clocks required for a serial transfer to the recorder from the RCLKI inputs, and outputs the extracted clocks as RCLK via the T/RCLK pin. Input clock frequency should be in the range from 1MHz to 10MHz with a duty cycle of 50%.

● CCD Image Sensor Interface Pins

Table 4-5 CCD Image Sensor Interface Pins

Pin Name	Mnemonic	Input/ Output	Active State	Three State	Pin Number	When not used
Transfer Gate Pulse Output	ϕTG	output	High	no	60	
CCD Driving Clock Output	ϕ1	output	High	no	57	
Output Amplifier Reset Clock Outpur	ϕR	output	High	no	58	
Image Signal Input 1	ISIN1	input	High	no	53	
Image Signal Input 2	ISIN2	input	High	no	52	*
Image Signal Output	IOUT	output	High	no	55	*

* No lines should be connected to this pin.

1) ϕTG (output)

Transfer gate pulse output pin. When the ϕTG output is high, the transfer gate of the CCD image sensor is open. The ϕTG output remains high for the period:

$$T1 = 40/(\text{sensor drive frequency}) \text{ sec}$$

Additionally, if ϕTGIN bit in R19 register is 1, the high level pulse width of ϕTG input (T1) can be changed via the TRIG pin.(See Fig. 4-6) The ϕTG cycle time (T2) depends on the DIPP internal timer. The range of T2 is:

$$T2 \leq 8192/(\text{sensor drive frequency}) \text{ sec}$$

If TGIN bit is 0, T2 can be extended via the TRIG pin. (See Fig. 4-6)

2) ϕ1 (output)

CCD driving clock output pin. This pin outputs the clock which drives the CCD image sensor. This clock behaves as follows while ϕTG output is high.

3) ϕR (output)

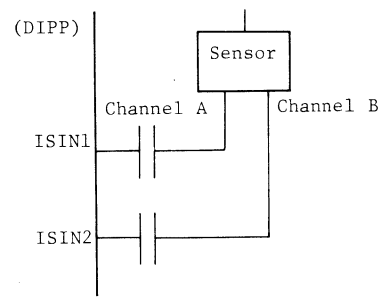
Sensor output reset clock output pin. This pin outputs the clock which resets the output of the CCD image sensor.

4) ISIN1 (input)

Image signal input pin 1. This pin acts as input of the CCD image sensor analog output signal. A capacitor across the external ISIN1 line must be used to level-shift the input black level signal to the VBL voltage. (See Fig. 4-7). When using a CCD image sensor with a single output channel, use this pin as input of the sensor output signal.

5) ISIN2 (input)

Image signal input pin 2. The CCD image sensor analog output signals are input to both the ISIN1 and ISIN2 pins when the DIPP uses two sensor output channels. (See Fig. 4-7) This pin can be used by writing the corresponding parameters to the SMD0 to SMD2 bits in the R09 register.



Connection between Sensor and Image Signal Input Pins

6) IOUT (output)

Image signal output pin. This pin outputs the analog signal which is obtained by smoothing ISIN1 or ISIN2 inputs in the sample and hold circuit. This output can be used by writing the corresponding parameters to the SMD0 to SMD2 bits in the R09 register.

● A/D Conversion Pins

A/D Conversion Pins

Pin Name	Mnemonic	Input/ Output	Active State	Three State	Pin Number	When not used
Peak Value Output	PEAKO	output	High	no	49	
Peak Value Input	PEAKI	input	High	no	48	*
Shading Waveform Output	DAO	output	High	no	46	
Slice Level Reference Input for Edge Emphasis 1	SLICE1	input	High	no	45	*
Slice Level Reference Input for Edge Emphasis 2	SLICE2	input	High	no	44	*

* No lines should be connected to this pin.

1) PEAKO (output)

Peak value output pin. This pin outputs the peak value of image signal referenced to VBL. The output impedance of this pin depends on the status of APEAKE bit in the R0A register.

2) PEAKI (input)

Peak value input pin. This pin is used to input the peak value of image signal which will be input to the 7-bit A/D and D/A converters. Writing 1 to APEAKE bit allows input to the PEAKI pin. In this case, the PEAKI input signal enters an internal unity gain amplifier. Thus, the input impedance of the PEAKI pin is several MΩ.
Writing 0 to APEAKE bit places the PEAKI input in a high impedance state.

3) DAO (output)

Shading waveform output pin. This pin outputs a shading waveform regenerated by the 7-bit D/A converter. This pin provides an internal unity gain amplifier, which allows for a very low output impedance.

4) SLICE1 (input)

Slice level reference input pin for edge emphasis 1. When the DIPP performs edge emphasis during binary coding of read data (in response to the contents of DMODE0 and DMODE1 bits in the R00 register), this pin is used to provide the reference voltage for slice levels which are input

to the 4-bit A/D converter in DIPP. Which slice level is used for binary coding is determined by ROB and ROC registers. The input signal via this pin enters an internal unity gain amplifier.

When not used, the SLICE1 input is placed in a high impedance state.

5) SLICE2 (input)

Slice level reference input pin for edge emphasis 2. When the DIPP performs an edge emphasis during dither coding or 4-bit coding of read data (in response to the contents of DMODE0 and DMODE1 bits in the R00 register), this pin is used to provide the reference voltage for slice levels which are input to the 4-bit A/D converter. With SLICE2, which slice level is used for dither coding or 4-bit coding is determined by the contents of dither RAM, VH0 to VH3 bits in the R0B register and the R0C register. The SLICE2 input signal enters an internal unity gain amplifier and the input impedance of this pin is almost equal to that of the SLICE1 pin.

● Internal Timer Pins

Internal Timer Pins

Pin Name	Mnemonic	Input/Output	Active State	Three State	Pin Number
Timer Trigger Input	TRIG	input	High	no	56
Timer Output	TIMO	output	High	no	23
Transfer Mask Gate	TMSK	output	High	no	18
INST/IWIN Output	LNST/IWIN	output	High	no	41

1) TRIG (input)

Timer trigger input pin. ϕTRIG input is used to extend the duration of the internal timer counting or to drive the internal timer synchronously with an external timer.

2) TIMO (output)

Timer output pin. This pin outputs the counting value of the internal timer. This output can be selected from 2^6, 2^7 and 2^8 bits of the internal timer using TM0 and TM1 bits in the R04 register. Additionally the user can monitor the $(m+1)/\overline{m}$ signal output from the

horizontal resolution conversion circuit by writing 1s to both TM0 and TM1 bits.

3) TMSK (output)

Transfer mask gate pin. This pin is used to advise the MPU of the DIPP internal state.
One of the $\overline{T}/R$, SENS, and IWIN internal signals is output depending on the contents of TS0 and TS1 bits in the R04 register.

4) LNST/IWIN (output)

LNST/IWIN output pin. This pin is used to advise the MPU of the DIPP internal state. The output of this pin depends on the $\overline{LN}/IW$ bit in the R03 register.

● Serial Interface Pins

Serial Interface Pins

Pin Name	Mnemonic	Input/Output	Active State	Three State	Pin Number	When not used
Serial Data Output	T/RDATA	output	High	no	20	*
Serial Clock Output	T/RCLK	output	High	no	19	*

* No lines should be connected to this pin.

1) T/RDATA (output)

Serial data output pin. This pin outputs data which is serially transferred to the recorder (e.g. printers). T/RDATA data output depends on the $\overline{T}/R$ bit in the R00 register.

2) T/RCLK (output)

Serial clock output pin. This pin outputs a clock signal used to latch serial data output from the T/RDATA pin. However, this clock signal is output only when the SCE bit in the R01 register is 1.
The function of this clock signal depends on the $\overline{T}/R$ bit in the R00 register.

● Memory Bus Interface Pins

Memory Bus Interface Pins

Pine Name	Mnemonic	Input/Output	Active State	Three State	Pin Number	When not used
Memory Address/ Data Bus	MAD0 to MAD7	input/output	High	yes	17,15,13 12,11,10 9, 8	*
Memory Address Strobe and Memory Data Strobe Output	MAS/MDS	output	High	no	7	*
Line Memory Write Enable	$\overline{\text{LWR}}$	output	Low	no	6	*
Line Memory Read Enable	$\overline{\text{LRD}}$	output	Low	no	5	*
Scan Line Select	LNSL	output	-	no	2	*
Pel Correction RAM Write Enable	$\overline{\text{PWR}}$	output	Low	no	4	*
Pel Correction RAM Read Enable	$\overline{\text{PRD}}$	output	Low	no	3	*
Memory Address 8/4-bit Coded Data Write Enable	MA8/ $\overline{\text{MIWR}}$	output	MA8-High $\overline{\text{MIWR}}$-Low	no	64	*
Memory Address 9/Line Start Notification	MA9/ LNSTN	output	High	no	63	*
Memory Address 10/Pel Correction Data Read	MA10/ $\overline{\text{MPRD}}$	output	MA10-High $\overline{\text{MPRD}}$-Low	no	62	*
Memory Address 11/Pel Data Enable/Memory Bus Enable	MA11/ $\overline{\text{PDEN}}$/ MBE	output	MA11-High $\overline{\text{PDEN}}$-Low MBE-High	no	61	*

* No lines should be connected to this pin.

1) MAD0 to MAD7 (I/O)

Memory address/data bus pins. These pins are interfaced with the 8-bit memory bus to provide bidirectional communication between the DIPP and the external RAM (pel correction RAM or line memory).

2) MAS/MDS (output)

Memory address strobe and memory data strobe output pin. The negative edge of MAS/MDS is used to latch the address or data which is output from MAD0 through MAD7 pins.

3) $\overline{LWR}$ (output)

Line memory write enable pin. The positive edge of $\overline{LWR}$ output is used to enable writing of data into the line memory. The data to write is either horizontal-resolution-converted data or 4-bit coded data. During a burst DMA transfer of data, this output remains high.

4) $\overline{LRD}$ (output)

Line memory read enable pin. When the $\overline{LRD}$ output is low, either the horizontal-resolution-converted data or 4-bit coded data can be read from the line memory.
During a burst DMA transfer of data, this output remains low.

5) LNSL (output)

Scan line select pin. The LNSL output is a control signal which selects the address area of the line memory to read or write horizontal-resolution-converted data or 4-bit coded data.

6) $\overline{PWR}$ (output)

Pel correction RAM write enable pin. A positive edge of the $\overline{PWR}$ output enables the pel correction data to be written to the pel correction RAM. The PWR output is low only during the pel correction data detection cycle (that is, when the internal PELWR signal is high) in B, C or D mode. (See Fig. 1-14 and Fig. 6-6.). In other cases, this output remains high.

7) $\overline{PRD}$ (output)

Pel Correction RAM read enable pin. A positive edge of the $\overline{PRD}$ output enables pel correction data to be read from the pel correction RAM. PRD output is low only when the internal PELWR signal is low in B, C or D mode. In other cases, this output remains high.

8) MA8/$\overline{MIWR}$ (output)

Memory address 8/4-bit coded data write enable pin. The function of this output depends on the memory bus interface mode selected by MMODE0 and MMODE1 bits in the R00 register.

9) MA9/LNSTN (output)

Memory address 9/Line Start Notification pin.
The function of this pin depends on the memory bus interface mode selected by MMODE0 and MMODE1 bits.

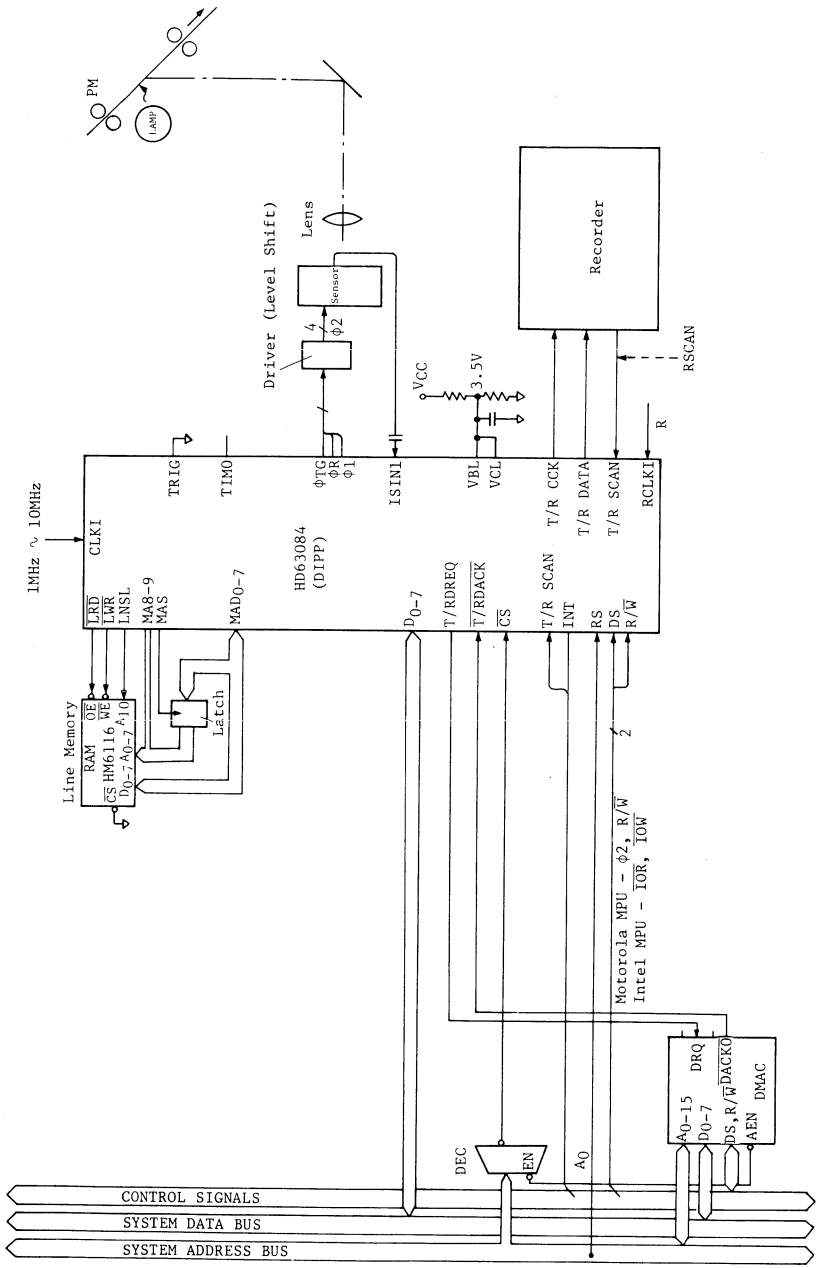
10) MA10/$\overline{\text{MPRD}}$ (output)

Memory address 10/Pel correction data read pin.
The function of this pin depends on the memory bus interface mode selected by MMODE0 and MMODE1 bits.

11) MA11/$\overline{\text{PDEN}}$/MBE

Memory address 11/pel data enable/memory bus enable pin.
The function of this pin depends on the memory bus interface mode selected by MMODE0 and MMODE1 pins.

■SYSTEM BUS INTERFACE



Operations of the system bus interface, memory bus interface, sensor interface and serial interface are described in the following paragraphs.

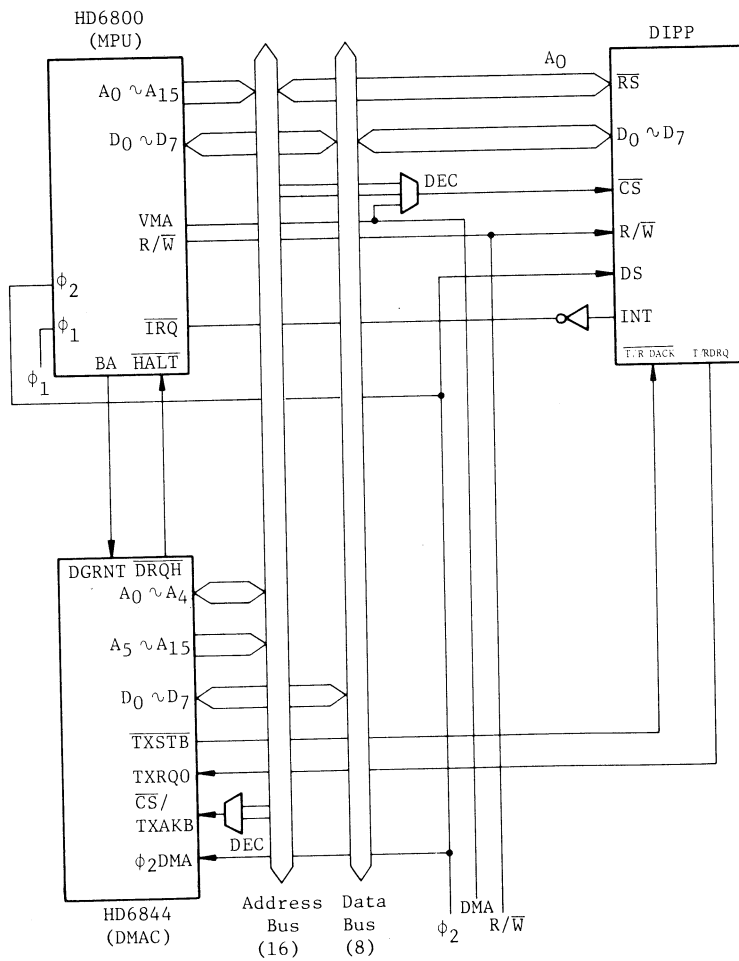
■SYSTEM BUS INTERFACE OPERATION

The DIPP can be interfaced to either a Motorola MPU or an Intel MPU. The following paragraphs explain interface operation through the system bus (including the document image bus).

- Interface with Motorola MPU

A Motorola MPU can be interfaced to the DIPP as shown as follows. Note that the $\overline{68}/80$ input pin must be low and that the $\phi 2$ clock signal and R/$\overline{W}$ signal must be input to the DS pin and the R/$\overline{W}$ pin respectively.

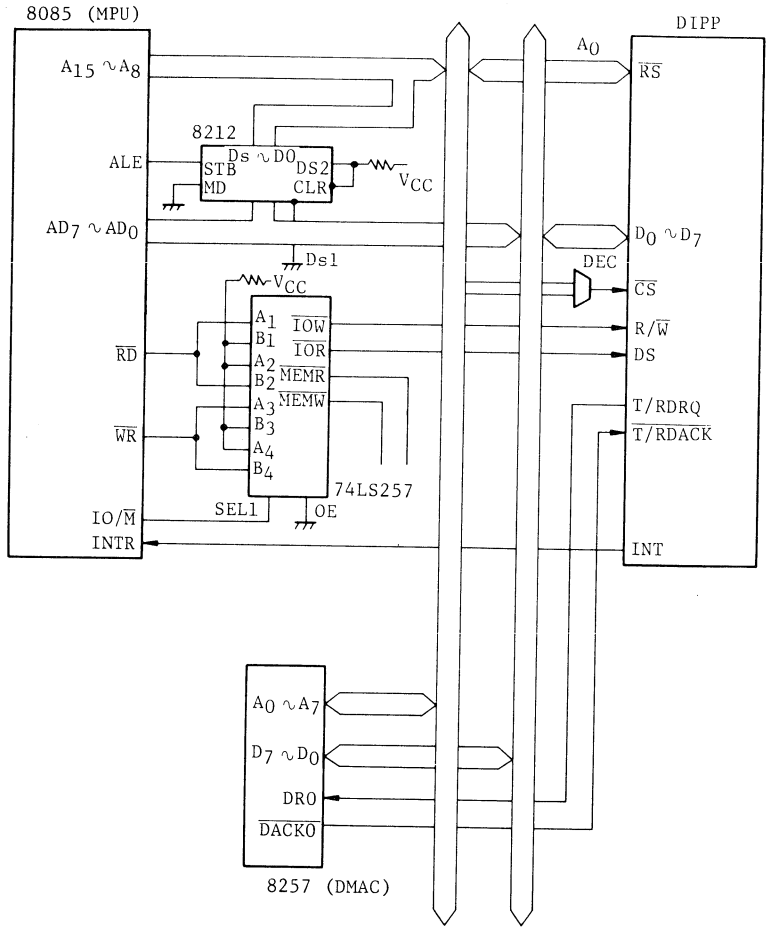
The DIPP can perform a DMA transfer through the system bus by using the DMA controller (DMAC) or the DICEP (The DICEP can be used as a DMA controller). While the $\overline{T}/\overline{RDACK}$ input signal is low during DMA operation, the DIPP recognizes the state of the R/$\overline{W}$ signal inversely.



Interface with Motorola MPU

- Interface with Intel MPU

An Intel MPU can be interfaced to the DIPP as shown as follows. Note that the $\overline{68}/80$ input pin must be high.



Interface with Intel MPU

■ABSOLUTE MAXIMUM RATING

● Internal Digital Circuits

(Voltages referenced to V_{SS} = 0V. Ta = 25°C)

No.	Item	Symbol	Value	Unit
1	Supply Voltage	V_{DD}	-0.3 to +7.0	V
2	Input Voltage (Digital Input Pins)	V_I	-0.3 to V_{DD}+0.3	V
3	Input Voltage (Digital I/O Pins)	V_{IT}	-0.3 to V_{DD}+0.3	V

● Internal Analog Circuits

(Voltages referenced to AVss = 0V. Ta = 25°C)

No.	Item	Symbol	Value	Unit
1	Supply Voltage	AV_{DD}	-0.3 to +7.0	V
2	Reference Voltage	$V_{2.5}$ V_{CL} V_{BL}	-0.3 to V_{DD}+0.3	V
3	Input Voltage (Analog Input Pins)	V_{IA}	-0.3 to V_{DD}+0.3	V

● Common Characteristics between Digital and Analog Circuits

No.	Item	Symbol	Value	Unit
1	Operating Temperature	Topr	0 to +70	°C
2	Storage temperature	Tstg	-55 to +125	°C
3	Power Consumption *1	Pc	500	mW

*1) Ta = 25°C

■ELECTRICAL CHARACTERISTICS

●Internal Digital Circuits

DC Characteristics

(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C)

No.	Item	Symbol	Test Condition	min	typ	max	Unit
1	Input High Voltage	V_{IH}	V_{DD}=5.25V	2.0	-	V_{DD} +0.3	V
2	Input Low Voltage	V_{IL}	V_{DD}=4.75V	-0.3	-	0.8	V
3	Output High Voltage	V_{OH}	V_{DD}=4.75V I_{OH}=-400μA V_{IH}=2.0V V_{IL}=0.8V	3.0	-	-	V
4	Output Low Voltage	V_{OL}	V_{DD}=4.75V V_{IH}2.0V V_{IL}=0.8V Other output pins : Low I_{OL}=1.6mA	-	-	0.4	V
5	Input Leakage Voltage	I_{IN}	V_{DD}=5.25V V_I =0 to V_{DD}	-10 *1	-	10	μA
6	Three-State (Off State) Leakage Current	I_{OZH}	V_{DD}=5.25V V_O =V_{DD}	-10	-	10	μA
		I_{OZL}	V_{DD}=5.25V V_O =V_{SS}	-10	-	10	μA

*1) The minimum leakage current at pin 34 ($\overline{68}$/80) is -100μA because it has an internal pull-up resistor.

● AC Characteristics

(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C)

(1) Motorola MPU Interface Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
DS Pulse Width	t_{WDS6}	I	**Fig. 1**	DS	450	—	—	ns
DS to R/$\overline{W}$ Setup Time	t_{SRW6}	I	**Fig. 1**	R/$\overline{W}$	140	—	—	ns
DS to R/$\overline{W}$ Hold Time	t_{HRW6}	I	**Fig. 1**	R/$\overline{W}$	10	—	—	ns
DS to $\overline{CS}$ Setup Time	t_{SCS6}	I	**Fig. 1**	$\overline{CS}$	140	—	—	ns
DS to $\overline{CS}$ Hold Time	t_{HCS6}	I	**Fig. 1**	$\overline{CS}$	10	—	—	ns
DS to $\overline{RS}$ Setup Time	t_{SRS6}	I	**Fig. 1**	$\overline{RS}$	140	—	—	ns
DS to $\overline{RS}$ Hold Time	t_{HRS6}	I	**Fig. 1**	$\overline{RS}$	50	—	—	ns
Read Data Access Time	t_{RAC6}	O	**Fig. 1**	D0 to D7	—	—	320	ns
Read Data Hold Time	t_{RH6}	O	**Fig. 1**	D0 to D7	10	—	—	ns
Write Data Setup Time	t_{WS6}	I	**Fig. 1**	D0 to D7	200	—	—	ns
Write Data Hold Time	t_{WH6}	I	**Fig. 1**	D0 to D7	40	—	—	ns
DS to $\overline{T/RDACK}$ Setup Time	t_{SDK6}	I	**Fig. 2**	$\overline{T/RDACK}$	(140)	—	—	ns
DS to $\overline{T/RDACK}$ Hold Time	t_{HDK6}	I	**Fig. 2**	$\overline{T/RDACK}$	(10)	—	—	ns

(2) Intel MPU Interface Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
DS ($\overline{RD}$) Pulse Width	t_{WDS8}	I	**Fig. 3**	DS	300	—	—	ns
R/$\overline{W}$ ($\overline{WR}$) Pulse Width	t_{WRW8}	I	**Fig. 3**	R/$\overline{W}$	250	—	—	ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{SRC8}	I	**Fig. 3**	$\overline{CS}$	125	—	—	ns
$\overline{RD}$ to $\overline{CS}$ Hold Time	t_{HRC8}	I	**Fig. 3**	$\overline{CS}$	0	—	—	ns
$\overline{WR}$ to $\overline{CS}$ Setup Time	t_{SWC8}	I	**Fig. 3**	$\overline{CS}$	125	—	—	ns

(to be continued)

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
$\overline{WR}$ to $\overline{CS}$ Hold Time	t_{HWC8}	I	Fig. 3	$\overline{CS}$	20	–	–	ns
$\overline{RD}$ to $\overline{RS}$ Setup Time	t_{SRR8}	I	Fig. 3	$\overline{RS}$	125	–	–	ns
$\overline{RD}$ to $\overline{RS}$ Hold Time	t_{HRR8}	I	Fig. 3	$\overline{RS}$	50	–	–	ns
$\overline{WR}$ to $\overline{RS}$ Setup Time	t_{SWR8}	I	Fig. 3	$\overline{RS}$	125	–	–	ns
$\overline{WR}$ to $\overline{RS}$ Hold Time	t_{HWR8}	I	Fig. 3	$\overline{RS}$	70	–	–	ns
Read Data Access Time	t_{RAC8}	O	Fig. 3	D0 to D7	–	–	300	ns
Read Data Hold Time	t_{RH8}	O	Fig. 3	D0 to D7	10	–	–	ns
Write Data Setup Time	t_{WS8}	I	Fig. 3	D0 to D7	180	–	–	ns
Write Data Hold Time	t_{WH8}	I	Fig. 3	D0 to D7	50	–	–	ns
$\overline{RD}$ to $\overline{T/RDACK}$ Setup Time	t_{SDK8}	I	Fig. 4	$\overline{T/RDACK}$	(125)	–	–	ns
$\overline{RD}$ to $\overline{T/RDACK}$ Hold Time	t_{HDK6}	I	Fig. 4	$\overline{T/RDACK}$	(0)	–	–	ns
$\overline{WR}$ to $\overline{T/RDACK}$ Setup Time	t_{SRK8}	I	Fig. 4	$\overline{T/RDACK}$	(125)	–	–	ns
$\overline{WR}$ to $\overline{T/RDACK}$ Hold Time	t_{HRK8}	I	Fig. 4	$\overline{T/RDACK}$	(25)	–	–	ns

(3) MPU Interface Timing (common to Motorola MPU and Intel MPU)

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
T/RDRQ Positive Edge Delay	t_{DRQH}	O	Fig. 5	T/RDRQ	–	–	200	ns
T/RDRQ Negative Edge Delay	t_{DRQL}	O	Fig. 5	T/RDRQ	–	–	200	ns
INT Positive Edge Delay	t_{INTH}	O	Fig. 6	INT	–	–	300	ns
T/RSCAN input to INT Negative Edge Delay	t_{INTL}	O	Fig. 6	INT	–	–	100	ns
DS input to INT Negative Edge Delay	t_{DSIL}	O	Fig. 1 Fig. 3	INT	–	–	(300)	ns

(4) Clock and Control Input Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
CLKI Cycle Time	t_{CYC}	I	**Fig. 7**	CLKI *2	100	—	1000	ns
RCLK Cycle Time	t_{RCYC}	I	**Fig. 7**	RCLKI *2	200	—	10^6	ns
TSCAN Pulse Width	t_{TSW}	I	**Fig. 7**	T/RSCAN	$(2 \times t_{CYC})$	—	—	ns
RSCAN Pulse Width	t_{RSW}	I	**Fig. 7**	T/RSCAN	$(2 \times t_{RCYC})$	—	—	ns
$\overline{RST}$ Pulse Width	t_{RSTW}	I	**Fig. 7**	$\overline{RST}$	$(2 \times t_{CYC})$	—	—	ns
TRIG Pulse Width	t_{TRIG}	I	**Fig. 7**	TRIG	(8)	—	—	μs

*2) Both CLKI and RCLKI input frequencies provide duty cycle of 50%.

(5) Serial Output Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
CLKI Input to TMSK Output Delay	t_{TMDT}	O	**Fig. 8**	TMSK	—	—	200	ns
CLKI Input to TMSK Output Hold	t_{TMHT}	O	**Fig. 8**	TMSK	—	—	200	ns
TDATA Output Delay	t_{TDD}	O	**Fig. 8**	T/RDATA	—	—	200	ns
TDATA Output Hold	t_{TDH}	O	**Fig. 8**	T/RDATA	—	—	250	ns
TCLK Positive Edge Delay	t_{TCH}	O	**Fig. 8**	T/RCLK	—	—	200	ns
TCLK Negative Edge Delay	t_{TCL}	O	**Fig. 8**	T/RCLK	—	—	200	ns
RCLK Output to TMSK Output Delay	t_{TMDR}	O	**Fig. 9**	TMSK	—	—	(200) *3	ns
RCLK Output to TMSK Output Delay	t_{TMHR}	O	**Fig. 9**	TMSK	—	—	(200) *3	ns
RDATA Output Delay	t_{RDD}	O	**Fig. 9**	T/RDATA	—	—	(200) *3	ns
RDATA Output Hold	t_{RDH}	O	**Fig. 9**	T/RDATA	—	—	(200) *3	ns
RCLK Positive Edge Delay	t_{RCH}	O	**Fig. 9**	T/RCLK	—	—	(200) *3	ns
RCLK Negative Edge Delay	t_{RCL}	O	**Fig. 9**	T/RCLK	—	—	(200) *3	ns

*3) Values for reference.

(6) Application Output and Sensor Interface Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
TIMO Output Delay	t_{TO}	O	**Fig. 10**	TIMO	—	—	200	ns
LNST/IWIN Output Delay	t_{LN}	O	**Fig. 10 (IWIN)**	LNST/IWIN	—	—	250	ns
ϕTG Output Positive Edge Delay	$t_{\phi TD}$	O	**Fig. 11,12**	ϕTG	—	—	150	ns
ϕTG Output Negative Edge Delay	$t_{\phi TH}$	O	**Fig. 11,12**	ϕTG	—	—	160	ns
ϕ1 Output Delay	$t_{\phi 1D}$	O	**Fig. 11,12**	ϕ1	—	—	100	ns
ϕ1 Output Hold	$t_{\phi 1H}$	O	**Fig. 11,12**	ϕ1	—	—	130	ns
ϕR Positive Edge Delay	$t_{\phi RD}$	O	**Fig. 13**	ϕR	—	—	100	ns
ϕR Positive Edge Hold	$t_{\phi RH}$	O	**Fig. 13**	ϕR	—	—	100	ns

(7) Memory Bus Interface Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	type	max	Unit
MAS/MDS Positive Edge Delay	t_{MASD}	O	**Fig. 14, 16, 18, 19, 20**	MAS/MDS	—	—	200	ns
MAS/MDS Negative Edge Delay	t_{MASH}	O	**Fig. 14, 16, 18, 19, 20**	MAS/MDS	—	—	200	ns
LNSL Output Delay	t_{LSD}	O	**Fig. 14 Fig. 19**	LNSL	—	—	200	ns
MA8 to 11 Output Delay *4	t_{MAUD}	O	**Fig. 14 Fig. 19**	MA8/$\overline{\text{MIWR}}$ to MA11/ $\overline{\text{PDEN}}$/MBE	—	—	200	ns
$\overline{\text{LRD}}$ Negative Edge Delay	t_{LRD}	O	**Fig. 14 Fig. 19**	$\overline{\text{LRD}}$	—	—	200	ns
$\overline{\text{LRD}}$ Positive Edge Hold	t_{LRH}	O	**Fig. 14 Fig. 19**	$\overline{\text{LRD}}$	—	—	200	ns
$\overline{\text{LWR}}$ Negative Edge Delay	t_{LWD}	O	**Fig. 14 Fig. 19**	$\overline{\text{LWR}}$	—	—	200	ns

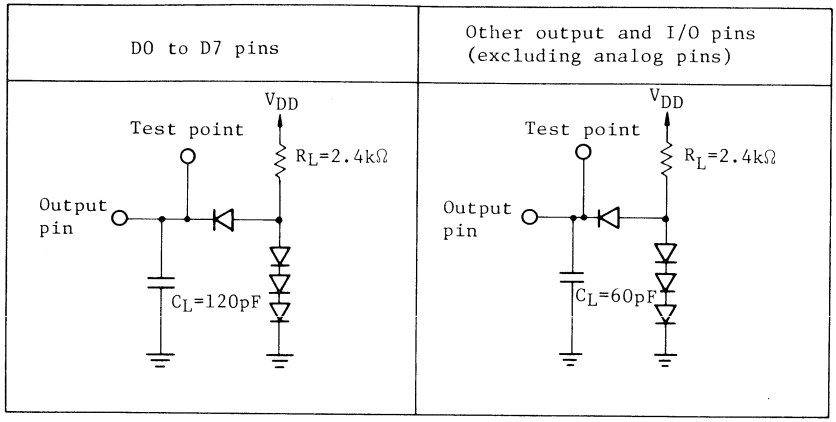
(To be continued)

*4) Values for reference.

(Continued)

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
$\overline{LWR}$ Positive Edge Hold	t_{LWH}	O	Fig. 14 Fig. 19	$\overline{LWR}$	—	—	200	ns
MAD0 to 7 Delay	t_{MADD}	O	Fig. 14 etc.	MAD0-7	—	—	200	ns
MAD0 to 7 Hold	t_{MADH}	O	Fig. 14 etc.	MAD0-7	—	—	200	ns
MAD0 to 7 Setup Time	t_{RDS}	I	Fig. 14	MAD0-8	50	—	—	ns
MAD0 to 7 Hold Time	t_{RDH}	I	Fig. 14	MAD0-7	50	—	—	ns
MBE Negative Edge Delay	t_{MBEL}	O	Fig. 15	MBE	—	—	200	ns
$\overline{T/RDACK}$ Input to MAS Negative Edge Delay	t_{BASL}	O	Fig. 17	MAS/MDS	—	—	200	ns
$\overline{T/RDACK}$ Input to MAS Positive Edge Delay	t_{BASH}	O	Fig. 17	MAS/MDS	—	—	200	ns
$\overline{T/RDACK}$ Input to T/RDRQ Negative Edge Delay	t_{BTDR}	O	Fig. 17	T/RDRQ	—	—	400	ns
MLNST Positive Edge Delay	t_{MLNH}	O	Fig. 16 Fig. 17 Fig. 18	MA9/LNSTN	—	—	250	ns
MLNST Negative Edge Delay	t_{MLNL}	O	Fig. 16 Fig. 17 Fig. 18	MA9/LNSTN	—	—	300	ns
$\overline{PRD}$ Negative Edge Delay	t_{PRD}	O	Fig. 16 Fig. 19	$\overline{PRD}$	—	—	200	ns
$\overline{PRD}$ Positive Edge Hold	t_{PRH}	O	Fig. 16 Fig. 19	$\overline{PRD}$	—	—	200	ns
$\overline{PWR}$ Negative Edge Delay	t_{PWD}	O	Fig. 18 Fig. 20	$\overline{PWR}$	—	—	200	ns
$\overline{PWR}$ Positive Edge Hold	t_{PWH}	O	Fig. 18 Fig. 20	$\overline{PWR}$	—	—	200	ns
$\overline{MIWR}$ Negative Edge Delay	t_{MIWL}	O	Fig. 16	MA8/$\overline{MIWR}$	—	—	400	ns
$\overline{MIWR}$ Positive Edge Delay	t_{MIWH}	O	Fig. 16	MA8/$\overline{MIWR}$	—	—	200	ns
$\overline{MPRD}$ Negative Edge Delay	t_{MPRL}	O	Fig. 18	MA10/$\overline{MPRD}$	—	—	250	ns
$\overline{MPRD}$ Positive Edge Delay	t_{MPRH}	O	Fig. 18	MA10/$\overline{MPRD}$	—	—	250	ns
$\overline{PDEN}$ Negative Edge Delay	t_{PDEL}	O	Fig. 18	MA11/$\overline{PDEN}$ /MBE	—	—	200	ns

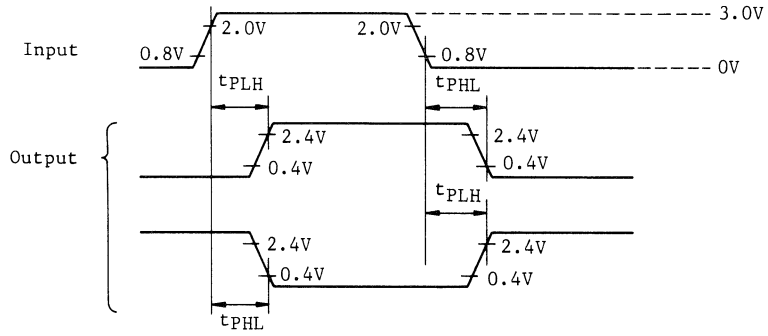
(Note 1) Bus Timing Test Loads



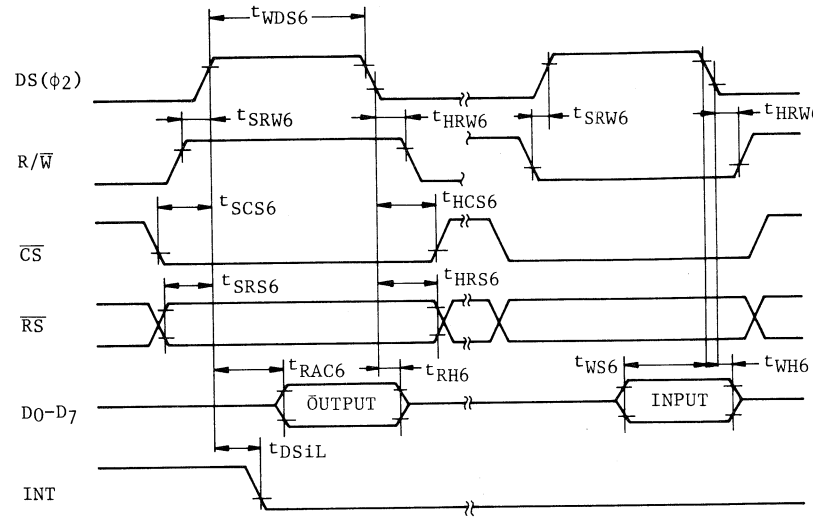
[Notes] 1. C_L includes stray capacitance caused by the probe and load capacitance.

2. Diodes are 1S2074 Ⓗ or equivalents.

(Note 2) I/O Signal Test Points

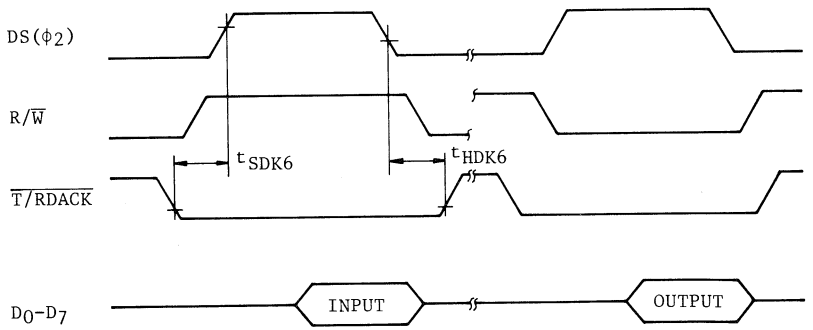


■TEST POINTS



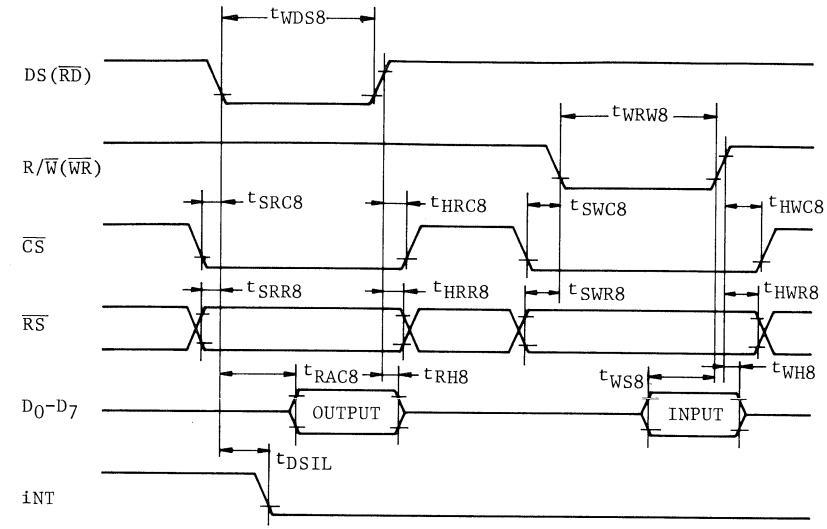
Note) $\overline{T/RDACK}$ input must be fixed high.

Fig. 1 Motorola MPU Access Timing



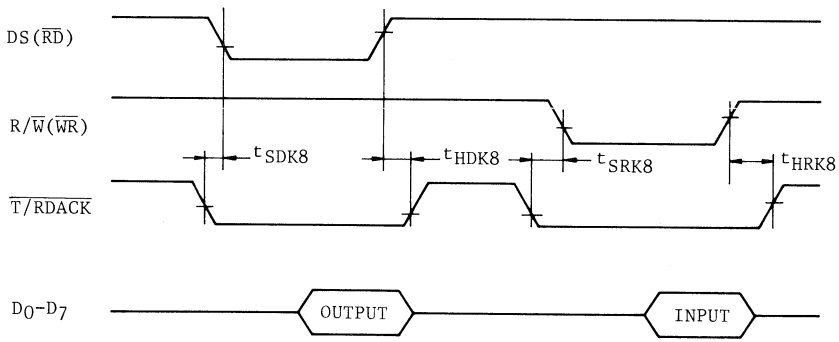
Note) $\overline{CS}$ input must be fixed high.

Fig. 2 DMA Operation Timing (Using Motorola MPU)



Note) T/RDACK input must be fixed high.

Fig. 3 Intel MPU Access Timing



Note) CS input must be fixed high.

Fig. 4 DMA Operation Timing (Using Intel MPU)

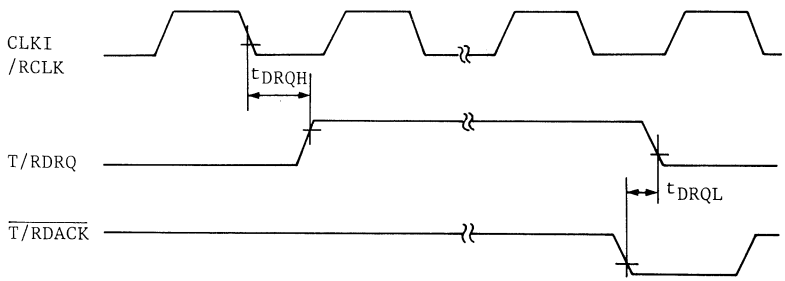


Fig. 5 T/RDRQ Output Timing

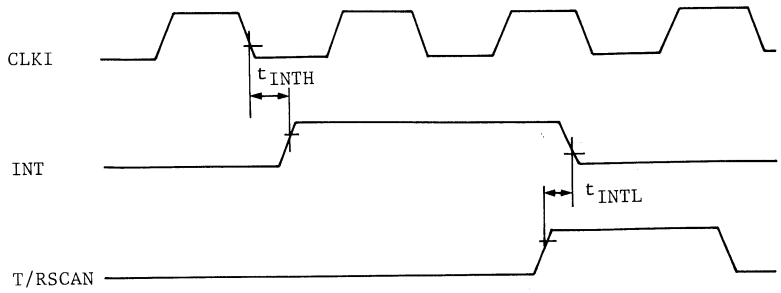


Fig. 6 INT Output Timing

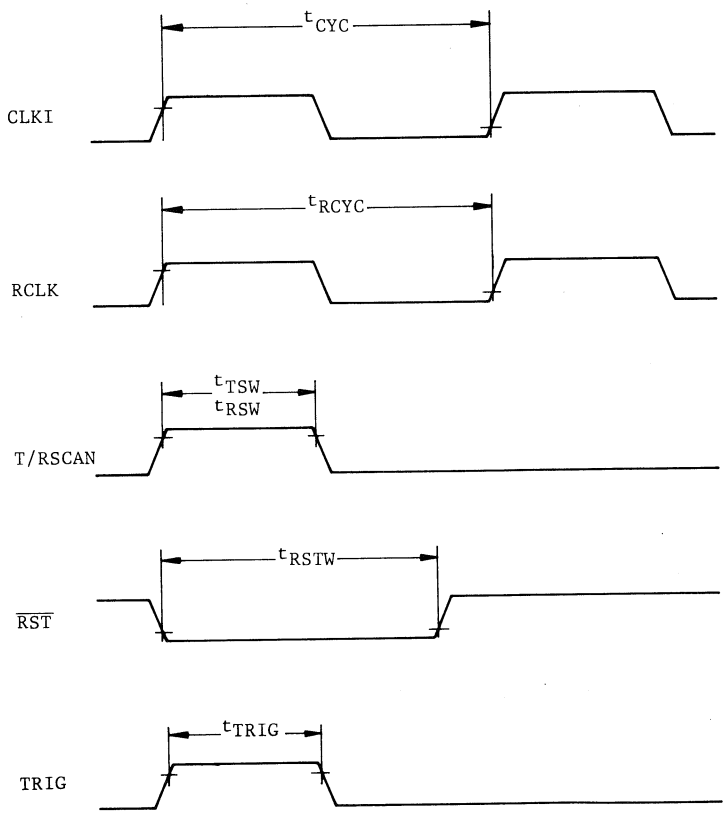


Fig. 7 CLKI, RCLK, T/RSCAN, $\overline{RST}$ and TRIG Input Timing

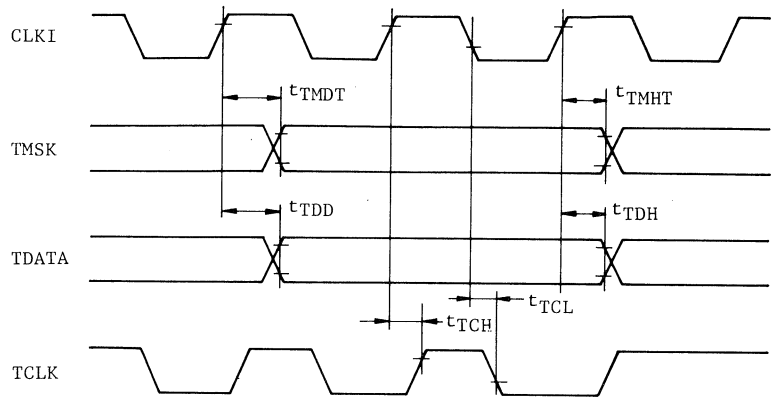


Fig. 8 Serial Output Timing (in Read (T) Mode)

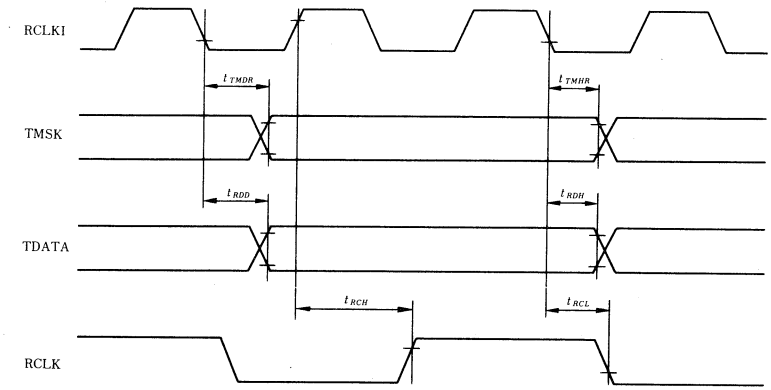


Fig. 9 Serial Output Timing (in Receive (R) Mode)

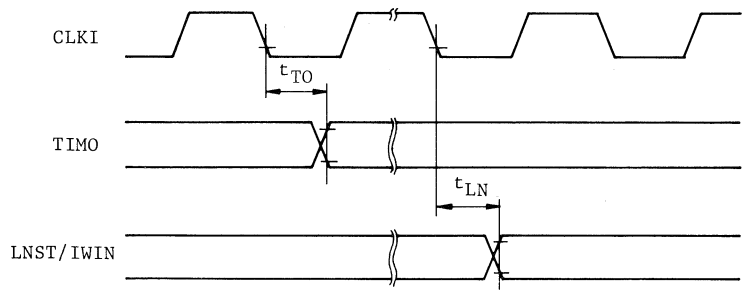
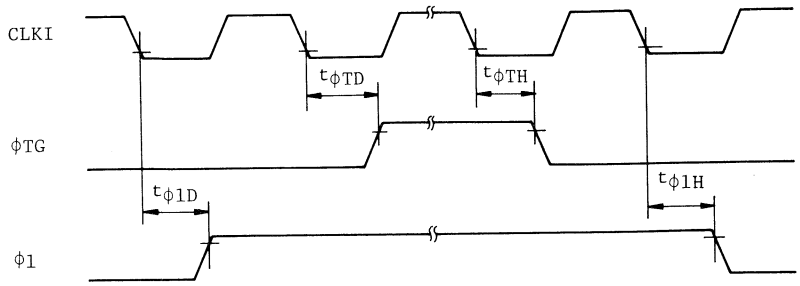
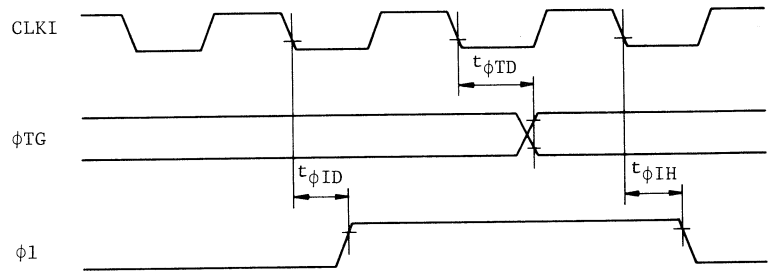


Fig. 10 Application Output Timing



Note) The SMD0, SMD1 and SMD2 bits in the R09 register must be 0,0 and 0 or 0,0 and 1 respectively.

Fig. 11 ϕ_{TG} and ϕ_1 Output Timing (1)



Note) The SMD0, SMD1 and SMD2 bits must be 0,1 and 0 or 0,1 and 1 respectively.

Fig. 12 ϕTG and ϕ1 Output Timing (2)

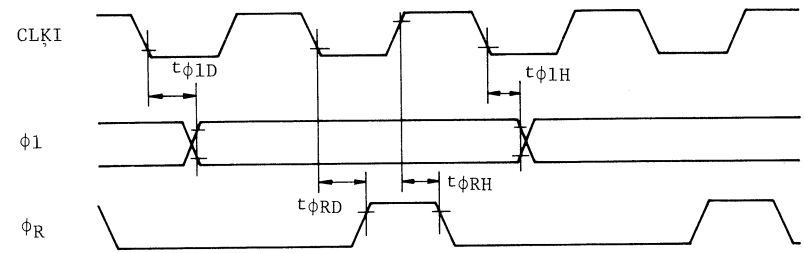


Fig. 13 ϕ1 and ϕ_R Output Timing

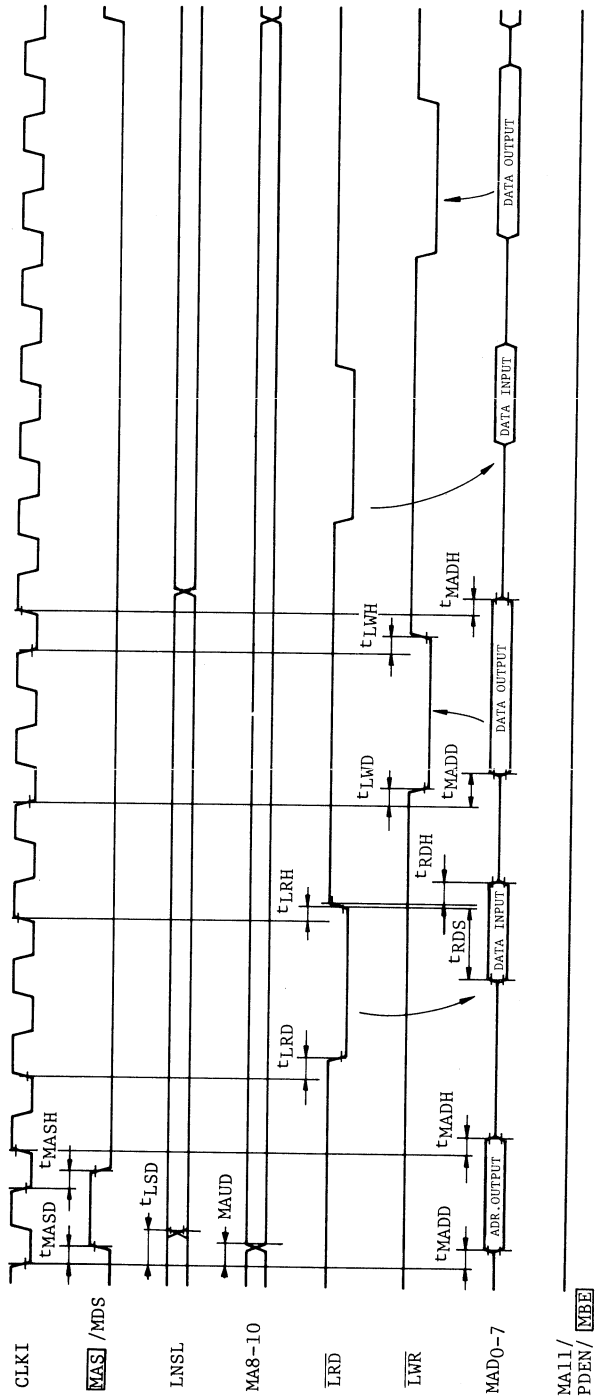


Fig. 14 Memory Bus Interface Timing in A Mode (1) During Image Data Processing

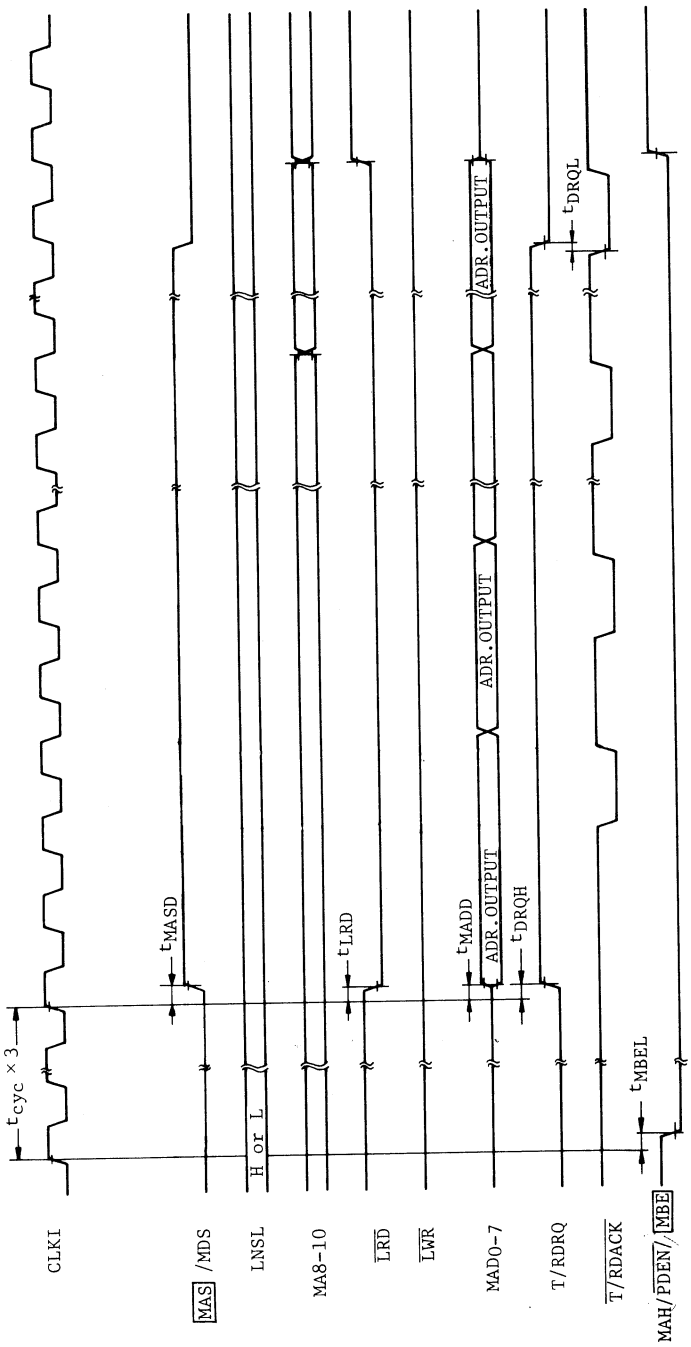


Fig. 15 Memory Bus Interface Timing in A Mode (2) During Burst DMA Transfer

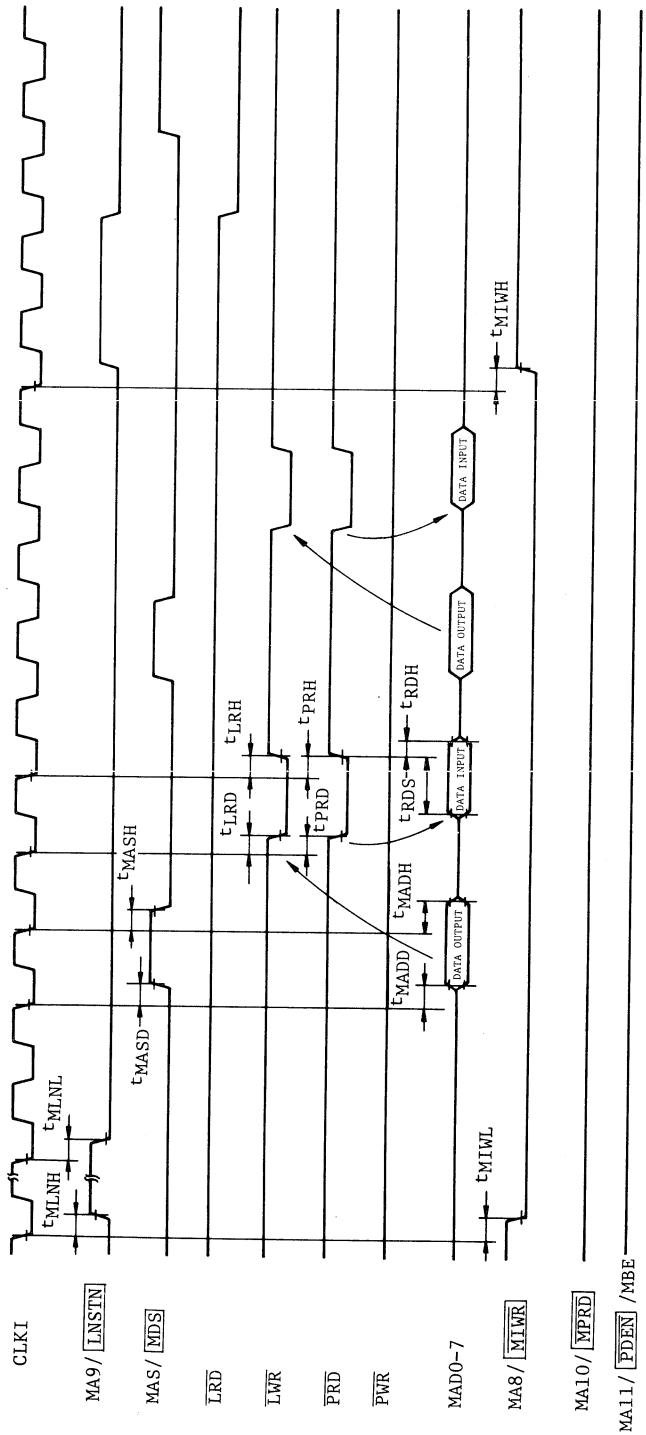


Fig. 16 Memory Bus Interface Timing in B Mode (1) During 4-bit Coded Data Output

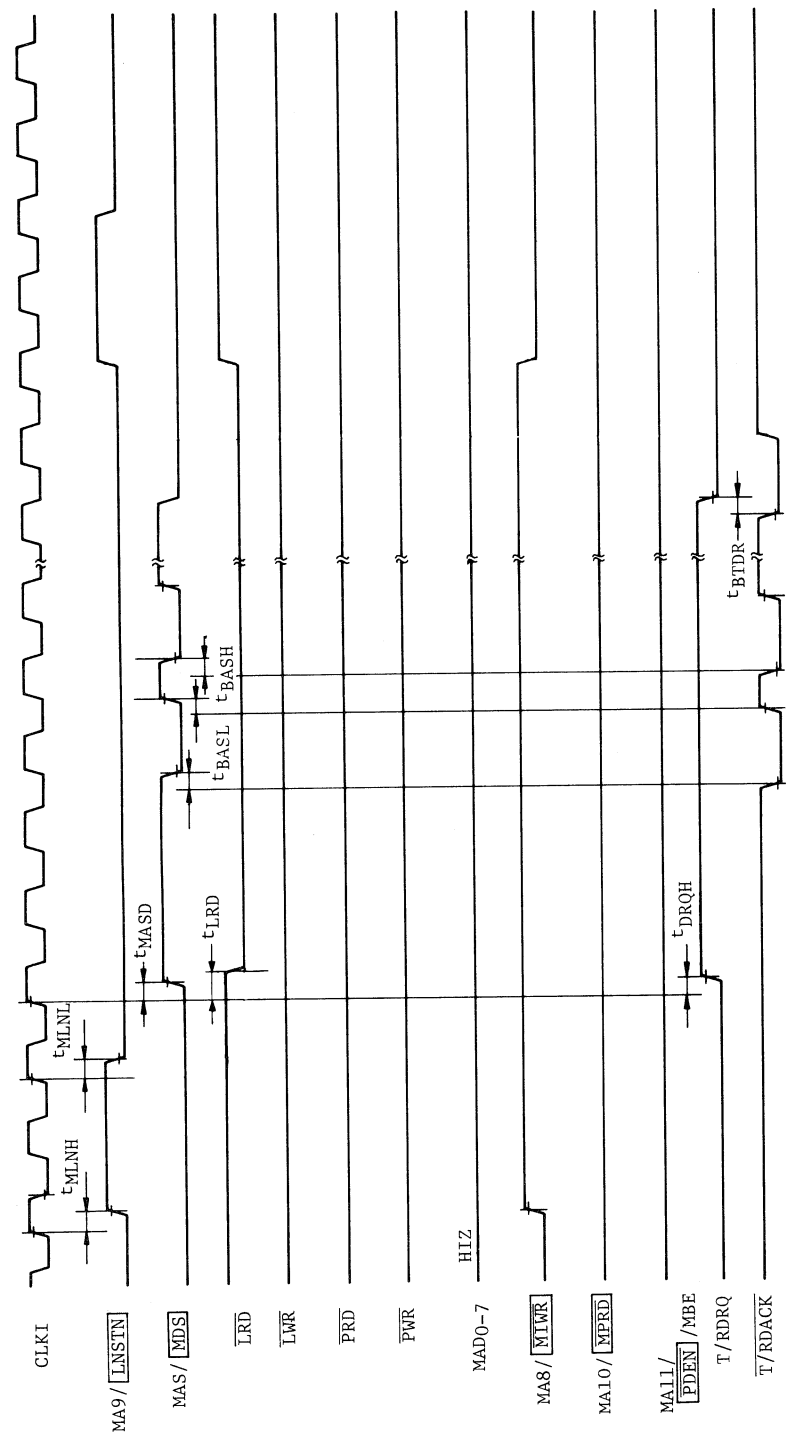


Fig. 17 Memory Bus Interface Timing in B Mode (2) During Burst DMA Transfer

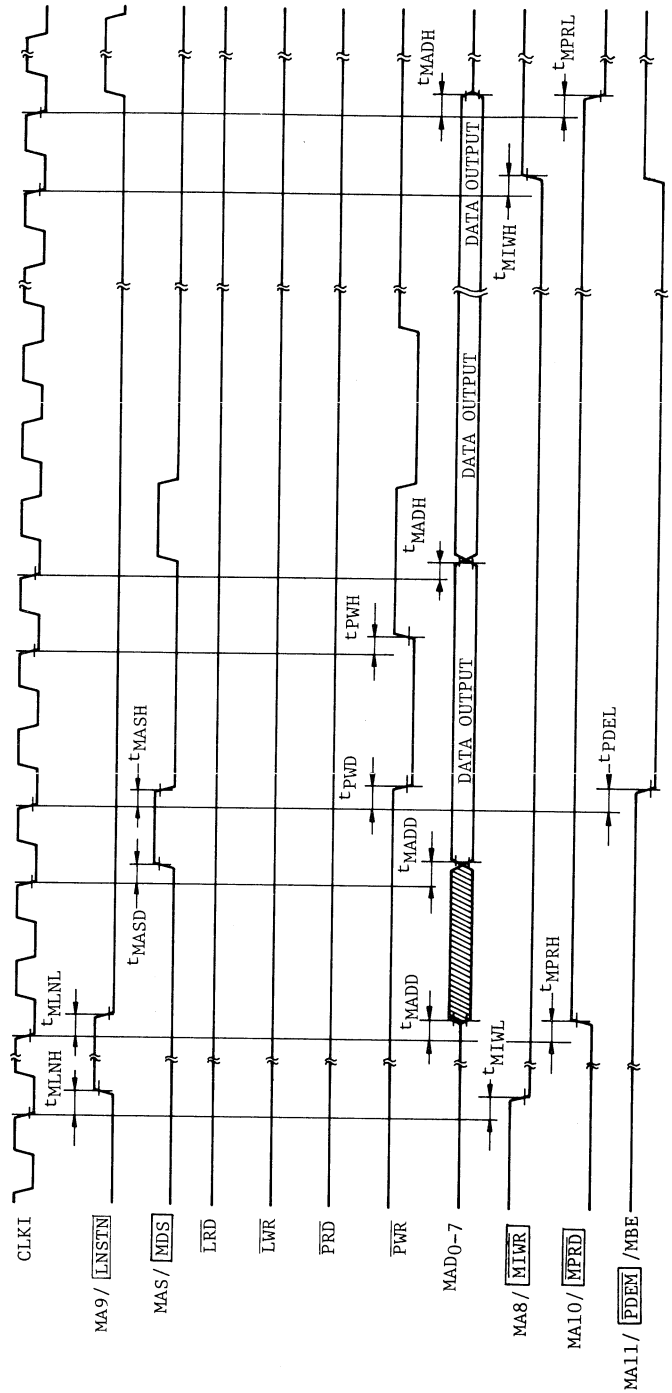


Fig. 18 Memory Bus Interface Timing in B Mode (3) During Pel Correction Data Detection

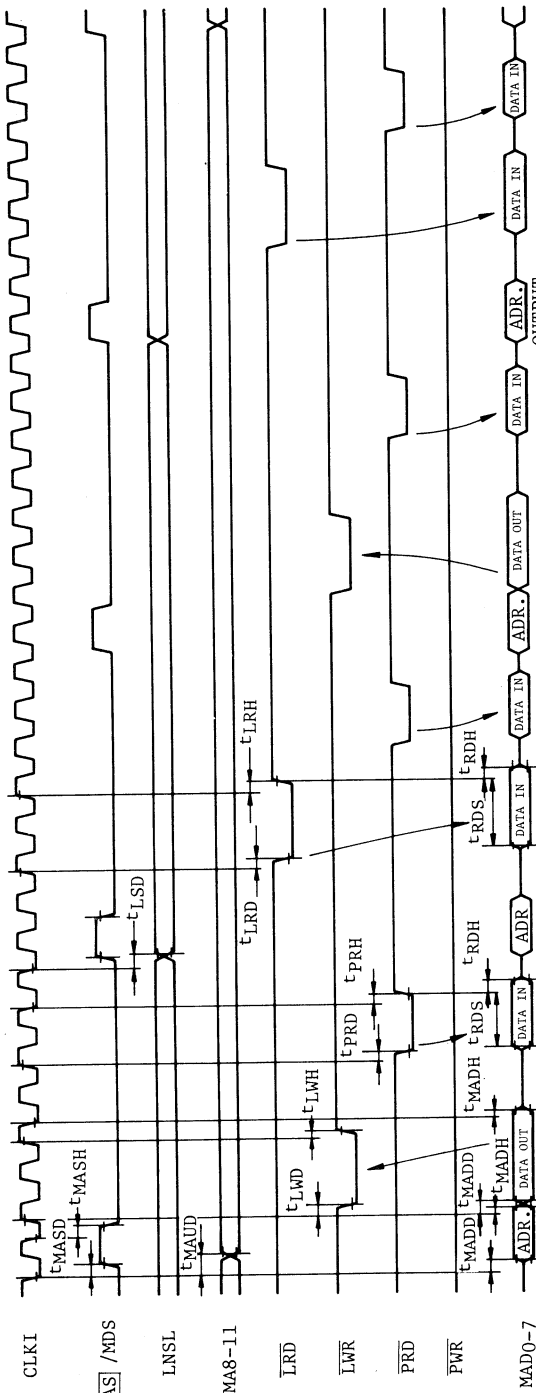


Fig. 19 Memory Bus Interface Timing in C or D Mode (1) During Image Data Processing

● Internal Analog Circuits

● Capacitance

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{IN}	f = 100kHz	—	—	12.5	pF
Output Capacitance	C_{OUT}		—	—	12.5	pF
Input/Output Capacitance	Cin/out		—	—	12.5	pF

* These parameters are sample values.

DC Characteristics

Item	Detailed Item	Symbol	Test Condition	min	typ	max	Unit
Input Current	VBL	L_{BL}	V_{BL}=3.5V	—	—	1.0	mA
Input Voltage Range	ISIN1,2	$V_{ISI1,2}$		1.5	—	3.5	V
	PEAKI	V_{INP}		1.5	—	3.0	
	SLICE1	V_{INS1}		1.5	—	3.5	
	SLICE2	V_{INS2}		1.5	—	3.5	
	VBL	V_{IBL}		0.3 × VDD	—	0.7 × VDD	
	VCL	V_{ICL}		0.3 × V_{DD}	—	0.7 × V_{DD}	
Output Current	IOUT	I_{OIO}		-16.0	—	-4.0	mA
	PEAKO	I_{OPK}		-5.0	—	-0.7	
	DAO	I_{ODO}		-6.0	—	-0.7	
Supply Current	Standby	I_{DS}		—	—	1	
	Operating	I_{DD}	CLKI=10MHz	—	—	60	

(to be continued)

Item	Detailed Item		Symbol	Test Condition	min	typ	max	Unit
Output Voltage	PEAK0	Resistance Chain Step 0	V_{P0}	$V_{CL}=V_{BL}$ =3.4V PEAKI = 1.5V	3.20	—	3.40	V
		Resistance Chain Step 255	V_{P255}		1.25	—	1.65	
	DA0	Resistance Chain Step 0	V_{D0}		1.40	—	1.60	
		Resistance Chain Step 127	V_{D127}		2.60	—	3.00	
	IOUT		V_{IOUT}	V_{ISIN1} = 2.5V	2.40	—	2.65	
Input Leakage Current	ISIN1		I_{LIS1}	V_{IN} = 0 to V_{DD}	-10	—	10	μA
	ISIN2		I_{LIS2}					
	PEAKI		I_{LPI}					
	SLICE1		I_{LSL1}					
	SLICE2		I_{LSL2}					
	VCL		I_{LVCL}					

AC Characteristics

Item	Detailed Item	Symbol	Test Condition	min	typ	max	Unit
Input Voltage Range	Peak to Peak Voltage	V_{IP}	f_{CLK}=10MHz	0.1	—	2.0	V
Operating Frequency	Image Signal Reading Frequency	V_{IF}	V_{BL}=3.4V V_{SLICE} = 1.8V	0.5	—	5.0	MHz

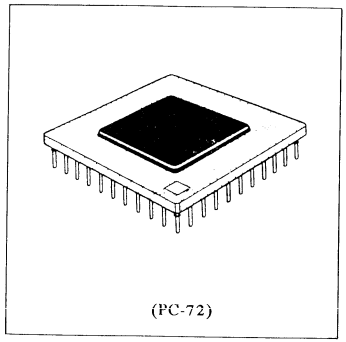
HD63085Y

Document Image Compression and Expansion Processor (DICEP)

The DICEP is an LSI that performs compression (or coding) and expansion (or decoding) of the digital data representing a document image.

The DICEP is used in G3 and G4 facsimile apparatus, intelligent copiers, word processors, telex, terminals, laser beam printers, file servers and other office automation systems.

The DICEP uses Modified Huffman (MH) coding scheme, Modified READ (MR) coding scheme and Modified MR (M^2R) coding scheme which are compatible with the CCITT (Comité Consultatif International Télégraphique et Téléphonique) recommendations for Group 3 and Group 4 facsimile apparatus.



(PC-72)

■KEY FEATURES

● Compatible with the CCITT Recommendations for Group 3 and Group 4 facsimile apparatus

The DICEP employs Modified Huffman (MH) coding scheme, Modified READ (MR) coding scheme and Modified MR (M^2R) coding scheme. These coding schemes are compatible with the CCITT recommendations for Group 3 and Group 4 facsimile apparatus.

● Simple MPU Command

As the DICEP stores coding and decoding algorithms in the microprogram ROM as firmware, a single MPU command allows this LSI to encode (i.e. compress) or decode (i.e. expand) a scan line of digital data.

● High Speed Coding and Decoding

The DICEP realizes high speed coding and decoding by:

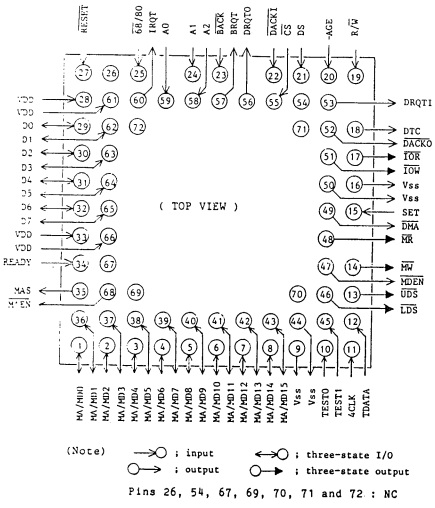
- o including a changing pels* detector which can detect a changing pel contained in a word (8 bits/16 bits) of document image data within an instruction cycle time (at least 125nsec), and
- o including a decoded pels generator which can generate a word (8 bits/16 bits) of document image data within an instruction cycle time.

(NOTE *) The term 'picture element' is abbribiated to 'pel' in this manual.

● Flexible System Configuration

- o Either 68 type MPU or 80 type MPU can be interfaced. The system bus has the size of 8 bits.
- o The DICEP has two bus interfaces ; the system bus interface and the document image bus interface.
- o The DICEP may be interfaced with two independent buses (i.e. the system bus and the document image bus), while it may be interfaced with a common bus.
- o The size of the document image bus is selectable (8 bits /16 bits) depending on the word size of document image memory.

■PIN ARRANGEMENT



(Top View)

This data only introduces an outline of the function. Please see the user's manual for details.

● High Speed DMA Transfer

o The DICEP can perform direct memory access (DMA) transfer between an I/O device (scanner or printer) and the document image memory. The maximum transfer rate is 4M Byte/sec .

o With a DMA controller (DMAC) on the system bus, DMA transfers can be performed between a memory on the system bus and the DICEP.

● A Variety of Programmable Parameters

Internal programmable registers present the DICEP flexibility to allow application to many kinds of systems.

o The parameters can be changed before initiation of every command.

o The length of a scan line is programmable from the word size of the document image memory (8 bits/16 bits) to 64K bits.

o One of coding operation, decoding operation and transfer operation can be selected.

o One of MH coding scheme, MR coding scheme, M^2R coding scheme and run length coding scheme can be selected.

o The minimum length of a coded scan line is programmable from 0 to 2^{16} - 1 bits.

o The number of End of Line (EOL) code words is programmable from 0 to 2^{16} - 1.

o The number of Return to Control (RTC) code words is programmable from 0 to 2^{16} - 1.

o The DICEP can code and decode a desired part of a document on a word (8 bits/16 bits) basis.

● Data Transfer between Buses

The DICEP can perform data transfer between the system bus and the document image bus without coding or decoding.

● Octet Mode

The DICEP provides Octet Mode. In this mode, a coded scan line or a coded page is 8-bit boundary conditioned.

● Run Length Coding Scheme

The DICEP provides run length coding scheme in addition to MH coding, MR coding and M²R coding.

● High Operating Speed

o Instruction cycle time is 125 nsec min. (at system clock of 8 MHz max.)

o Input clock frequency is 32 MHz max.

■FUNCTIONAL SUMMARY

No.	Item	Function
1	Coding Scheme	MH, MR, M²R, Run Length
2	Maximum Scan-line Length	64 K pels
3	Document Image Bus Addressing Capacity	Document Image Memory ..... 64K Byte I/O Devices ..... 64K Byte
4	Maximum DMA Transfer Rate	4M Byte/sec *1
5	Maximum Changing Pels Detect Speed	3.2M Byte/sec *1
6	Maximum Decoded Pels Generation Speed	3.2M Byte/sec *1
7	Coding Speed	See Fig. 1-2

*1 : Input clock frequency is 32 MHz.

■CODING SPEED

The DICEP operates with an instruction cycle time of 125 ns. Coding speed of the DICEP is given by:

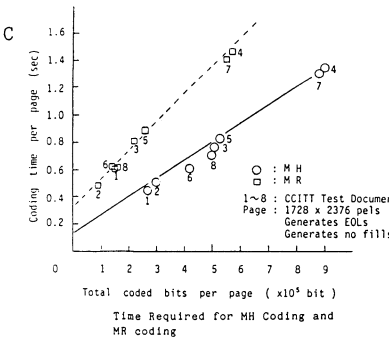
$$T = k1P + k2C$$

where P : number of pels in a page (pels/page)
C : a coded page (bits/page)
T : time required to encode a page (cycles/page)
k1, K2 : constants

(1) Coding speed with the MH coding

The DICEP needs 5 cycles to detect the changing pels in the 16 bit pels. In this case, k1 is 3.91 x 10^{-8} (sec/pel) and k2 is 1.26 x 10^{-6} (sec/bit). Therefore, T is given by:

$$T = 3.91 \times 10^{-8} \times P + 1.26 \times 10^{-6} \times C$$



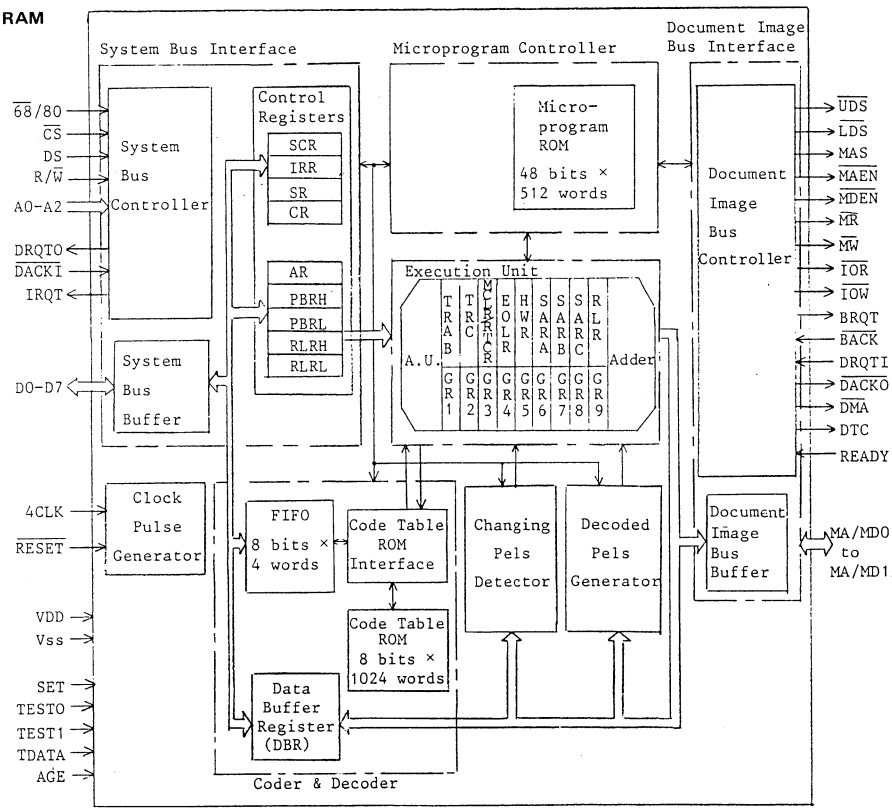
Time Required for MH Coding and MR coding

(2) Coding speed with the MR coding

The DICEP needs 9 cycles to detect the changing pels in the 16 bit pels. In this case, k1 is 7.03 x 10^{-8} (sec/pel) and k2 is 2.18 x 10^{-6} (sec/bit). Therefore, T is given by:

$$T = 7.03 \times 10^{-8} \times P + 2.18 \times 10^{-6} \times C$$

■**BLOCK DIAGRAM**



■BLOCK CONFIGURATIONS

● System Bus Interface

The system bus interface has a timing specification compatible with 8-bit MPUs (ex. 6800/8085). This block includes control registers which can be directly accessed by the MPU.

● Microprogram Controller

The microprogram controller stores coding and decoding programs in the microprogram ROM to control all other blocks of the DICEP.

This block consists of the microprogram ROM with 512 words of 48 bits, the sequence controller and the pipeline register.

● Execution Unit

The execution unit generates document image memory addresses, and calculates the position of changing pels, run lengths, and the relative distance between changing pels on the coding line and those on the reference line.

This block consists of eighteen 16-bit registers, the arithmetic unit (A.U.) and the adder. Nine registers (TRAB, TRC, MCLR/RTCR, EOLR, HWR, SARA, SARB, SARC and RLR) can be programmed by the MPU via the control registers in the system bus interface. These nine registers are called "parameter registers".

● Coder and Decoder

The coder generates the addresses of the code table ROM from input run lengths or relative distances, and generates appropriate code words by looking up the code table ROM.

On the other hand, the decoder generates the addresses of the code table ROM from input code words, and generates run lengths or relative addresses by looking up the code table ROM.

This block consists of the code table ROM with 1024 words of 8 bits, the code table ROM interface, the First-In First-Out memory (FIFO) with 4 words of 8 bits, and the Data Buffer Register (DBR). The code table ROM stores the data which is referenced for coding and decoding operations. The code table ROM interface generates the addresses of the code table ROM. The FIFO temporarily stores code words during coding or decoding operation. The DBR is a intermediate buffer which is used to

transfer data between the system bus and the document image bus.

● Changing Pels Detector

The changing pels detector detects a changing pel whose color is different from that of the previous pel on the same scan line. It can detect a changing pel in a word (8 bits/16 bits) of the document image memory within an instruction cycle time.

This block consists of two changing pels detectors : the reference line detector and the coding line detector. For detailed information of the reference line and the coding line, see '7. Coding Schemes'.

● Decoded Pels Generator

The decoded pels generator can generate at most a word (8 bits/16 bits) of decoded pels within an instruction cycle time, using the information of the positions of changing pels.

● Document Image Bus Interface

The document image bus interface provides an interface between the DICEP and the document image bus. It has a 16-bit multiplexed address/data bus.

This block has the following functions:

o it has bus arbitration technique.
o it outputs control signals for the document image bus.

■PIN DESCRIPTIONS

• System Bus Interface Pins

SIGNAL	PIN NO.	I/O	DESCRIPTIONS
$\overline{68}$/80	25	I	If $\overline{68}$/80 is low, it indicates that a 68 type MPU is interfaced with the DICEP. If high, it indicates that an 80 type MPU is interfaced.
A0	59	I	Addresses 0 to 2. These pins are connected to the 3 low-order bits of the system address bus to address the DICEP internal registers.
A1	24		
A2	58		
D0	29	I/O,	Data 0 to 7. These pins are interfaced with the system data bus to provide bidirectional communication between the MPU and the DICEP. The MPU can read/write the DICEP internal registers via D0 to D7 pins.
D1	62	3-state	
D2	30	output	
D3	63		
D4	31		
D5	64		
D6	32		
D7	65		
$\overline{CS}$	55	I	Chip select. A low level on this pin indicates that the MPU accesses a DICEP internal register.
DS	21	I	Data strobe. This pin must be connected to $\phi 2$ clock pin of 68 type MPU or $\overline{RD}$ pin of 80 type MPU.
R/$\overline{W}$	19	I	Read/Write. This pin is connected to R/$\overline{W}$ pin of 68 type MPU or $\overline{WR}$ pin of 80 type MPU.

(to be continued)

SIGNAL	PIN NO.	I/O	DESCRIPTIONS
$\overline{\text{RESET}}$	27	I	A low level on $\overline{\text{RESET}}$ initializes the DICEP.
4CLK	11	I	4 Clock. The clock frequency is four times as high as the DICEP system clock frequency.
IRQT	60	O	Interrupt Request. The DICEP sends an interrupt request to the MPU by driving IRQT high upon completion of a command, end of a DMA transfer, occurrence of decoding error or reception of Return to Control (RTC) code words. MPU can know the cause of an interrupt by reading the Interrupt Request Register (IRR). When the MPU reads the IRR, IRQT returns to the low state.
DRQTO	56	O	DMA Request Output. The DICEP can drive DRQTO high to provide DMA request to the DMA Controller (DMAC) when: (1) coded data of more than 1 byte are stored in the FIFO during coding operation, (2) the FIFO has empty space of more than 1 byte during decoding operation or (3) Data Buffer Register (DBR) is ready for a read or write operation during data transfer between the system bus and the document image bus.
$\overline{\text{DACKI}}$	22	I	DMA Acknowledge Input. This input is a response to DRQTO. When $\overline{\text{DACKI}}$ goes low during coding operation or decoding operation, the FIFO is accessed. If $\overline{\text{DACKI}}$ goes low during data transfer between the system bus and the document image bus, the DBR is accessed. $\overline{\text{CS}}$ and $\overline{\text{DACKI}}$ must not be pulled low together.

- **Document Image Bus Interface Pins**

SIGNAL	PIN NO.	I/O	DESCRIPTIONS
BRQT	57	O	Bus Request. When BRQT is driven high by DICEP, it indicates to all other potential bus master devices on the document image bus that the DICEP desires to become the bus master. When the document image bus has no other potential master device, BRQT does not have to be connected to any line.
$\overline{\text{BACK}}$	23	I	Bus Acknowledge. This input is a response to the BRQT. A low level on BACK indicates that the DICEP is granted to be the master of the document image bus. This pin must be fixed low when the document image bus has no potential bus master devices other than the DICEP.
$\overline{\text{MEAN}}$	68	O	Memory Address Enable. When $\overline{\text{MEAN}}$ is driven low by DICEP, it indicates that the DICEP has become the master of the document image bus. If $\overline{\text{MEAN}}$ is high, all of three state outputs interfaced with the document image bus are in high impedance state.
MAS	35	O	Memory address Strobe. When the DICEP drives MAS high, it indicates that the DICEP outputs an address onto MA/MDO through MA/MD15.
$\overline{\text{UDS}}$	13	3-state output	When $\overline{\text{UDS}}$ is driven low by DICEP, it indicates that the DICEP uses the high-order byte of the document image bus.
$\overline{\text{LDS}}$	46	3-state output	When $\overline{\text{LDS}}$ is driven low by DICEP, it indicates that the DICEP uses the low-order byte of the document image bus.
$\overline{\text{MDEN}}$	47	O	Memory Data Bus Enable. When $\overline{\text{MDEN}}$ is driven low by DICEP, it indicates that there is a valid data on MA/MDO through MA/MD15. This output is used to control the output of bidirectional bus buffer on the MA/MDO through MA/MD15.

(to be continued)

SIGNAL	PIN NO.	I/O	DESCRIPTIONS
MA/MD0 MA/MD1 MA/MD2 MA/MD3 MA/MD4 MA/MD5 MA/MD6 MA/MD7 MA/MD8 MA/MD9 MA/MD10 MA/MD11 MA/MD12 MA/MD13 MA/MD14 MA/MD15	1 36 2 37 3 38 4 39 5 40 6 41 7 42 8 43	I/O, 3-state output	Memory Address Data Bus. This is multiplexed address/data bus for document image bus operation. MA/MD0 – MA/MD15 are used as follows: 1) Output address lines when the $\overline{\text{MEAN}}$ is low and the MAS is high. 2) Input data lines when both $\overline{\text{MEAN}}$ and $\overline{\text{MDEN}}$ are low during read cycle. 3) Output data lines when both $\overline{\text{MEAN}}$ and $\overline{\text{MDEN}}$ are low during write cycle.
$\overline{\text{MR}}$	48	3-state output	Memory Read. The DICEP drives $\overline{\text{MR}}$ low to read data from the document image memory.
$\overline{\text{MW}}$	14	3-state output	Memory Write. The DICEP drives $\overline{\text{MW}}$ low to write data into the document image memory.
$\overline{\text{IOR}}$	17	3-state output	I/O Read. The DICEP drives $\overline{\text{IOR}}$ low to read data from an I/O device on the document image bus. However, $\overline{\text{IOR}}$ is used only for data transfer between buses or for DMA transfer through the document image bus during coding operation.
$\overline{\text{IOW}}$	51	3-state output	I/O Write. The DICEP drives $\overline{\text{IOW}}$ low to write data into an I/O device on the document image bus. However, $\overline{\text{IOW}}$ is used only for data transfer between buses or for DMA transfer through the document image bus during decoding operation.
DRQTI	53	I	DMA Request Input. DRQTI is driven high when an I/O device on the document image bus sends a DMA request to the DICEP.
$\overline{\text{DACKO}}$	52	O	DMA Acknowledge Output. When this output is driven low, it notifies the peripherals on the document image bus that they have been granted a DMA operation.

(to be continued)

SIGNAL	PIN NO.	I/O	DESCRIPTIONS
DMA	49	O	Direct Memory Access. When DMA is driven low, it indicates that the DICEP is executing a DMA transfer. During coding operation, data is transferred from the I/O device (scanner) to the document image memory. During decoding operation, data is transferred from the document image memory to the I/O device (printer).
DTC	18	O	DMA Terminal Count. When DTC is driven high, it indicates that DMA transfer of a scan line has been completed.
READY	34	I	When READY is high during a read or write to the document image memory or the I/O devices, it indicates that the memory or I/O device is ready to send or receive data. If READY is low, the DICEP will wait until READY becomes high.

- **Power Supplies & Others**

SIGNAL	PIN NO.	I/O	DESCRIPTIONS
V_{DD}	28, 33 61, 66	I	Supply voltage (+5V)
V_{SS}	9, 16 44, 50	I	Ground
SET TEST0 TEST1 TDATA AGE	15 10 45 12 20	I	These pins must be fixed low.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}*	−0.3 to +7.0	V
Input Voltage	Vin*	−0.3 to V_{DD} +0.3	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +150	°C

* Voltage referenced to V_{SS}=0V.

■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{DD}*	4.75	5	5.25	V
Input Voltage	V_{IL}*	−0.3	–	0.8	V
	V_{IH}*	2.2	–	V_{DD}	V
Operating Temperature	Topr	0	25	70	°C

* Voltages referenced to V_{SS}=0V.

■DC CHARACTERISTICS (V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Input High Voltage	V_{IH}		2.2	–	V_{DD} +0.3	V
Input Low Voltage	V_{IL}		−0.3	–	0.8	V
Input Leakage Current	I_{IN}	Vin=0 to 5.25V	−10	–	10	μA
Three-State (Off State) Leakage Current	I_{tsi}	Vin=0 to 5.25V	−10	–	10	μA
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	–	–	V
Output Low Voltage	V_{OL}	I_{OL}=2mA	–	–	0.4	V
Standby Current	I_{DDS}		–	–	1	mA
Power Dissipation	P_T		–	–	250	mW

■CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{IN}	f = 1MHz	–	–	8	pF
Output Capacitance	C_{OUT}		–	–	10	pF
Input/Output Capacitance	$C_{I/O}$		–	–	12	pF

* These parameters are sample values.

■AC CHARACTERISTICS

- **Clock Timing** (V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
4CLK Cycle Time	ϕ4CLK	Fig. 1	31.25	–	500	ns	4CLK

- **System Bus Timing**

  Using a 68 Type MPU (V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C, Cout=140pF unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
DS Cycle Time	tCYCLE	Fig. 2, Fig. 5	500	–	–	ns	DS
DS Pulse Width	PWEH, PWEL	Fig. 2, Fig. 5	220	–	–	ns	DS
DS Rise or Fall Time	tr, tf	Fig. 2, Fig. 5	–	–	25	ns	DS
Address Setup Time	tAS	Fig. 2	70	–	–	ns	$\overline{CS}$, A0-A2, R/$\overline{W}$
Address Hold Time	tAH	Fig. 2	30	–	–	ns	$\overline{CS}$, A0-A2, R/$\overline{W}$
Output Data Delay Time	tDDR	Fig. 2, Fig. 5	–	–	180	ns	D0-D7
Output Data Hold Time	tDHR	Fig. 2, Fig. 5	10	–	–	ns	D0-D7
Input Data Setup Time	tDSW	Fig. 2, Fig. 5	60	–	–	ns	D0-D7
Input Data Hold Time	tDHW	Fig. 2, Fig. 5	40	–	–	ns	D0-D7
$\overline{DACKI}$ Setup Time	tAS	Fig. 5	70	–	–	ns	$\overline{DACKI}$
$\overline{DACKI}$ Hold Time	tAH	Fig. 5	30	–	–	ns	$\overline{DACKI}$

Using an 80 Type MPU (V_{DD}=5.0±5%, V_{SS}=0V, Ta=0 to +70°C, Cout=140pF unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
Address Setup Time	tAR	Fig. 3	70	–	–	ns	$\overline{CS}$, A0-A2
Address Hold Time	tRA	Fig. 3	30	–	–	ns	$\overline{CS}$, A0-A2,
Output Data Delay Time	tRD	Fig. 3, Fig. 6	–	–	180	ns	D0-D7
Output Data Hold Time	tDR	Fig. 3, Fig. 6	10	–	–	ns	D0-D7
Read Pulse Width	tRW	Fig. 3, Fig. 6	200	–	–	ns	DS
Address Setup Time	tAW	Fig. 4	70	–	–	ns	$\overline{CS}$, A0-A2
Address Hold Time	tWA	Fig. 4	30	–	–	ns	$\overline{CS}$, A0-A2
Input Data Setup Time	tWD	Fig. 4, Fig. 7	60	–	–	ns	D0-D7
Input Data Hold Time	tDW	Fig. 4, Fig. 7	40	–	–	ns	D0-D7
Write Pulse Width	tWW	Fig. 4, Fig. 7	200	–	–	ns	R/$\overline{W}$
$\overline{DACKI}$ Setup Time	tAR	Fig. 6	70	–	–	ns	$\overline{DACKI}$
$\overline{DACKI}$ Hold Time	tRA	Fig. 6	30	–	–	ns	$\overline{DACKI}$
$\overline{DACKI}$ Setup Time	tAW	Fig. 7	70	–	–	ns	$\overline{DACKI}$
$\overline{DACKI}$ Hold Time	tWA	Fig. 7	30	–	–	ns	$\overline{DACKI}$

- **Document Image Bus Timing**

  V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C, Cout=140pF unless otherwise noted.
  However, the values in the parentheses are the values at Cout=50pF.

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
Address Enable Active Delay Time	tDAEL	Fig. 8, Fig. 9	–	(70)	150	ns	$\overline{MAEN}$
Address Enable Inactive Delay Time	tDAEH	Fig. 8, Fig. 9	–	(70)	140	ns	$\overline{MAEN}$
Address Strobe Active Delay Time	tDASH	Fig. 8, Fig. 9	–	(70)	140	ns	MAS
Address Strobe Inactive Delay Time	tDASL	Fig. 8, Fig. 9	–	(60)	120	ns	MAS
Data Strobe Valid Delay Time	tDDSV	Fig. 8, Fig. 9	–	(60)	140	ns	$\overline{UDS}$, $\overline{LDS}$
Data Strobe Active Delay Time	tDDSL	Fig, 8, Fig. 9	–	(75)	140	ns	$\overline{UDS}$, $\overline{LDS}$
Data Strobe Inactive Delay Time	tDDSH	Fig. 8, Fig. 9	–	(75)	140	ns	$\overline{UDS}$, $\overline{LDS}$
Data Enable Active Delay Time	tDDEL	Fig. 8	–	(80)	130	ns	$\overline{MDEN}$
Data Enable Inactive Delay Time	tDDEH	Fig. 8	–	(75)	140	ns	$\overline{MDEN}$
Read Valid Delay Time	tDRDV	Fig. 8, Fig. 9	–	(60)	140	ns	$\overline{IOR}$, $\overline{MR}$
Read Active Delay Time	tDRDL	Fig. 8, Fig. 9	–	(70)	140	ns	$\overline{IOR}$, $\overline{MR}$
Read Inactive Delay Time	tDRDH	Fig. 8, Fig. 9	–	(75)	140	ns	$\overline{IOR}$, $\overline{MR}$
Write Valid Delay Time	tDWRV	Fig. 8, Fig. 9	–	(60)	140	ns	$\overline{IOW}$, $\overline{MW}$

(to be continued)

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
Write Active Delay Time	tDWRL	Fig. 8, Fig. 9	–	(70)	140	ns	$\overline{IOW}$, $\overline{MW}$
Write Inactive Delay Time	tDWRH	Fig. 8, Fig. 9	–	(80)	140	ns	$\overline{IOW}$, $\overline{MW}$
Address Valid Delay Time	tMAV	Fig. 8, Fig. 9	–	(75)	140	ns	MA/MD0-MA/MD15
Address Hold Delay Time	tMAH	Fig. 8, Fig. 9	25	(50)	–	ns	MA/MD0-MA/MD15
Data Setup Time (Read)	tDSR	Fig. 8	10	(10)	–	ns	MA/MD0-MA/MD15
Data Hold Time (Read)	tDHR	Fig. 8	70	(70)	–	ns	MA/MD0-MA/MD15
Data Delay Time (Write)	tDDW	Fig. 8	–	(95)	170	ns	MA/MD0-MA/MD15
Data Hold Time (Write)	tDHW	Fig. 8	15	(15)	–	ns	MA/MD0-MA/MD15
DMA Acknowledge Active Delay Time	tDAKL	Fig. 9	–	(60)	140	ns	$\overline{DACKO}$
DMA Acknowledge Inactive Delay Time	tDAKH	Fig. 9	–	(65)	140	ns	$\overline{DACKO}$
DMA Active Delay Time	tDDMAL	Fig. 9	–	(80)	140	ns	$\overline{DMA}$
DMA Inactive Delay Time	tDDMAH	Fig. 9	–	(70)	140	ns	$\overline{DMA}$
DTC Active Delay Time	tDDTCH	Fig. 9	–	4CLK +75	4CLK 140	ns	DTC
DTC Inactive Delay Time	tDDTCL	Fig. 9	–	(50)	130	ns	DTC

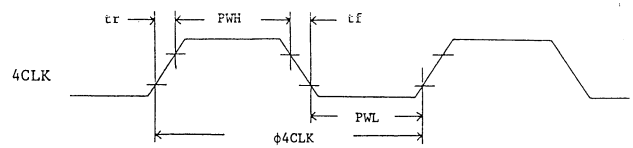


Fig. 1 Clock Timing

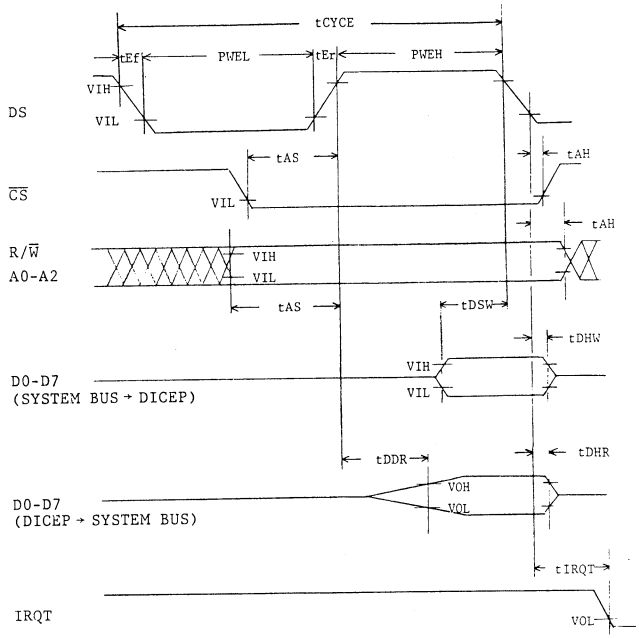


Fig. 2 System Bus Read/Write Timing
(68 Type MPU)

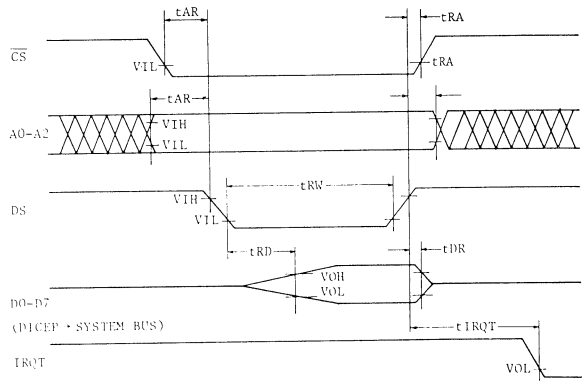


Fig. 3 System Bus Read Timing
(80 Type MPU)

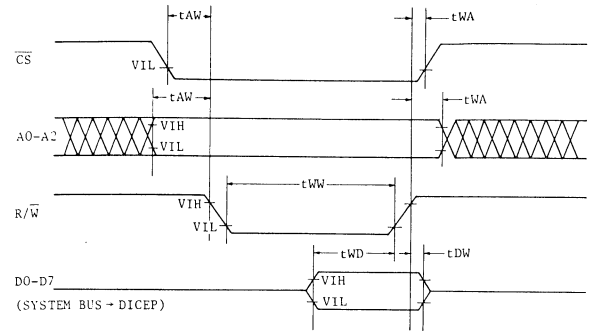


Fig. 4 System Bus Write Timing
(80 Type MPU)

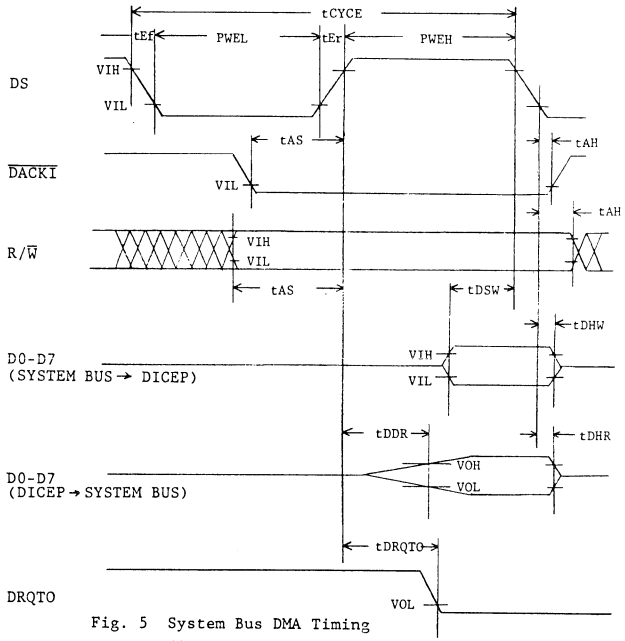


Fig. 5 System Bus DMA Timing
(68 Type MPU)

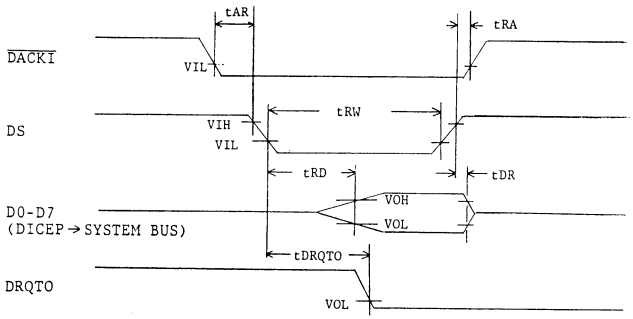


Fig. 6 System Bus DMA Timing
(DICEP → SYSTEM BUS)
(80 Type MPU)

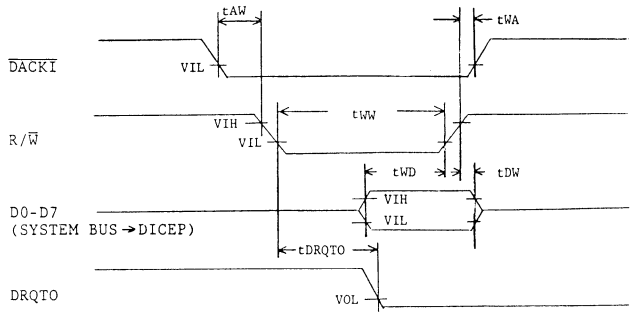


Fig. 7 System Bus DMA Timing
(SYSTEM BUS → DICEP)
(80 Type MPU)

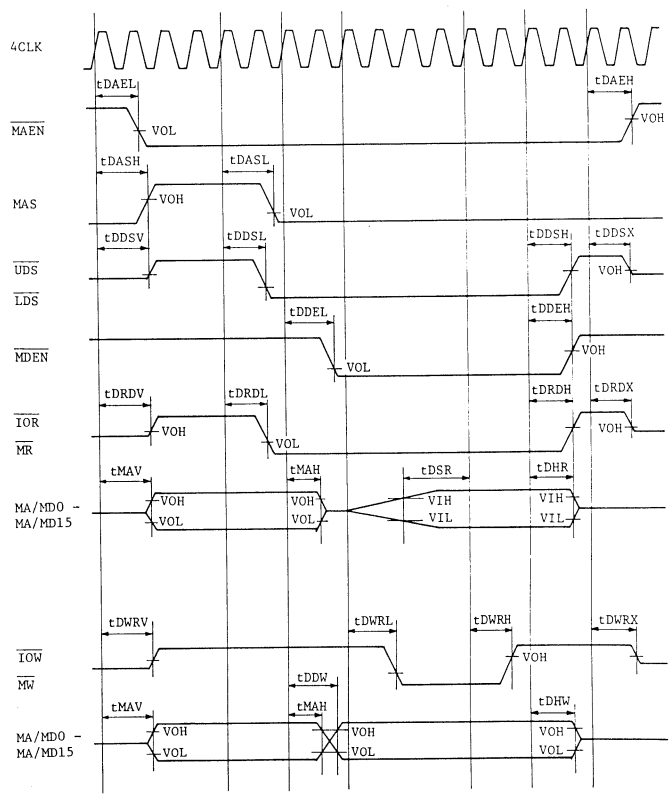


Fig. 8 Document Image Bus Read/Write Timing

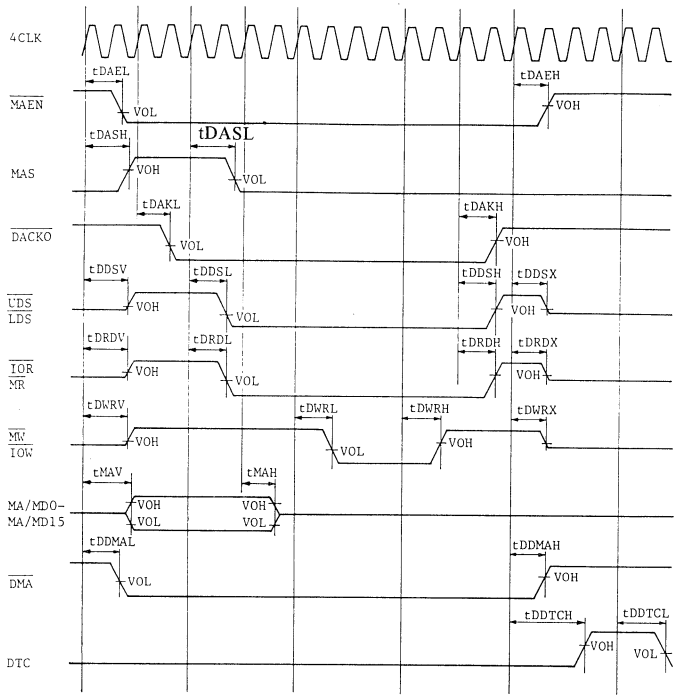


Fig. 9 Document Image Bus DMA Timing

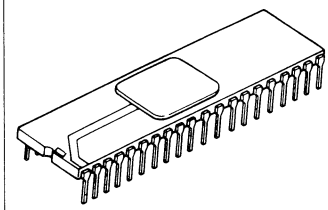
Digital Signal Processor(HSP)

HD61810

High Performance Signal Processor

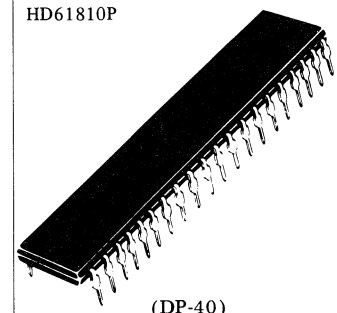
A High Performance Signal Processor (HSP) is a single chip processor with a stored program designed for a high speed digital signal processing. The HSP contains a high speed floating point arithmetic unit and performs an operation (addition/subtruction/multiplication) with an instruction in a single cycle of only 250 ns. Moreover, the HSP employs a CMOS process to realize a low power consumption.

HD61810



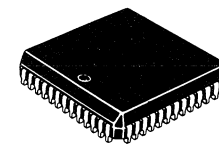
(DC-40)

HD61810P



(DP-40)

HD61810CP



(CP-52)

■KEY FEATURES

- 3 μm CMOS technology
- Arithmetic
  - Floating point arithmetic
  - Pipeline control
  - Horizontal microinstructions
- Large capacity memories
  - 200 × 16-bit data RAM (2-port accessible)
  - 128 × 16-bit data ROM
  - 512 × 22-bit instruction ROM
- System bus compatible with 8/16-bit microcomputer
- DMA operation between the HSP and external memory
- Serial I/O interface for up to 16 bits
- Operation speed
  - Input clock ; 16 MHz
  - Internal clock ; 4 MHz
  - Instruction cycle; 250 ns
  - MULT, ALU ; 250 ns (throughput with pipeline control)
- A single power supply of +5V
- Low power dissipation of 250 mW typ.
- Two levels of subroutine and interrupt
- Interrupt by three factors (end of three kinds of data I/O transfer)

■ARCHITECTURE

● Floating Point Arithmetic

The floating point arithmetic expresses a number with a mantissa and an exponent as follows;

$$n = a \cdot 2^b \quad (a;\ \text{mantissa},\ b;\ \text{exponent})$$

The floating point arithmetic allows a wide range of numbers to be expressed with less bits, and realizes an easy programming without digit adjustment.

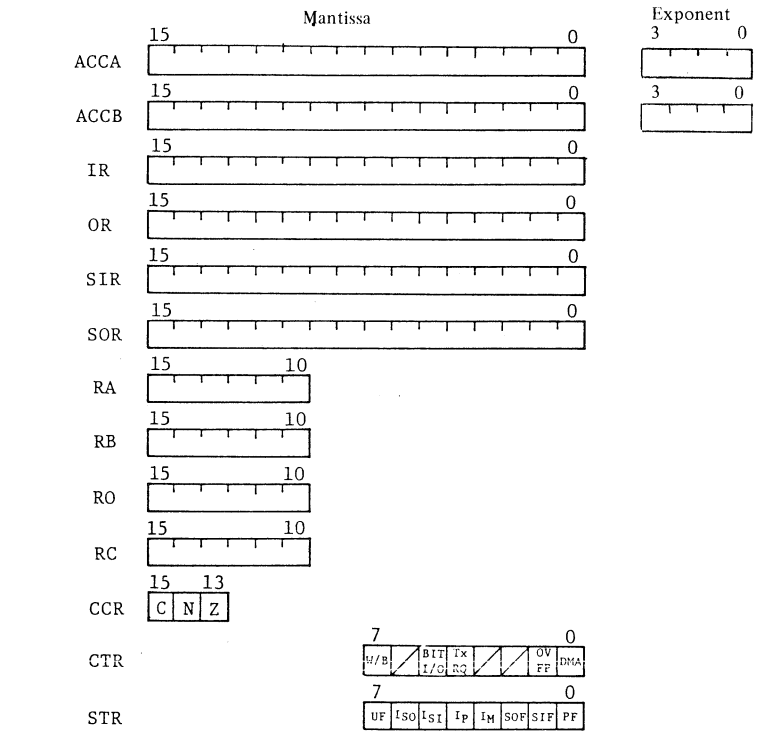
The HSP provides 16 bits for mantissa and 4 bits for exponent and can always work in the maximum precision (16 bits).

In the ALU and an accumulator, the mantissa is 16 bits and the exponent is 4 bits, while in multiplier and memory, the mantissa is 12 bits and the exponent is 4 bits. These data formats allow the HSP to have the precision given by the hatches in next figure in the floating point operation. As the exponent is 4 bits, it is fixed to -8 when the data amplitude is low. Therefore, the effective bit length varies in proportion to the data amplitude. When the data exceeds 2^{-8}, the mantissa is normalized and the exponent varies; the effective bit length is fixed to 16 bits maximum.

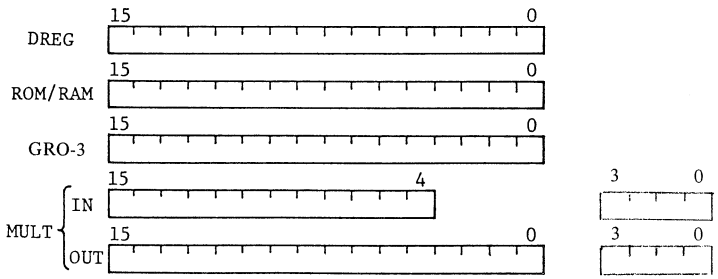
As described above, the HSP realizes a 32-bit dynamic range with 16 bits of the mantissa and 4 bits of the exponent.

This data only introduces an outline of the function.
Please see the user's Manual for details.

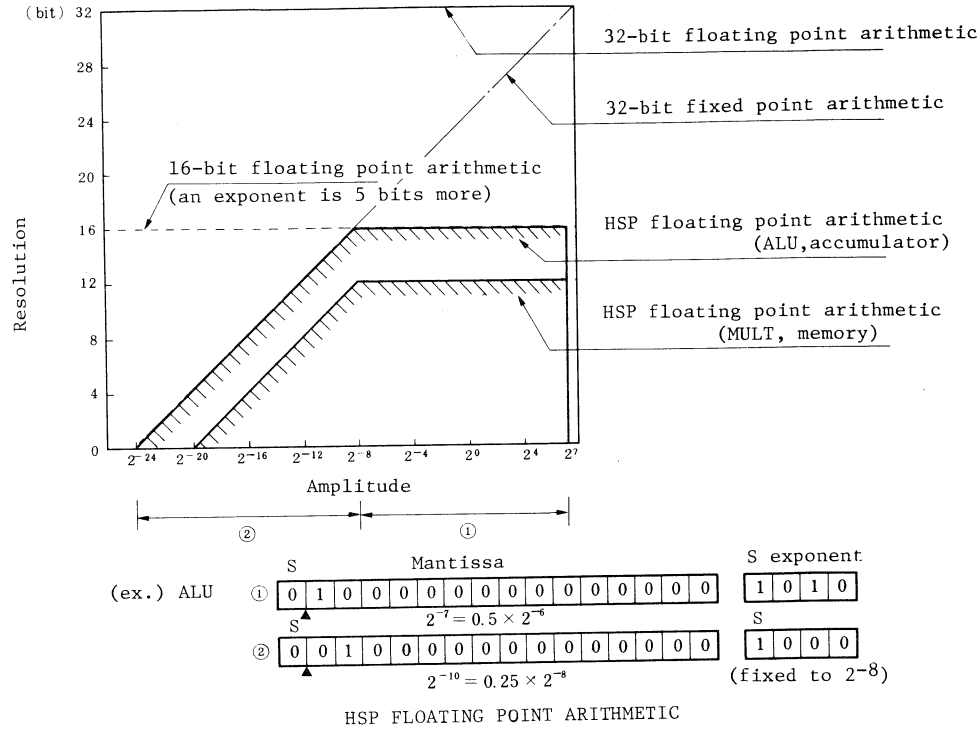
■HSP REGISTER MODEL



I/O register, General purpose register, ROM/RAM corresponding bit

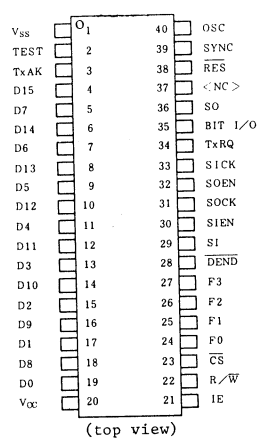


(Note) ROM/RAM 16 bits read and write:
In the floating point operation, lower 4 bits of the memory used as the exponent part.



HSP FLOATING POINT ARITHMETIC

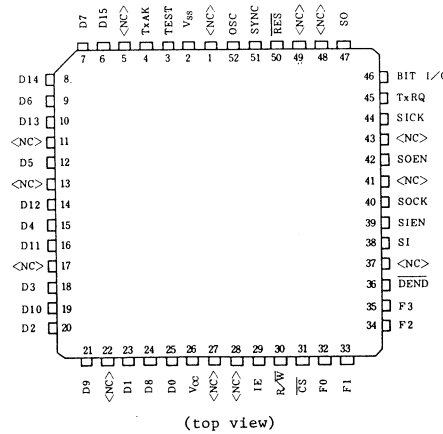
■PIN ARRANGEMENT



(top view)

(NOTE) Any line should not be connected to <NC> pins.

DIC/DIP PACKAGE PIN ASSIGNMENT



(top view)

(NOTE) Any line should not be connected to <NC> pins.

PLCC PACKAGE PIN ASSIGNMENT

■PIN FUNCTIONS

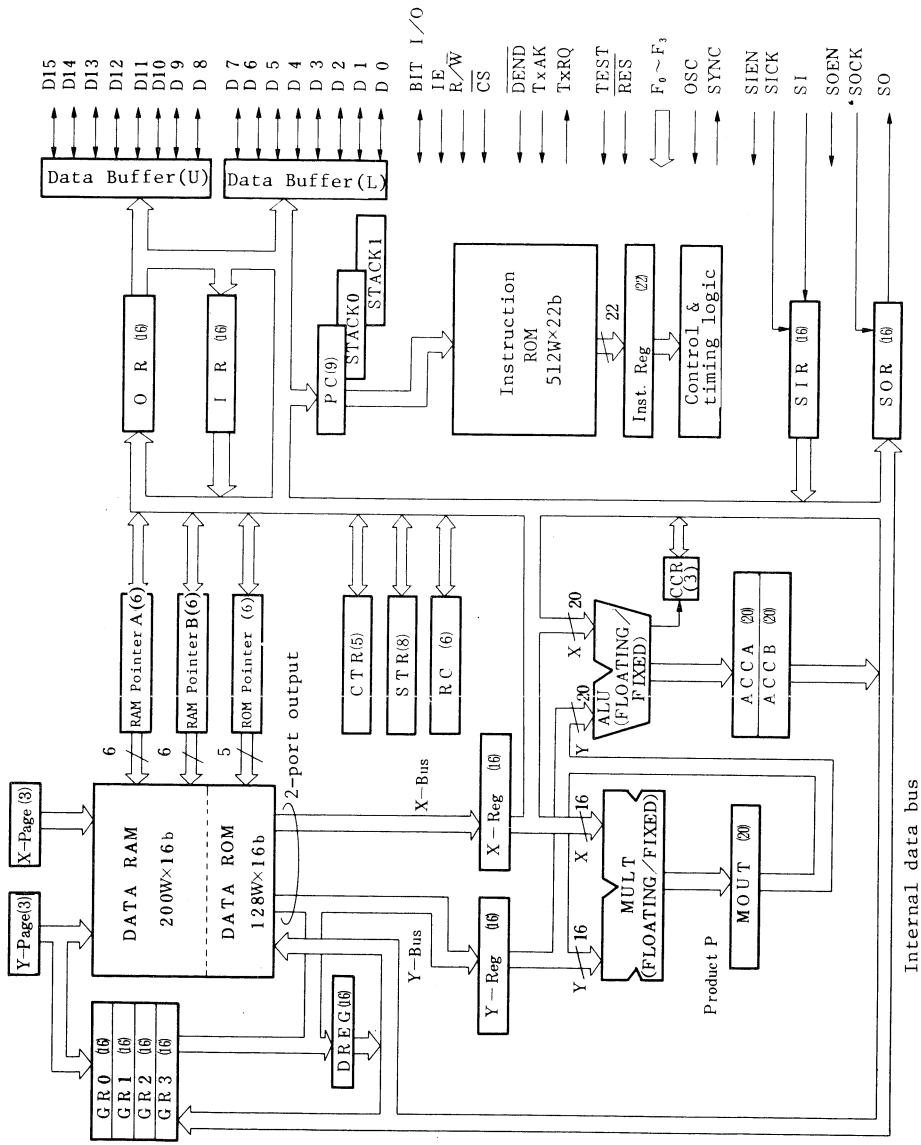
(Each pin number corresponds to that of DIP package.)

Signal	Pin	I/O	Functions
			Power Supply
Vcc	20		5V
Vss	1		0V
			Clocks
OSC	40	I	The external clock used to operate the HSP. Clock rate; 16 MHz
SYNC	39	O	The internal clock of the HSP. Clock rate; 4 MHz
			Serial I/O
SICK	33	I	Serial input clock. The serial data is input synchronously with this clock.
SIEN	30	I	Serial input enable. The serial input data is fetched into the serial input register with high level of SIEN. After the completion of a fetch, an interrupt can be generated in the HSP.
SI	29	I	Serial data input. Enters the serial data into the serial input register on the negative edge of SICK.
SOCK	31	I	Serial output clock. The serial data is output synchronously with this clock.
SOEN	32	I	Serial output enable. The serial output data is output from the serial output register with high level of SOEN. After the completion of output, an interrupt can be generated in the HSP on the negative edge of SOEN.
SO	36	O	Serial data output. Three states. Outputs the serial data from the serial output register on the positive edge of SOCK. When SOEN is low, this pin goes to the high-impedance state.
			DMA Operation
TxAK	3	I	Transfer acknowledge. DMA data transfer acknowledge input signal.
TxRQ	34	O	Transfer request, open drain output. Used mainly in the DMA operation mode. This signal requests the external device (DMAC) to transfer data. If TxRQ (DMA transfer request bit) in the control register (CTR) is set, this pin goes to the high level, which requests a DMA service. This signal is automatically cleared with an input of TxAK. Even in the DMA operation mode, internal data transfer among the input/output register (IR/OR), an accumulator and memory is controlled by software. TxRQ can be used as just an output pin in the non-DMA operation mode, and the status of TxRQ is altered by software.
$\overline{\text{DEND}}$	28	I	DMA operation end signal. When $\overline{\text{DEND}}$ is active low, a DMA operation is completed.

(to be continued)

Signal	Pin	I/O	Functions
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	19 17 15 13 11 9 7 5 18 16 14 12 10 8 6 4	I/O ↓ I/O	Data Bus Three states, bidirectional I/O ports. The direction of data bus depends on Read/Write (R/$\overline{W}$) control signal. When $\overline{CS}$ (Chip Select) is high, these pins are placed in the high-impedance state. The contents of the CTR and the function control pins (F0 to F3) select 8-bit or 16-bit transfer mode.
F0 F1 F2 F3	24 25 26 27	I I I I	Parallel I/O Control Function control. These signals select an internal register for the parallel data I/O. Connected to address buses of the microcomputer (6800/68000).
$\overline{CS}$	23	I	Chip select. The chip select signal enables the parallel I/O. When $\overline{CS}$ is active low, D0 to D15, F0 to F3, R/$\overline{W}$ and IE are valid.
R/$\overline{W}$	22	I	Read/Write signal of the microcomputer. Data is read from the HSP with high level of this pin, and is written into the HSP with low level. Valid only when $\overline{CS}$ is active low.
IE	21	I	Interface enable. Data transfer timing signal on data bus (D0 to D15). The data on the data bus is transferred to the internal shift register with this signal. Valid only when $\overline{CS}$ is active low.
TEST	2	I	Chip test pin (tied to GND).
$\overline{RES}$	38	I	Reset pin. The low level input of $\overline{RES}$ clears the program counter (PC). In the status register (STR), interrupt mask flag I_M is set to disable an interrupt, and the I/O data transfer end flags (PF, SIF and SOF) are cleared. In the control register, DMA and TxRQ bits for DMA operation are cleared. When $\overline{RES}$ goes to high level, the program is executed from location 1. The instruction of location 0 is not executed. (note) To reset, $\overline{RES}$ should remain low for more than 1 μs when OSC is applied.
BIT I/O	35	I/O	Open drain output, 1-bit bidirectional I/O pin. The status of BIT I/O depends on software. Set the internal flip-flop of BIT I/O to a one before data input.

■BLOCK DIAGRAM



Input/Output Registers		
Input Register	IR	16-bit register. Data is input to this register through the external data bus (D0-D15).
Output Register	OR	16-bit register. Data is output from this register to the external data bus (D0-D15).
Serial Input Register	SIR	16-bit shift register for serial data input. After a serial data is transferred from the SIR to an accumulator (ACCA or ACCB), the SIR is cleared.
Serial Output Register	SOR	16-bit shift register for serial data output. If data has been transferred to the SOR through the internal data bus, the data is output to peripherals on a bit basis.
Control Registers		
Condition Code Register	CCR	The CCR contains three flag bits; Carry (C), Negative (N), and Zero (Z). They indicate the results of ALU operation.
Status Register	STR	The STR flags are individually set or cleared depending on the status of the HSP. The contents of the STR can be transferred to an accumulator.
Control Register	CTR	The CTR is used to select the desired operating modes for the HSP. The CTR contents are determined by either the HSP instructions or the MPU.
Instruction Controllers		
Instruction ROM		A 512 word by 22 bit ROM. The instruction ROM stores instructions for the HSP. 22-bit instruction is transferred to the instruction register in parallel in a single instruction cycle.
Program Counter	PC	The PC is a 9-bit address counter that is used to address the Instruction ROM. The PC generates the instruction ROM addresses 0 through 511.
Stack Registers	STACK0 STACK1	The stack registers are 9-bit registers that are used to save the PC contents. The contents of the PC is pushed onto these registers when a subroutine jump or an interrupt occurs.
Repeat Counter	RC	6-bit down counter. The RC is used for repeated execution of an instruction and for the control of loops.
Instruction Register	Inst. Reg.	22-bit buffer register. This register temporarily stores the instruction transferred from the instruction ROM.

Internal Memory Controllers		
Data RAM		A 200 word by 16 bit RAM. 50 ward x 4 pages (page 0 through 3)
Data ROM		A 128 word by 16 bit ROM. 32 word x 4 pages (page 4 through 7)
RAM Pointer A RAM Pointer B	RA RB	These are 6-bit address pointers which are used to generate the data RAM address, combining with the contents of page address.
ROM Pointer	RO	This is a 6-bit address pointer which is used to generate the data ROM address, combining with the contents of page address.
X and Y page Address Pointers	X/Y-Page	These are 3-bit buffer registers for a page address. The effective address for the data RAM or the data ROM consists of this address and the contents of the RAM/ROM pointer.
General Registers	GR0-3	16-bit general purpose registers. The GRs can be used as working registers. Data is transferred to or from the GRs through the Y-Bus.
Delay Register	DREG	16-bit register. The DREG holds the data to be transferred through the Y-but for a single instruction cycle period.
Arithmetic Elements		
Accumulator A Accumulator B	ACCA ACCB	20-bit accumulators. The accumulators store the output from the ALU. Either the ACCA or ACCB is selected in response to the instructions.
Arithmetic Logic Unit	ALU	The ALU performs arithmetic and logical operations. Either the fixed point operation or the floating point operation is selected depending on the instructions.
Multiplier	MULT	The MULT performs a multiply operation. Either the fixed point operation or the floating point operation is selected depending on the instructions.
Multiplier Input X-Register	X-Reg.	16-bit register. The X-Reg. holds the data transferred from the X-bus or the internal data bus during a multiply operation.
Multiplier Input Y-Register	Y-Reg.	16-bit register. The Y-Reg. holds the data transferred from the Y-bus or the internal data bus during a multiply operation.
Multiplier Output Register	MOUT	This is a 20-bit buffer register which holds the output from the MULT for a single instruction cycle period. This register consists of a mantissa (16 bits) and an exponent (4 bits).

■INTERNAL RESOURCES

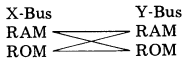
The HSP contains large capacity memories; a data RAM of 200 word × 16 bits, a data ROM of 128 words × 16 bits and an instruction ROM of 512 words × 22 bits, and contains dedicated multiplier and ALU which permit high-speed, high-accuracy floating point operation. The instruction ROM stores a comprehensive instruction set, which allows a wide range of applications.

■MEMORY ADDRESSING MODE

There are two modes of data memory addressing; pointer addressing and direct addressing.

(1) Pointer addressing mode
Pointer addressing uses the page address (0 through 7 page) and the pointer address as the data memory address. Page address is contained in the instruction code, and the pointer address is determined by each address pointer (RA/RB/RO).

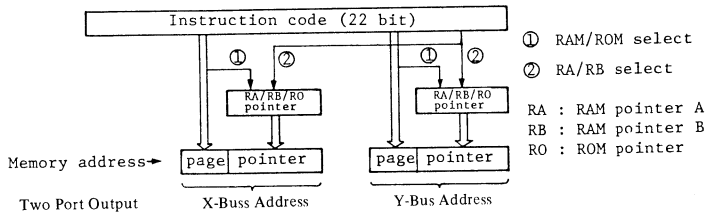
In this mode, the X-Bus output and Y-Bus output are as follows;
- The data RAM and data ROM are accessed.



- The data RAM/ROM and GR are accessed.

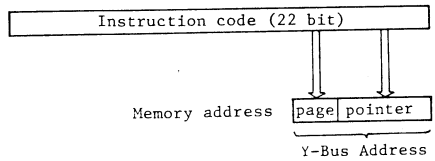
The pointer addressing mode is available for accessing two-word data during the product sum operation, reading data from sequential addresses, etc.

(2) Direct addressing mode
In direct addressing, nine bits of the instruction code specify data RAM/ROM address (page address and pointer address). The direct addressing mode is available for multiplying one-word data in the data ROM/RAM by data in an accumulator, or reading data from discrete addresses.



Pointer part is specified by ROM/RAM pointer indirectly.

(a) Pointer addressing mode



Memory address is specified directly.

(b) Direct addressing mode

MEMORY ADDRESSING MODE

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{cc}	−0.3 to 7.0	V	
Input Voltage	V_{in}	−0.3 to V_{cc} + 0 3	V	
Operating Temperature Range	T_{opr}	0 to +70	°C	
Storage Temperature Range	T_{stg}	−55 to +150	°C	DIC Package
		−55 to +125	°C	DIP, PLCC Package

■ **ELECTRICAL CHARACTERISTICS**

• **DC Characteristics** (V_{cc} = 5.0V ± 5%, Vss = 0V, Ta = −20 to +75°C unless otherwise specified.)

Item		Symbol	Test Condition	Min	Typ	Max	Unit
Input "High" Voltage	OSC,IE,SICK,SOCK	V_{IH}		2.4	-	V_{cc}+0.3	V
	All others			2.2	-	V_{cc}+0.3	V
Input "Low" Voltage	OSC,IE,SICK,SOCK	V_{IL}		-0.3	-	0.4	V
	All others			-0.3	-	0.8	V
Input Leak Current	$\overline{TEST}$,TxAK,IE,R/$\overline{W}$, $\overline{CS}$, F_0∿F_3,$\overline{DEND}$,SI SIEN,$\overline{SOCK}$,SOEN SICK,$\overline{RES}$,OSC	$\lvert I_{IN}\rvert$	V_{IN}=0.4 to 2.4V	-	-	10	μA
Three State Current (OFF State)	D_0∿D_{15}, SO	$\lvert I_{TSI}\rvert$	V_{IN}=0.4 to 2.4V	-	-	10	μA
Open Drain Current (OFF State)	TxRQ,BIT I/O	$\lvert I_{LOH}\rvert$	V_{IN}=0.4 to 2.4V	-	-	10	μA
Output "High" Voltage	D_0∿D_{15},SO,SYNC	V_{OH}	$-I_{OH}$=400μA	2.4	-	-	V
Output "Low" Voltage	All output pins	V_{OL}	I_{OL}=1.6 mA	-	-	0.8	V
Input Capacitance	All output pins	C_{IN}	V_{IN}=0V, f=1MHz T_a=25°C	-	-	12.5	pF
Current Dissipation		I_{CC}	Not port loading	-	50	100	mA

- **AC Characteristics**

System Clock (V_{cc}=5.0V±5%, V_{ss}=0V, T_a=−20 to +75°C unless otherwise specified.)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Clock (OSC) cycle	ϕ_{cyc}	Fig. 1	61.5	62.5	70.0	ns
Clock (OSC) Pulse Width	ϕ_{WH}		20	-	-	ns
	ϕ_{WL}		20	-	-	ns
Clock (OSC) Rise Time	ϕ_r		-	-	10	ns
Clock (OSC) Fall Time	ϕ_f		-	-	10	ns

Serial I/O Timing (V_{cc}=5.0V±5%, V_{ss}=0V, T_a=−20 to +75°C unless otherwise specified.)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Clock (SICK, SOCK) cycle	S_{cyc}	Fig. 2 Fig. 5	1.0	-	10.0	µs
Clock (SICK, SOCK) Pulse Width	S_{WH}		450	-	-	ns
	S_{WL}		450	-	-	ns
Clock (SICK, SOCK) Rise Time	S_r		-	-	25	ns
Clock (SICK, SOCK) Fall Time	S_f		-	-	25	ns
Serial Input Data Set-up Time	t_{SDS}		100	-	-	ns
Serial Input Data Hold Time	t_{SDH}		100	-	-	ns
Serial Output Data Delay Time	t_{SDD}		-	-	300	ns
Enable Delay Time	t_{ED}		50	-	-	ns
Enable Set-up Time	t_{ES}		100	-	-	ns

Parallel I/O (Bus Interface) Timing (V_{CC}=5.0V±5%, V_{SS}=0V, T_a=−20 to +75°C unless otherwise specified.)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
IE cycle	t_{cyc}	Fig. 3 Fig. 5	1.0	-	10.0	µs
IE Pulse Width	t_{WH}		450	-	-	ns
	t_{WL}		450	-	-	ns
IE Rise Time	t_r		-	-	25	ns
IE Fall Time	t_f		-	-	25	ns
$\overline{CS}$ Set-up Time	t_{CS}		140	-	-	ns
$\overline{CS}$ Hold Time	t_{CH}		10	-	-	ns
Address Set-up Time	t_{AC}		10	-	-	ns
Address Hold Time	t_{CA}		20	-	-	ns
Input Data Set-up Time	t_{DSW}		190	-	-	ns
Input Data Hold Time	t_{DHW}		10	-	-	ns
Output Data Delay Time	t_{DDR}		-	-	220	ns
Output Data Hold Time	t_{DHR}		10	-	-	ns

DMA Interface Timing (V_{CC}=5.0V±5%, V_{SS}=0V, T_a=−20 to +75°C unless otherwise specified.)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
TxAK Set-up Time	t_{AS}	Fig. 4 Fig. 5	140	-	-	ns
TxAK Hold Time	t_{AH}		-	-	600	ns
TxRQ Delay Time	t_{TR}		-	-	470	ns

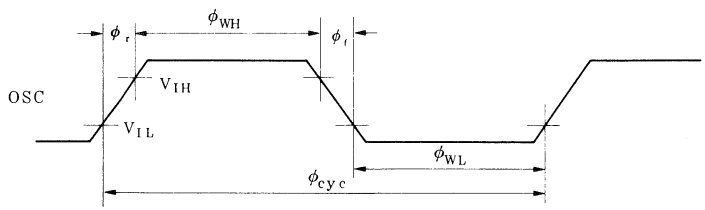
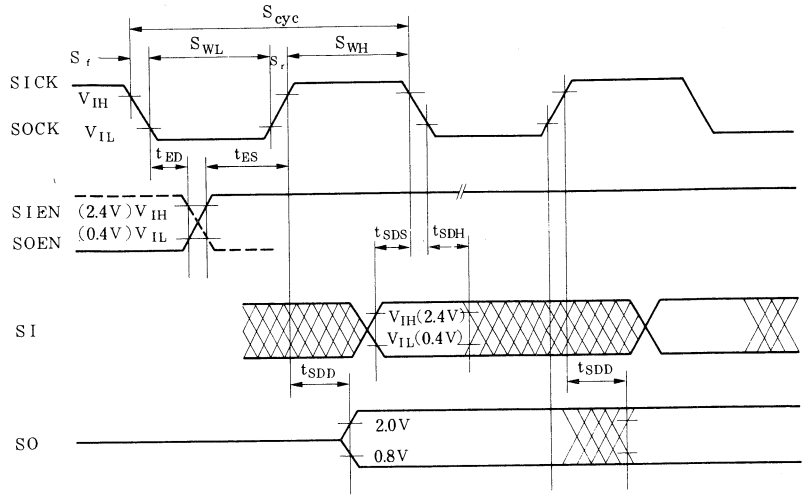
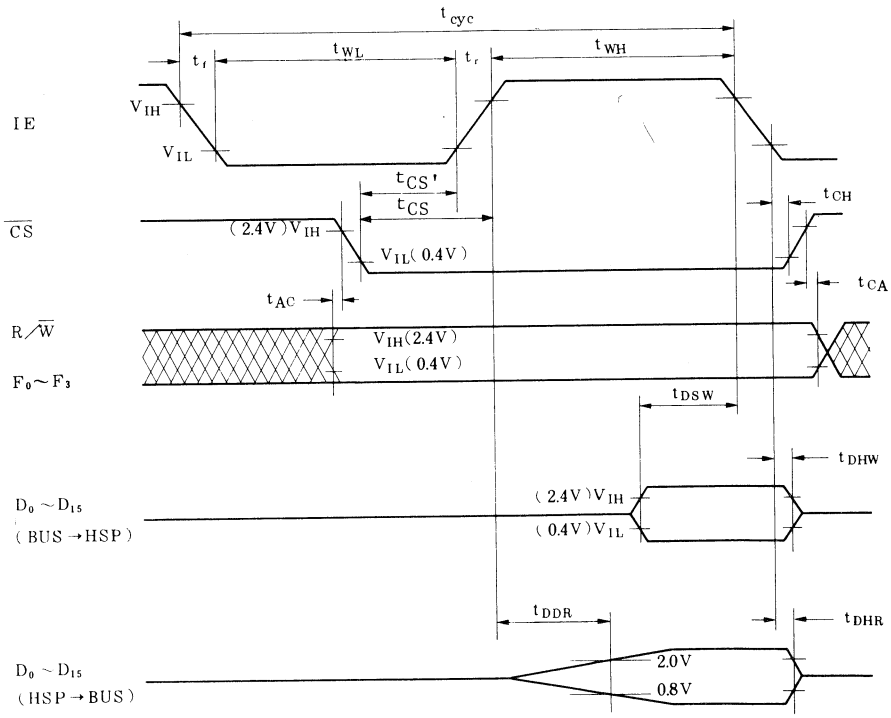


Fig. 1 SYSTEM CLOCK WAVEFORM



(Note) The SO pin goes to the high-impedence state by latching SOEN with SOCK.

Fig. 2 SERIAL I/O WAVEFORM



(Note 1) Keep t_{CS} (min. 140ns) with CTR/PC transfer instructions.

The data transfer instruction using the IR/OR takes t_{CS}'of more than 10 ns.

(Note 2) The data bus output in the byte transfer mode is 16 bit ($D_0 - D_{15}$). In this case, the upper half ($D_8 - D_{15}$) is not valid. Therefore, $D_8 - D_{15}$ should not be directly connected to V_{CC}/GND.

Fig. 3 PARALLEL I/O TIMING

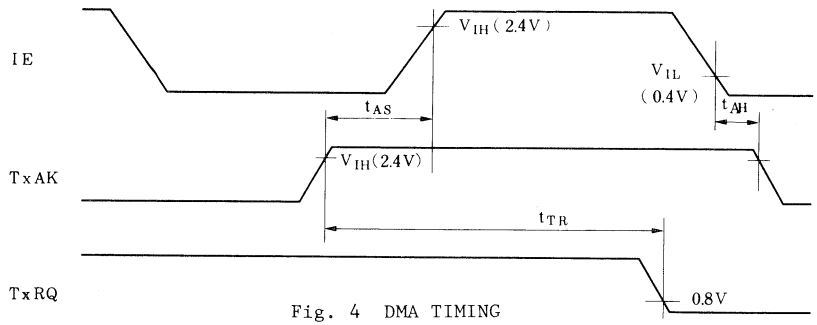
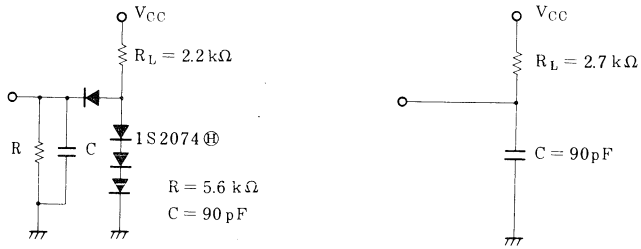


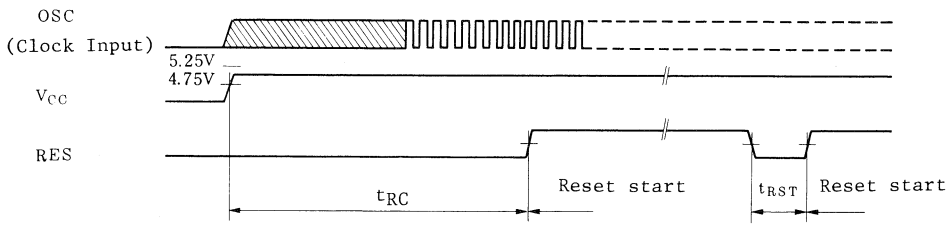
Fig. 4 DMA TIMING



Applicable terminal ($D_0 - D_{15}$, SO) Applicable terminal (TxRQ)

C : includes probe and jig capacitance

Fig. 5 LOAD CIRCUIT (FOR TIMING TEST)



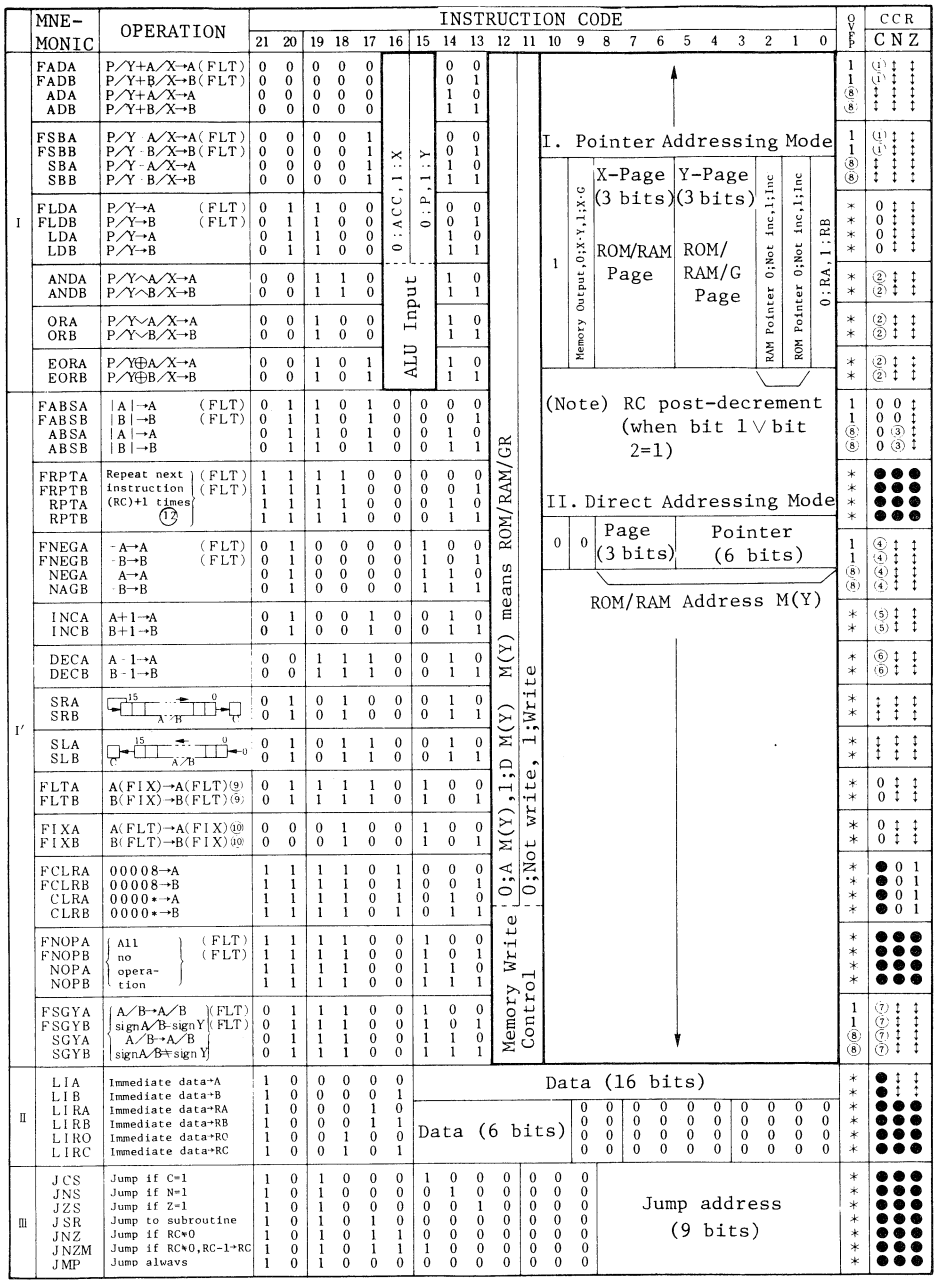
Power-ON reset t_{RC} = 20ms (min)

Reset during operation t_{RST} = 1μs (min)

(Note) Clock (16 MHz) should be input during t_{RST} or the power-ON rest start.

Fig. 6 **RESET TIMING**

■INSTRUCTION SET

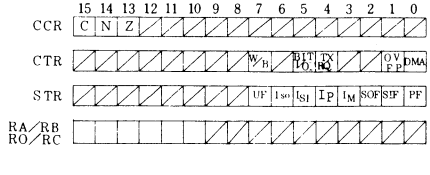


	OPERAND	OPERATION	INSTRUCTION CODE 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OVFP	CCR CNZ
IV (MNEMONIC : TFR)	A,STR	A→STR	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	B,STR	B→STR	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	A,CTR	A→CTR	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	B,CTR	B→CTR	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	A,RC	A→RC	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	B,RC	B→RC	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	A,OR	A→OR	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	B,OR	B→OR	1	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	A,RO	A→RO	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	B,RO	B→RO	1	1	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	A,RA	A→RA	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	B,RA	B→RA	1	1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	A,RB	A→RB	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	*	● ● ●
	B,RB	B→RB	1	1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	*	● ● ●
	A,CCR	A→CCR	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	—⑪—
	B,CCR	B→CCR	1	1	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	—⑪—
	A,SOR	A→SOR	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	B,SOR	B→SOR	1	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	STR,A	STR→A	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	STR,B	STR→B	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	CTR,A	CTR→A	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	CTR,B	CTR→B	1	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	RC,A	RC→A	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	RC,B	RC→B	1	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	IR,A	IR→A	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	IR,B	IR→B	1	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	RO,A	RO→A	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ 0
	RO,B	RO→B	1	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ 0
	RA,A	RA→A	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ 0
	RA,B	RA→B	1	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ 0
	RB,A	RB→A	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	*	● ↕ 0
	RB,B	RB→B	1	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	*	● ↕ 0
	CCR,A	CCR→A	1	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● 1 0
	CCR,B	CCR→B	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● 1 0
	SIR,A	SIR→A	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	SIR,B	SIR→B	1	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	A,B	A→B(FIX only)	1	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕
	B,A	B→A(FIX only)	1	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	● ↕ ↕

	MNEMONIC	OPERATION	INSTRUCTION CODE 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OVFP	CCR CNZ
V	INCRA	RA+1→RA	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	INCRB	RB+1→RB	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	*	● ● ●
	INCRO	RO+1→RO	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	DECRA	RA-1→RA	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	DECRB	RB-1→RB	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	*	● ● ●
	DECRO	RO-1→RO	1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	DECRC	RC-1→RC	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
VI	RTI	Return from interrupt	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●
	RTN	Return from subroutine	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	● ● ●

A: Accumulator A
B: Accumulator B
X: X-Bus memory output
Y: Y-Bus memory output
P: Multiplier output
G: General register
D: Delay register
PC: Program counter
RC: Repeat counter
RO: ROM pointer
RA: RAM pointer A
RB: RAM pointer B

IR: Input register
OR: Output register
SIR: Serial input register
SOR: Serial output register
CCR: Condition code register
STR: Status register
CTR: Control register
M(Y): Y-Bus output memory address
A/B (15∿10)↔RC/RO/RA/RB(5∿0)
A/B (15∿13)↔CCR(15∿13)
A/B (7 ∿ 0)↔STR/CTR(7∿0)



1 Generated by the mantissa parts of two inputs (after adjusting digit of mantissa
2 Undefined
3 1 when A/B=$8000 before execution and OVFP=0; otherwise 0.
4 1 when A/B=$0000 before execution; otherwise 0.
5 1 when A/B=$FFFF before execution; otherwise 0.
6 1 when A/B≠0000 before execution; otherwise 0.
7 1 when Sign A/B≠Sign Y and A/B=$0000; otherwise 0.
8 OVFP(CTR(1)) = 0: Not overflow protect
= 1: Overflow protect
9 Scaling with exponent of Y-Bus output.
10 Scaling with exponent of Y-Bus output: Mantissa is $000.
11 Depends on the 13∿15 bits of A/B.
12 Repeated (RC) times in the pointer address mode with RC decrement.

CCR Column
↕ 1; True, 0; False after execution/Change
● Not affected

OVFP Column
* Not affected by OVFP (CTR, bit 1)
1 OVFP should be set to 1 beforehand. Once set, OVFP does not change unless TFR instruction (A/B→CTR) is executed.

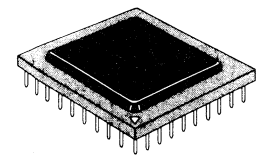
HD61811Y

High Performance Signal Processor (RAM Version)

The HSP-RAM (HD61811) is a high performance signal processor using RAM in place of ROM in the HSP (HD61810), which permits desired programs to be loaded by external control. In addition, as the HSP-RAM provides the same instruction set and functions as the HSP, it can be used for the HSP evaluation and low volume production.

For detail of the basic operation of the HSP-RAM, see the HSP user's manual. This data sheet concentrates on the differences from the HSP.

HD61811Y



(PC-68)

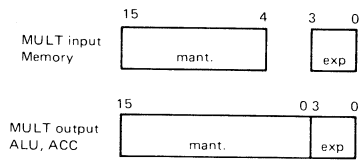
■ KEY FEATURES

- High-speed arithmetic operations (instruction cycle: 250 ns)
  Floating point arithmetic (realizes 32-bit dynamic range)
  Pipeline control
  Horizontal micro instructions
- Large capacity memories
  512 x 22-bit instruction RAM
  200 x 16-bit data RAM [1] (2-port accessible)
  128 x 16-bit data RAM [2]
- System bus compatible with 6800 family microcomputer through 8/16-bit parallel I/O ports
- Serial I/O interface for up to 16 bits
- Interrupt by three factors (end of three kinds of data I/O transfer: papallel I/O, serial input and serial output)
- Two nesting levels of subroutine and interrupt
- The store program is alterable.

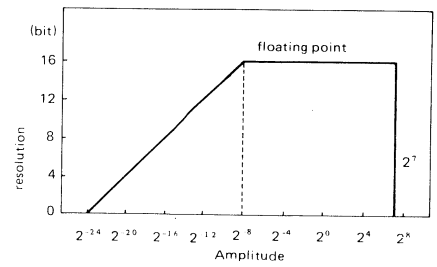
■ ARCHITECTURE

- **Floating Point Arithmetic**

The HD61811 can perform some kinds of floating point arithmetics (multiplication, addition and subtraction) in parallel in single instruction cycle (250 ns). Floating point arithmetic allows 32-bit dynamic range in spite of the 16-bit resolution.



Data format (floating point)



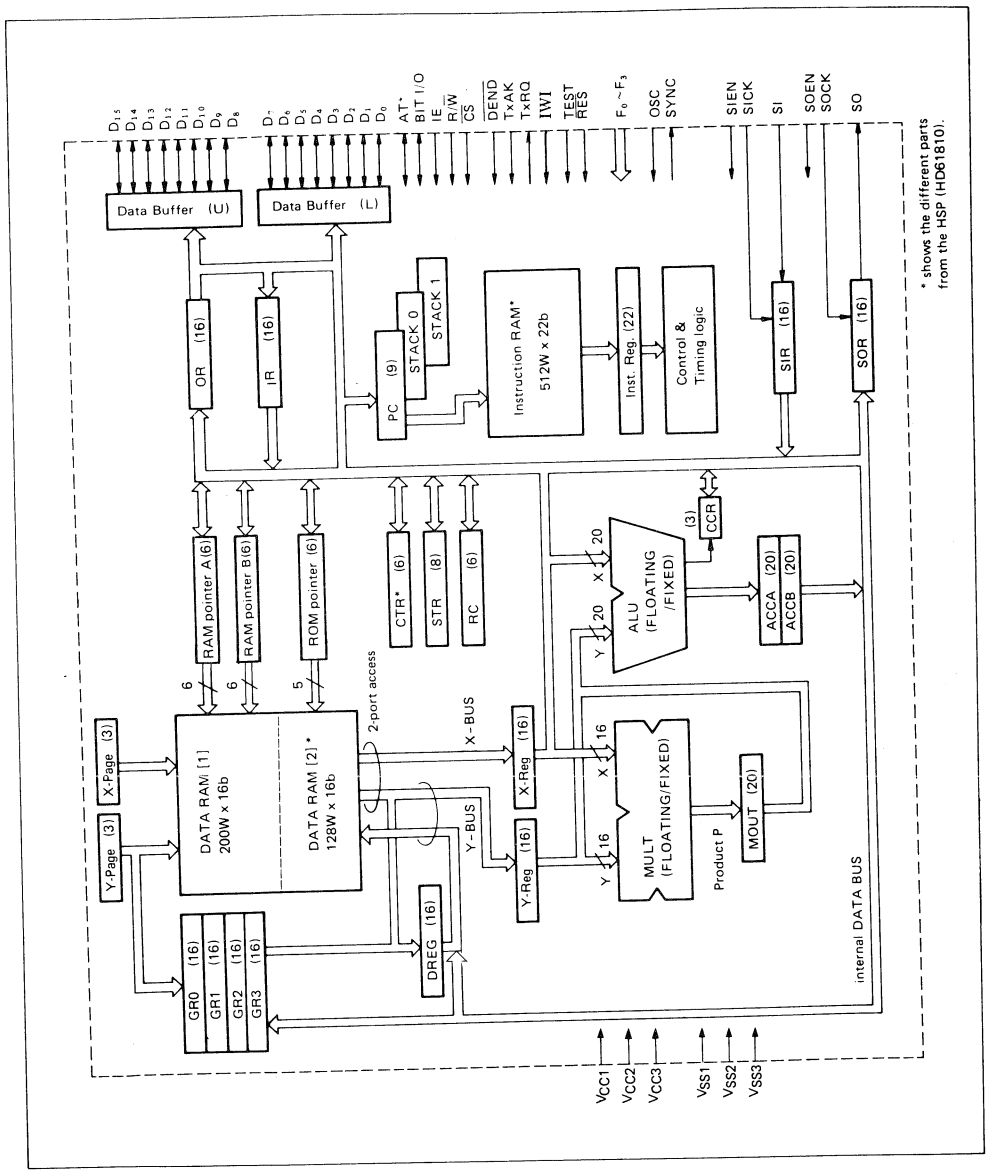


Fig. 1 HD61811 Block Diagram

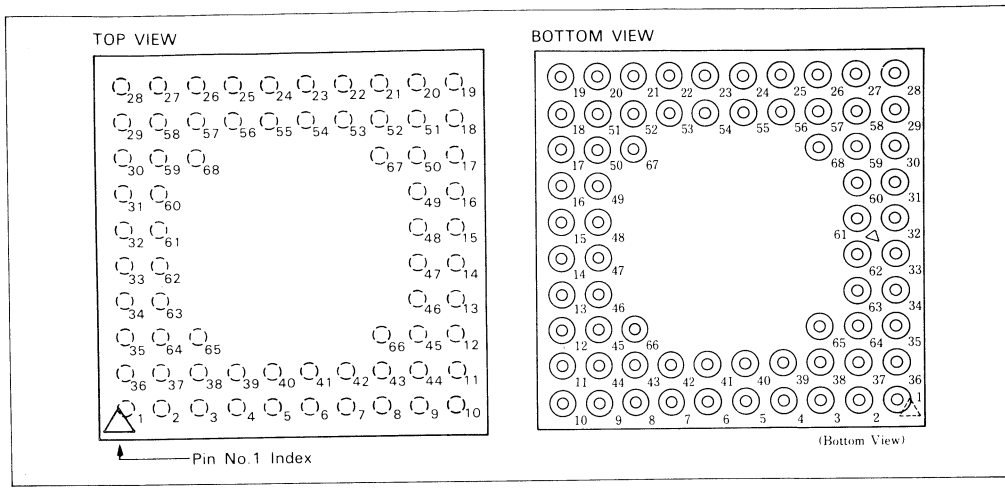


Fig. 2 HD61811 Pin Arrangement

Table 1 Functional Pin List

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	TEST	18	R/$\overline{W}$	35	$\overline{RES}$	52	F_1
2	D_{15}	19	(NC)	36	OSC	53	F_3
3	D_7	20	F_2	37	TxAK	54	(NC)
4	D_{14}	21	(NC)	38	(NC)	55	V_{CC2}
5	D_6	22	$\overline{DEND}$	39	(NC)	56	SIEN
6	(NC)	23	V_{SS2}	40	D_{13}	57	SI
7	(NC)	24	(NC)	41	(NC)	58	(NC)
8	D_5	25	(NC)	42	(NC)	59	SICK
9	D_{12}	26	(NC)	43	D_4	60	BIT I/O
10	(NC)	27	SOCK	44	D_{11}	61	AT
11	D_3	28	SOEN	45	D_{10}	62	V_{CC3}
12	D_2	29	TxRQ	46	D_9	63	SYNC
13	(NC)	30	V_{SS3}	47	V_{CC1}	64	V_{SS1}
14	(NC)	31	SO	48	D_8	65	(NC)
15	D_1	32	IWI	49	IE	66	(NC)
16	(NC)	33	(NC)	50	$\overline{CS}$	67	(NC)
17	D_0	34	(NC)	51	F_0	68	(NC)

(Note) V_{CC1}, V_{CC2} and V_{CC3} are connected in common. (pin voltage $V_{CC1}=V_{CC2}=V_{CC3}$)
V_{SS1}, V_{SS2} and V_{SS3} are connected in common. (pin voltage $V_{SS1}=V_{SS2}=V_{SS3}$)
IWI pin must be fixed to high level ("H").

■ DIFFERENCES BETWEEN THE HSP AND THE HSP-RAM

In the HSP-RAM (HD61811), RAM is used in place of ROM in the HSP (HD61810). The following table describes differences between the HSP and the HSP-RAM.

Table 2 The HSP and the HSP-RAM

	HSP (HD61810)	HSP-RAM (HD61811)
Instruction memory	Instruction ROM (512W x 22b)	Instruction RAM (512W x 22b)
Data memories	Data RAM (200W x 16b)	Data RAM [1] (200W x 16b)
	Data ROM (128W x 16b)	Data RAM [2] (128W x 16b)
Parallel I/O functions	Provides one mode only. (See 'I/O INTERFACE' in the HSP user's manual.)	Provides two modes. (Normal mode and test mode)
Control register	Consists of five bits. (W/B, BIT I/O, TxRQ, OVFP, DMA)	Adds AT bit (bit 6) to conventional bits.

■ INSTRUCTION RAM

The instruction RAM is organized as 512 words by 22-bit, which is the same capacity as the instruction ROM of the HSP. Locations $1E7 through $1FE can be used for user's program, though unusable in the HSP. Location $1FE (the last address) is a vector address for interrupt, so the user must store the jump instruction here for a jump to an interrupt service routine.

The contents of the instruction RAM are undefined at power-on. First of all, an auxiliary program must be written to the instruction RAM through external data bus ($D_0 \sim D_{15}$). This program execution permits working the HSP-RAM. For details, see 'HD61811 APPLICATION CIRCUIT'.

A 22-bit word data in this RAM is divided into two for transfer; the upper bits (U, 11 bits) and the lower bits (L, 11 bits). For details of data transfer to the instruction RAM, see 'READ AND WRITE TO THE INSTRUCTION RAM'.

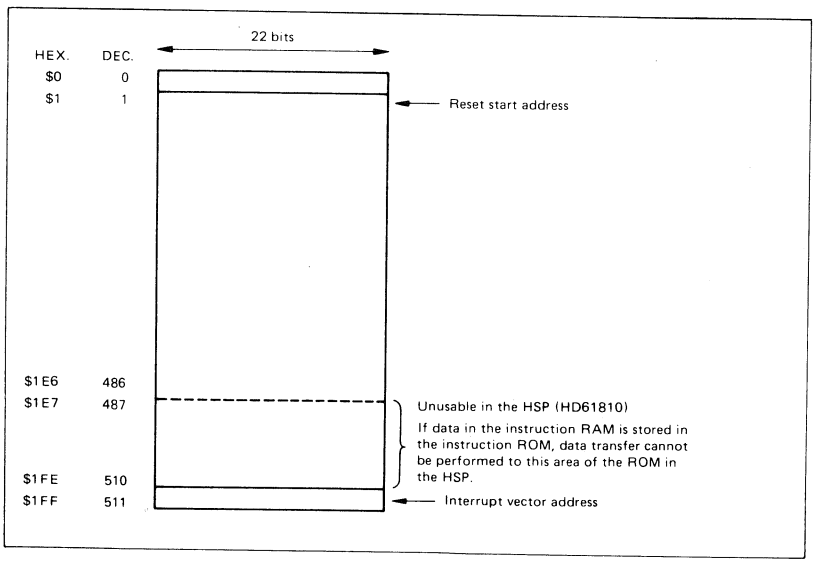


Fig. 3 Instruction RAM

■ DATA RAM

The HSP-RAM (HD61811) provides two data RAMs.

• Data RAM [1]

Data RAM [1] is organized as 200 words by 16 bits, corresponding to the data RAM in the HSP (HD61810).

• Data RAM [2]

Data RAM [2] is organized as 128 words by 16 bits, corresponding to the data ROM in the HSP.

A write to data RAM must be performed by software.

There are two modes of data memory addressing: pointer addressing and direct addressing. In pointer addressing mode, the RAM pointer A/B are used for the addressing of the data RAM [1] and the ROM pointer for the data RAM [2]. The address pointer for generating data 'RAM' [2] address is called the 'ROM' pointer in order to standardize the technical term between the HD61810 and the HD61811.

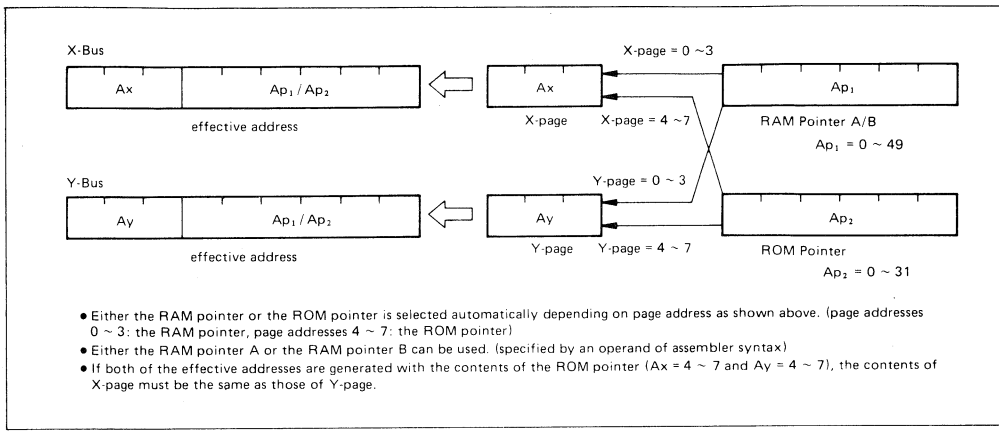


Fig. 4 Generation of Effective Address Using Address Pointers

■ CONTROL REGISTER (CTR)

In the HSP-RAM (HD61811), the control register consists of 6 bits, adding an I/O bit (AT) to the CTR bits in the HSP (HD61810). At has the same function as BIT I/O.

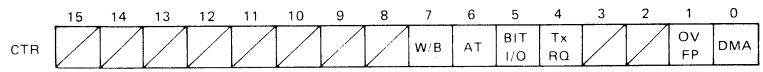


Table 3 Functions of the CTR

Bit	Name	Functions	Description
0	DMA	Parallel I/O Data Transfer Mode Select bit	• Selection of the mode for data transfer through the parallel I/O ports. 1: DMA operation mode 0: Non-DMA operation mode This bit must be cleared during an usual data transfer. Even in the DMA operation mode data is transferred through parallel I/O ports by software.
1	OVFP	Overflow Protection bit	• Protection against overflows. If an overflow occurs during an ALU operation, the result is fixed to the maximum value. 1: Performing a protection against overflow. 0: Not performing a protection against overflow.
4	TxRQ	DMA Operation Request bit	• Request for DMA operation. This bit is set to request a DMA operation in the DMA operation mode. The TxAK input clears this bit and then it is set automatically. However after the $\overline{\text{DEND}}$ input, this bit remains clear. In the non-DMA operation mode, the TxRQ can be used as a programmable output.
5	BIT I/O	Bit I/O bit	• Input and output of one bit. This bit controls an input/output of Bit I/O pin. When using Bit I/O pin as an output an user must write data directly to this register. When using the bit as an input, the user must write a 1 to this register and then read the register.
6	AT	AT bit	• Input and output of one bit. This bit functions in the same way as BIT I/O bit does. In the HSP (HD61810) AT is not used and a zero must be written into this bit by software.
7	W/B	Word/Byte bit	• Selection of the size of the data transferred through parallel I/O ports. 1: Word (16-bit) data is used. 0: Byte (8-bit) data is used.

■ PARALLEL I/O FUNCTIONS

The HSP-RAM has more parallel I/O functions than the HSP does. The parallel data is transferred between the HSP-RAM and external device through parallel I/O ports (D_0 through D_{15}). The parallel data transfer is controlled by the function control pins F_0 through F_3.

The HSP-RAM provides two parallel data transfer modes: normal mode and test mode. If TEST pin is set to high, the HSP-RAM enters test mode. This mode permits a read from the status register and a read or write to the instruction RAM.

The HD61811 provides the following parallel I/O functions.

(1) Data transfer

Data is transferred between the IR/OR and data buses (D_0 through D_{15}). In normal mode the HSP-RAM is active, and in test mode it is halted.

(a) Word (16-bit) data transfer ($D_0 \sim D_{15} \longleftrightarrow$ IR/OR)
16-bit data is transferred in parallel between the I/O pins (D_0 through D_{15}) and the IR/OR.

(b) Byte (8-bit) data transfer ($D_0 \sim D_7 \longleftrightarrow$ IR/OR)
A word data (16 bits) is divided into two for transfer; the high-order byte (bit 8 through bit 15) and low-order byte (bit 0 through bit 7). A byte data is transferred in parallel between the I/O pins (D_0 through D_7) and the IR/OR.

In parallel I/O functions other than data transfer, data is always transferred on a word basis.

(2) PC/CTR data transfer

in normal mode: $D_0 \sim D_7 \rightarrow$ PC/CTR

in test mode: $D_0 \sim D_7 \longleftrightarrow$ CTR, $D_0 \sim D_8 \longleftrightarrow$ PC

The contents of the PC/CTR can be changed externally. This function can be used to resume the HSP-RAM program from the optional address. In normal mode the PC can specify locations 0 through 255 and in test mode locations 0 through 511. The start address is (PC)+1.

In normal mode the PC/CTR is written only, while in test mode an MPU read or write can be performed to the PC/CTR.

In addition to the above, test mode permits the following parallel I/O functions.

(3) STR data transfer ($D_0 \sim D_7 \rightarrow$ STR)
An MPU read can be performed to the status register (STR), which permits an information of the HSP-RAM internal state to be given.

(4) Instruction transfer ($D_0 \sim D_{10} \longleftrightarrow$ Inst. Reg. 0 ~ 10/Inst. Reg. 11 ~ 21)
Data is transferred between the external device and the instruction RAM through the instruction register. As an instruction code consists of 22 bits, transfer data is divided into two: low-order bits data and high-order bits data.
Instruction transfer alone cannot read the instruction RAM. For details of data transfer of the instruction RAM, see 'READ AND WRITE TO THE INSTRUCTION RAM'.

Table 4 lists parallel I/O functions of the HSP-RAM.

Parallel I/O timing is shown in Fig. 5.

The HSP and the HSP-RAM work with the HMCS6800 bus timing. While $\overline{CS}$ is low, these LSIs select parallel I/O function depending on the level of F_0 through F_3, so $\overline{CS}$ should not become to low unnecessarily, as at time when address transient.

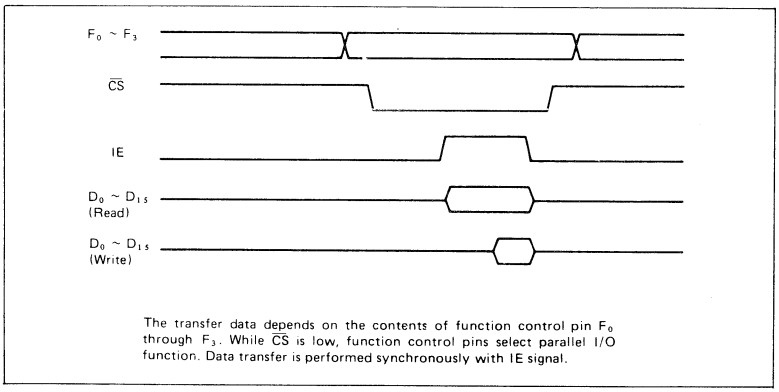


Fig. 5 Parallel I/O Bus Timing

In TEST RUN mode, IE signal timing is designed differently from the above one. For details, see 'TEST RUN OPERATION'.

Table 4 Parallel I/O Function

Control					Function	Normal mode (TEST=0)			Test mode (TEST=1)		
Chip Select	Function Control					Operation	HSP Operation	Interrupt	Operation	HSP Operation	Interrupt
$\overline{CS}$	F_3	F_2	F_1	F_0							
1	*	*	*	*	Run (normal)/ halt (test)	Run (execute internal program) No I/O operation (Note 1)	Active	—	Halt (stop the program run) No I/O operation (Note 2)	Halt	—
0	0	0	0	0	Run (normal)/ test run (test)	Run (execute internal program) No I/O operation (note 2)	Active	—	Test run No I/O operation	(Note 3)	—
	0	0	1	0	Data transfer (lower)	Data transfer (CTR (W/B)=0) • low-order byte Read: $D_{0\sim7} \leftarrow OR_{0\sim7}$ Write: $D_{0\sim7} \rightarrow IR_{0\sim7}$	Active	No interrupt	Data transfer The same operations as in normal mode	Halt	—
	0	0	1	1	Data transfer (upper)	Data transfer (1) Byte transfer mode (CTR (W/B) = 0) • high-order byte Read: $D_{0\sim7} \leftarrow OR_{8\sim15}$ Write: $D_{0\sim7} \rightarrow IR_{8\sim15}$ (2) Word transfer mode (CTR (W/B)=1) • word (16 bits) Read: $D_{0\sim15} \leftarrow OR_{0\sim15}$ Write: $D_{0\sim15} \rightarrow IR_{0\sim15}$	Active	Interrupt occurs	Data transfer The same operations as in normal mode	Halt	—
	0	1	0	0	CTR data transfer	CTR data transfer • Write: $D_{0\sim7} \rightarrow CTR_{0\sim7}$	Halt	—	CTR data transfer • Read: $D_{0\sim7} \leftarrow CTR_{0\sim7}$ • Write: $D_{0\sim7} \rightarrow CTR_{0\sim7}$	Halt	—
	0	1	1	0	STR data transfer		—	—	STR data transfer • Read: $D_{0\sim7} \leftarrow STR_{0\sim7}$	Halt	—

Control					Function	Normal mode (TEST=0)			Test mode (TEST=1)		
Chip Select	Function Control					Operation	HSP Operation	Interrupt	Operation	HSP Operation	Interrupt
$\overline{CS}$	F_3	F_2	F_1	F_0							
0	1	0	0	0	PC data transfer	PC data transfer • Write: $D_{0\sim7} \rightarrow PC_{0\sim7}$ • The value of PC should be in the range of 0 through 255. (D_{10}=1, D_9=0, D_8=0) • The interrupt mask bit I_M (in the STR) is set. The contents of other registers may be changed. The contents of RAM remain unchanged.	Halt	—	PC data transfer • Read: $D_{0\sim8} \leftarrow PC_{0\sim8}$ • Write: $D_{0\sim8} \rightarrow PC_{0\sim8}$ • The value of the PC should be in the range of 0 through 511. (D_9=D_{10}=0) • The interrupt mask bit I_M (in the STR) is set. The contents of data RAM and other registers may be changed, but they remain unchanged while the HSP-RAM is placed in the halt state.	Halt	—
	1	1	0	0	Instruction transfer (lower)		—	—	Instruction transfer (lower) • Read: $D_{0\sim10} \leftarrow$ Inst. Reg. $_{0\sim10}$ • Write: $D_{0\sim10} \rightarrow$ Inst. Reg. $_{0\sim10}$ $\rightarrow$ Inst. RAM $_{0\sim10}$ • Data is written to the instruction RAM address specified by the PC through parallel I/O data bus, however, external devices cannot read the instruction RAM.	Halt	—
	1	1	0	1	Instruction transfer (upper)		—	—	Instruction transfer (upper) • Read: $D_{0\sim10} \leftarrow$ Inst. Reg. $_{11\sim21}$ • Write: $D_{0\sim10} \rightarrow$ Inst. Reg. $_{11\sim21}$ $\rightarrow$ Inst. RAM $_{11\sim21}$	Halt	—

(Note 1) In DMA operation mode, I/O operation is performed.
(Note 2) D_0 to D_{15} output data if R/$\overline{W}$=1.
(Note 3) The state of the HSP-RAM depends on IE.
(IE=0: halt, IE=1: test run operation). During test run operation the data on internal data bus are latched to the OR automatically every instruction cycle. For details, see 'TEST RUN OPERATION'.

■ HALT

The internal data bus is used for the HSP-RAM internal operation. Therefore while using this data bus for the parallel data transfer between the HSP-RAM and an external device (PC/CTR data transfer), the HSP-RAM must be halted.

During transfer of the PC or CTR contents, the HD61811 enters the halt state, and after the end of the transfer, the HSP-RAM leaves the halt state and resumes processing of the program.

Data transfer between the IR/OR and the MPU is performed without using internal data bus, so the HSP-RAM does not enter the halt state.

In test mode, the HSP-RAM is always placed in the halt state except while test run operation is performed.

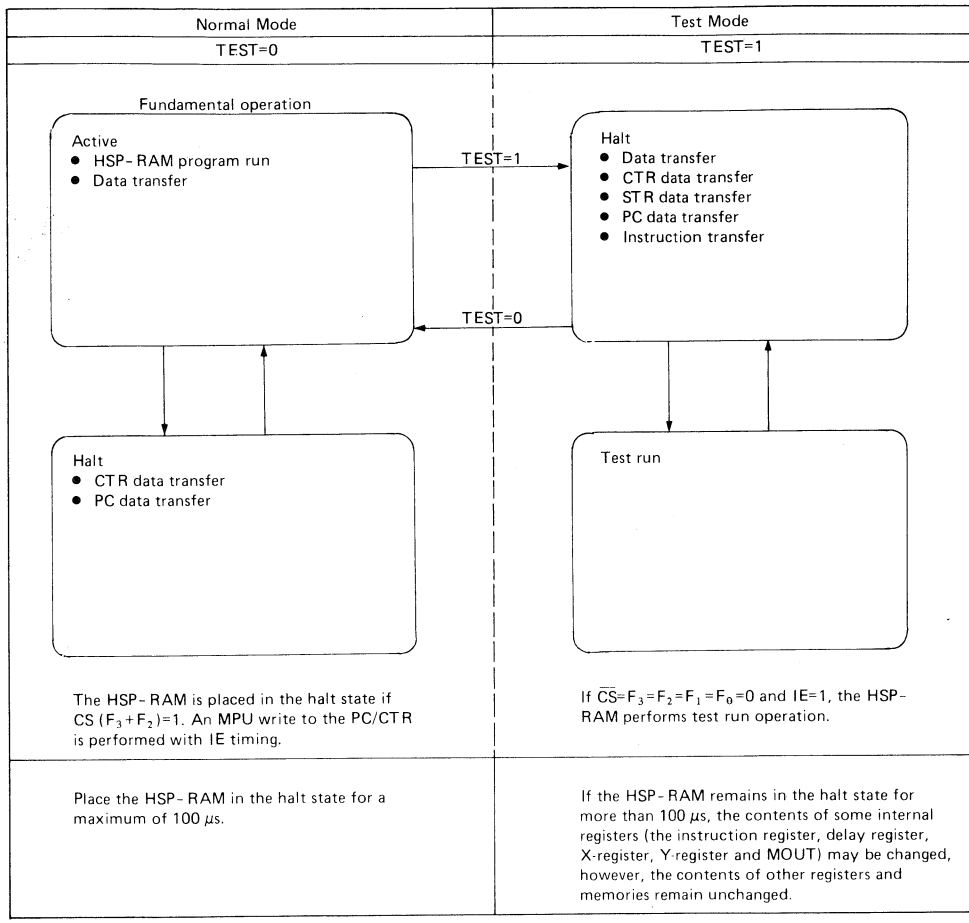


Fig. 6 HD61811 Operating Modes

■ TRANSITION BETWEEN ACTIVE/HALT STATE IN NORMAL MODE

Fig. 7 and 8 show bus timing of PC/CTR data transfer.

○ CTR Data Transfer

An MPU write is performed to the CTR through parallel I/O ports while the HSP-RAM is in the halt state, however, the contents of other registers remain unchanged.

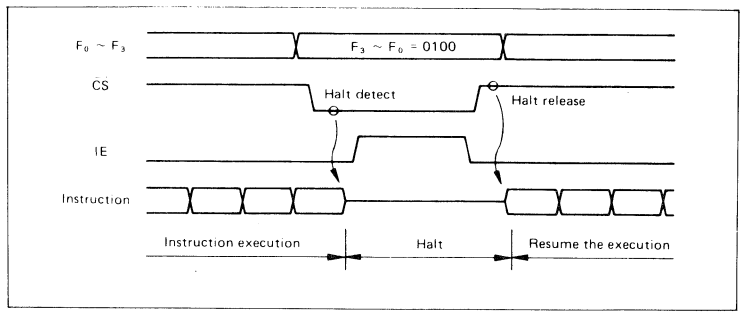


Fig. 7 CTR Data Transfer

○ PC Data Transfer

An MPU write is performed to the PC through parallel I/O ports while the HSP-RAM is in the halt state. When $\overline{CS}$ is set to high, the program routine is resumed. In this case, however, the instruction in the address specified by the PC is not executed and this instruction cycle is a dummy. The instruction execution starts from the next address. In a dummy cycle, the contents of some internal registers (the accumulator, RAM pointer A/B, ROM pointer and repeat counter) may be changed. The contents of memories remain unchanged.

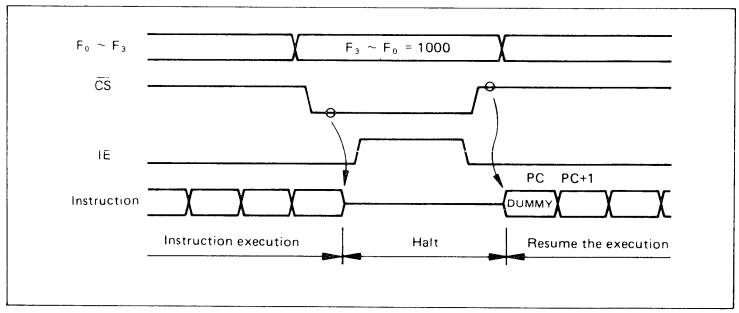


Fig. 8 PC Data Transfer

If IE does not become active during $\overline{CS}$ is low, data is not transferred to the PC/CTR and the HSP-RAM program routine is resumed.

■ PROCESSING AFTER PC DATA TRANSFER IN TEST MODE

In test mode, when data is transferred to the program counter through parallel I/O ports (D_0 through D_{15}), the contents of the instruction register may be changed, which may cause the contents of registers or RAM to be changed.

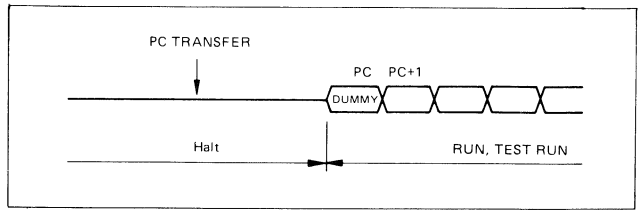


Fig. 9 After PC Data Transfer the Contents of Registers or RAM may be Changed.

In order not to change the contents of the registers and RAM, write a proper instruction to the instruction register after PC data transfer. (ex. NOP EE, etc.) After the HSP-RAM leaves the halt state, this instruction is executed in the first place.

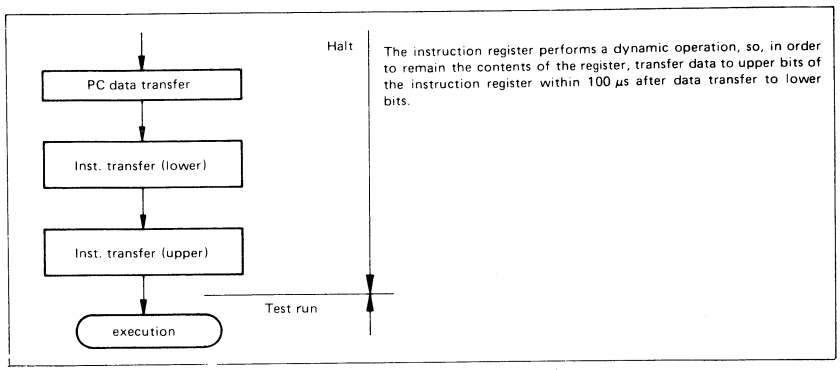


Fig. 10 Processing After PC Data Transfer

Instruction transfer function causes a write to the instruction RAM as well as a write to the instruction register. In this case, in order not to change the contents of the instruction RAM, the instruction code in the RAM must be written to the RAM again, which allows the HD61811 to operate as if the program is re-started from the memory location specified by the PC.

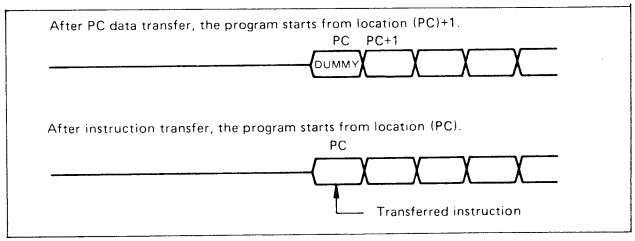


Fig. 11 Starting Address

■ READ AND WRITE TO THE INSTRUCTION RAM

An MPU read or write to the instruction RAM is performed with some parallel I/O functions.

Data is transferred between the MPU and instruction RAM through the instruction register using parallel I/O ports.

Fig. 12 shows data transfer to and from the instruction RAM.

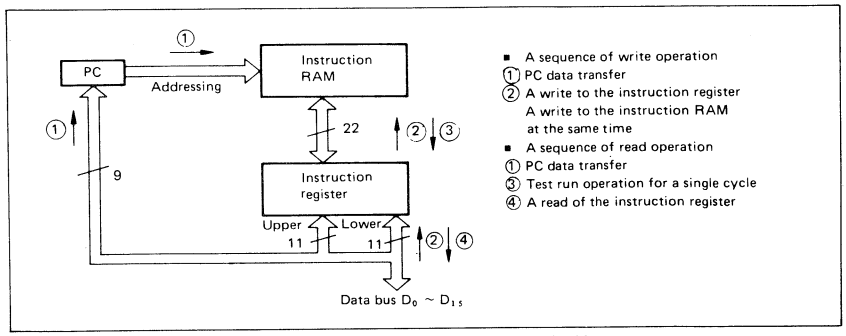


Fig. 12 Input/Output of the Instruction RAM

Parallel I/O lines (D_0 through D_{15}) are connected to the program counter, and to the instruction register. Data transfer of the instruction register is performed through these lines on 11-bit basis. (22-bit data of the instruction register is divided into two: 11 low-order bits and 11 high-order bits). So, special attention is needed in interfacing with an 8-bit microcomputer.

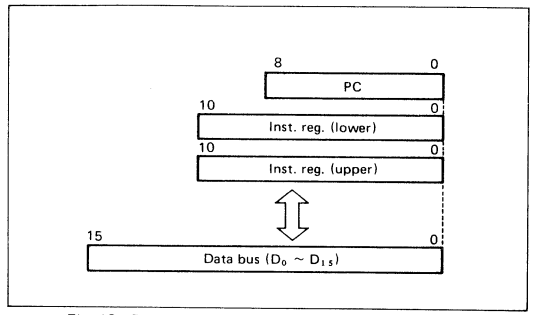


Fig. 13 Data between Data Bus and Internal Registers

A flowchart of an MPU read or write to the instruction RAM is shown in Fig. 14 and 15 respectively.

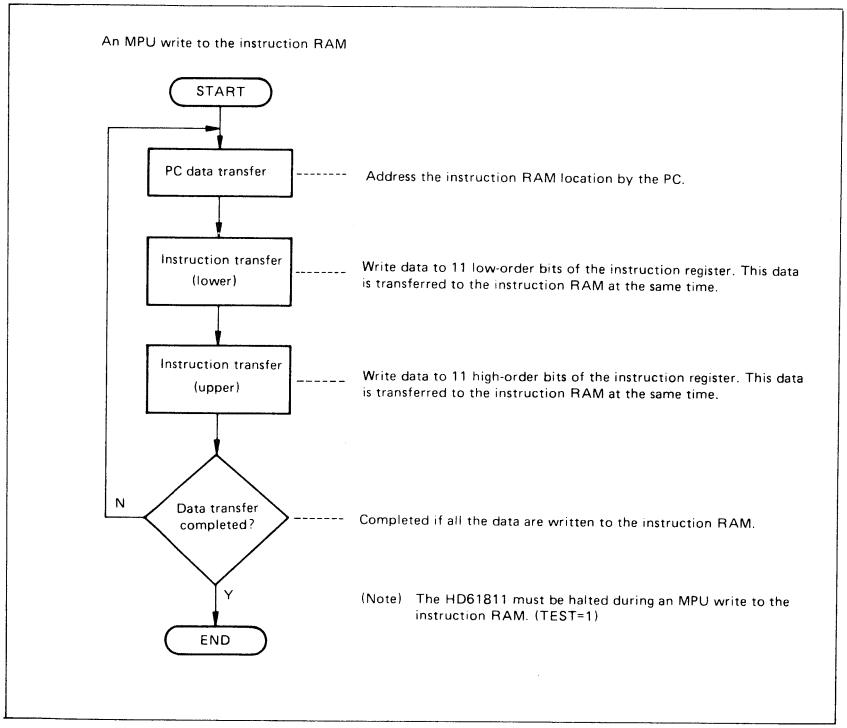


Fig. 14 A Flowchart of an MPU Write to the Instruction RAM

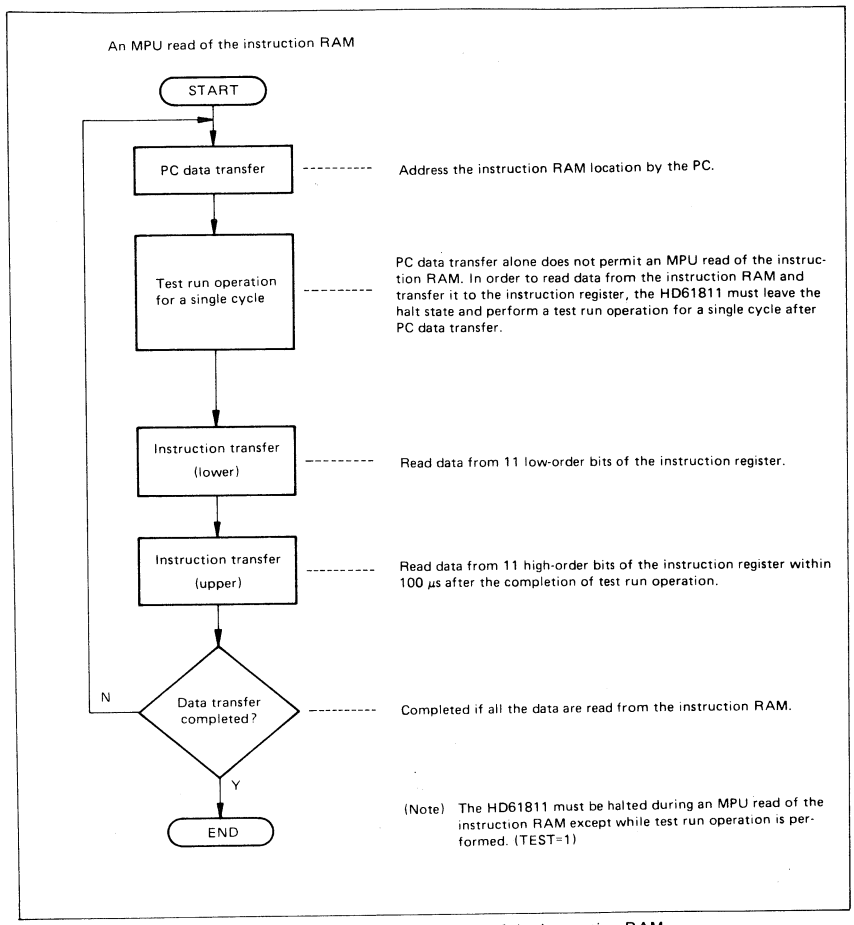


Fig. 15 A Flowchart of an MPU Read of the Instruction RAM

■ READ AND WRITE TO DATA RAM

An MPU read or write cannot be performed to data RAM through parallel I/O ports. Data is transferred to and from data RAM by software while the HD61811 runs the program. In order to perform these operations, a dedicated program should be written into the instruction RAM before PC data transfer.

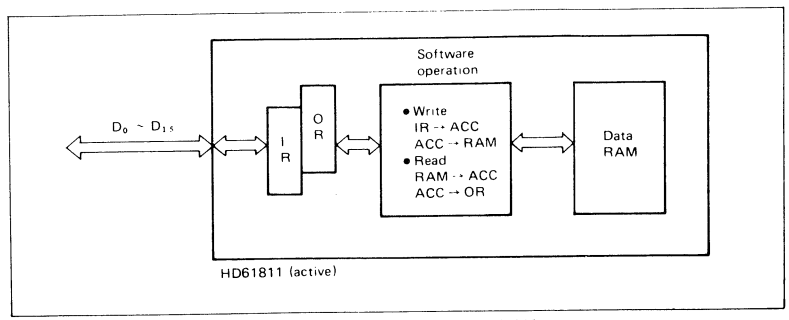


Fig. 16 Read and Write to Data RAM

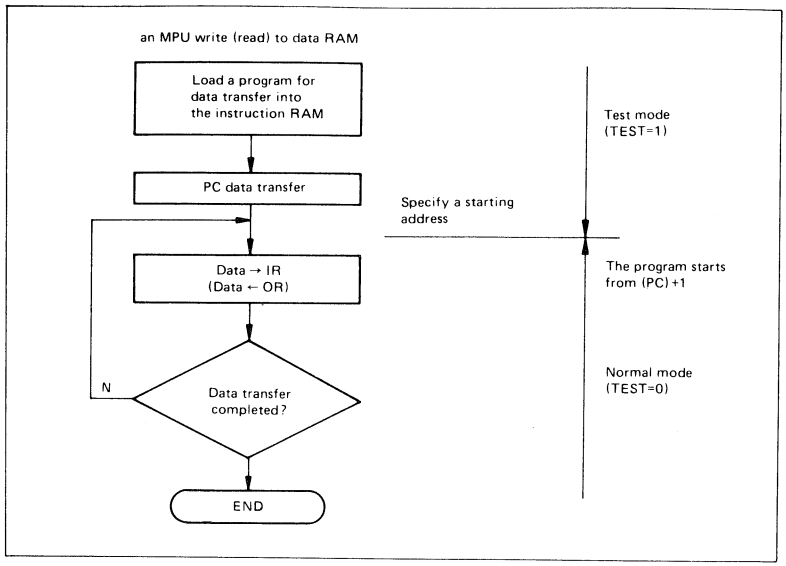


Fig. 17 A Flowchart of Data Transfer to Data RAM

■ TEST RUN OPERATION

While the HD61811 is in test mode, the HSP-RAM can perform a test run operation for any given cycles clocked by IE signal synchronously with SYNC output signal. Test run operation permits the HD61811 to be checked every step.

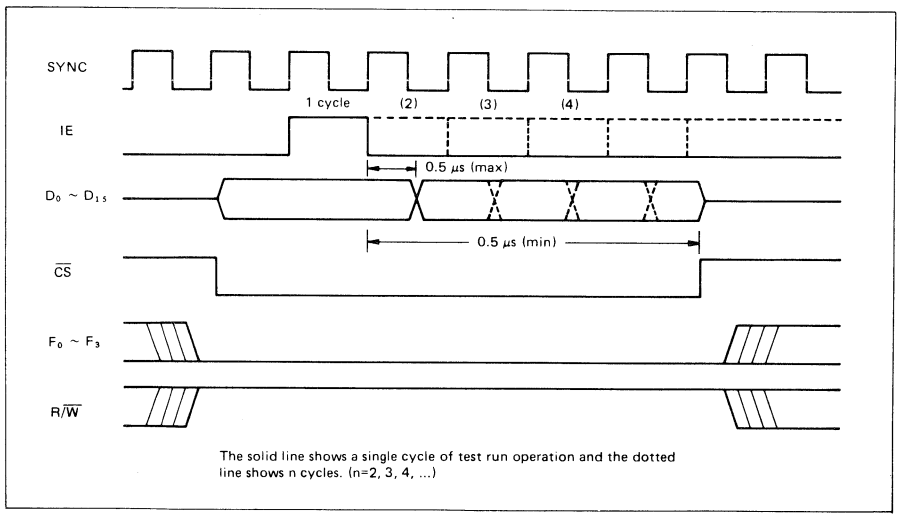


Fig. 18 Bus Timing of Test Run Operation

The data on internal data bus are latched to the OR automatically during test run operation. If R/$\overline{W}$=1, these data can be found on external data bus (D_0 through D_{15}). At the completion of test run operation (0.5 μs after IE=0) data can be read from data bus, however, an MPU read should be performed to the OR using data transfer function through parallel I/O ports.

In test mode, the HD61811 is halted except during test run operation, however, the HSP-RAM must not remain in the halt state for more than 100 μs in order not to change the contents of internal registers.

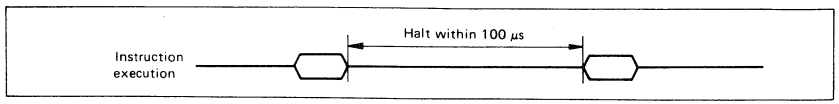


Fig. 19 Test Run Operation

■ THE HD61811 OPERATION MODES

The mode of the HD61811 depends on the level of TEST pin.

TEST=0 (low level): Normal mode
TEST=1 (high level): Test mode

The following attentions are needed in transition between normal mode and test mode.

● TEST=0 → TEST=1 (Normal mode → Test mode)

When the HD61811 enters test mode and is placed in the halt state, an instruction may not be executed. Set TEST pin to high after execution of the instruction which does not affect the HSP-RAM internal state.

Example: LBL JMP LBL

However, if the internal state permits changed, as after power-on, these operations need not be performed.

● TEST=1 → TEST=0 (Test mode → Normal mode)

The HD61811 enters normal mode in optional timing, leaving the halt state, however, TEST pin does not go to low during test run operation (IE=1).

■ HD61811 APPLICATION CIRCUIT

Fig. 22 gives an example of the system consisting of the MPU (HD6809E), the HSP-RAM (HD61811) and memory.

Fig. 23 shows an initial procedure of the HSP-RAM in the application circuit. In this procedure an initial load is performed to RAM in the HD61811 for compatibility with the HD61810. An execution of initial small program transfers data from the EPROM to the instruction RAM and data RAM [2]. For details of data on the EPROM, see Appendix 6 'EPROM DATA FORMAT'.

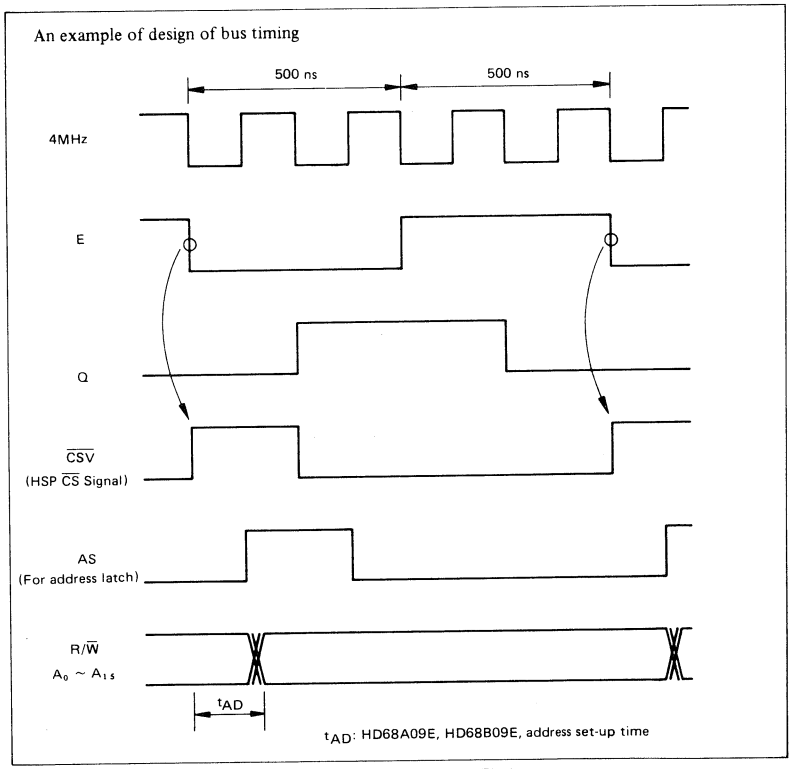
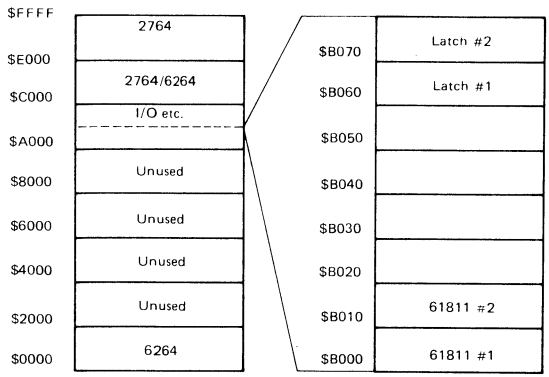


Fig. 20 HD6809E MPU Bus Timing

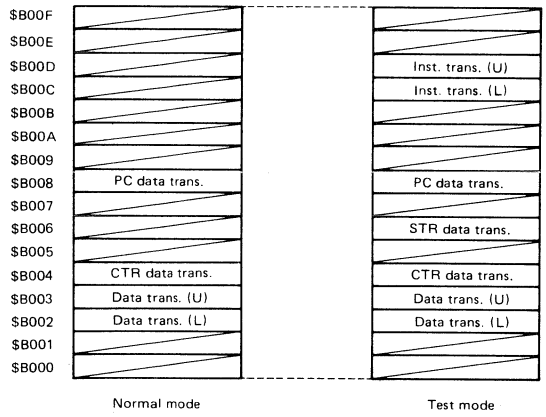
● Address Map

The following memory locations of microcomputer are reserved for the HD61811 in the application circuit. The memory location is addressed by function control pins.



(a) HD6809E Address Map

- The mode of the HD61811 depends on data in Latch #2 (locations $B070 through $B07F) and Latch #1 (locations $B060 through $B06F) is used for an output latch of data in high-order bits (D_8 through D_{15}).
- As the HD6809E is an 8-bit microcomputer, 16-bit transfer data to the HSP-RAM must be divided into two: data of high-order bits is saved into locations Latch #1, and then lower data and upper data are transferred to data bus (D_0 through D_{15}) at the same time.
- The state of TEST pin depends on data in the address of Latch #2 connected to D_0.



(b) Address Map of the HD61811

- In this application circuit, data is read from low-order bits of each register to data bus (D_0 through D_7), and the HD61811 cannot perform a test run operation because there is no bus timing designed for that operation.
- Fig. 21(b) shows an address map of 61811 #1, which has the same configuration as that of 61811 #2 ($B010 through $B01F).

Fig. 21 An Address Map in the Application Circuit

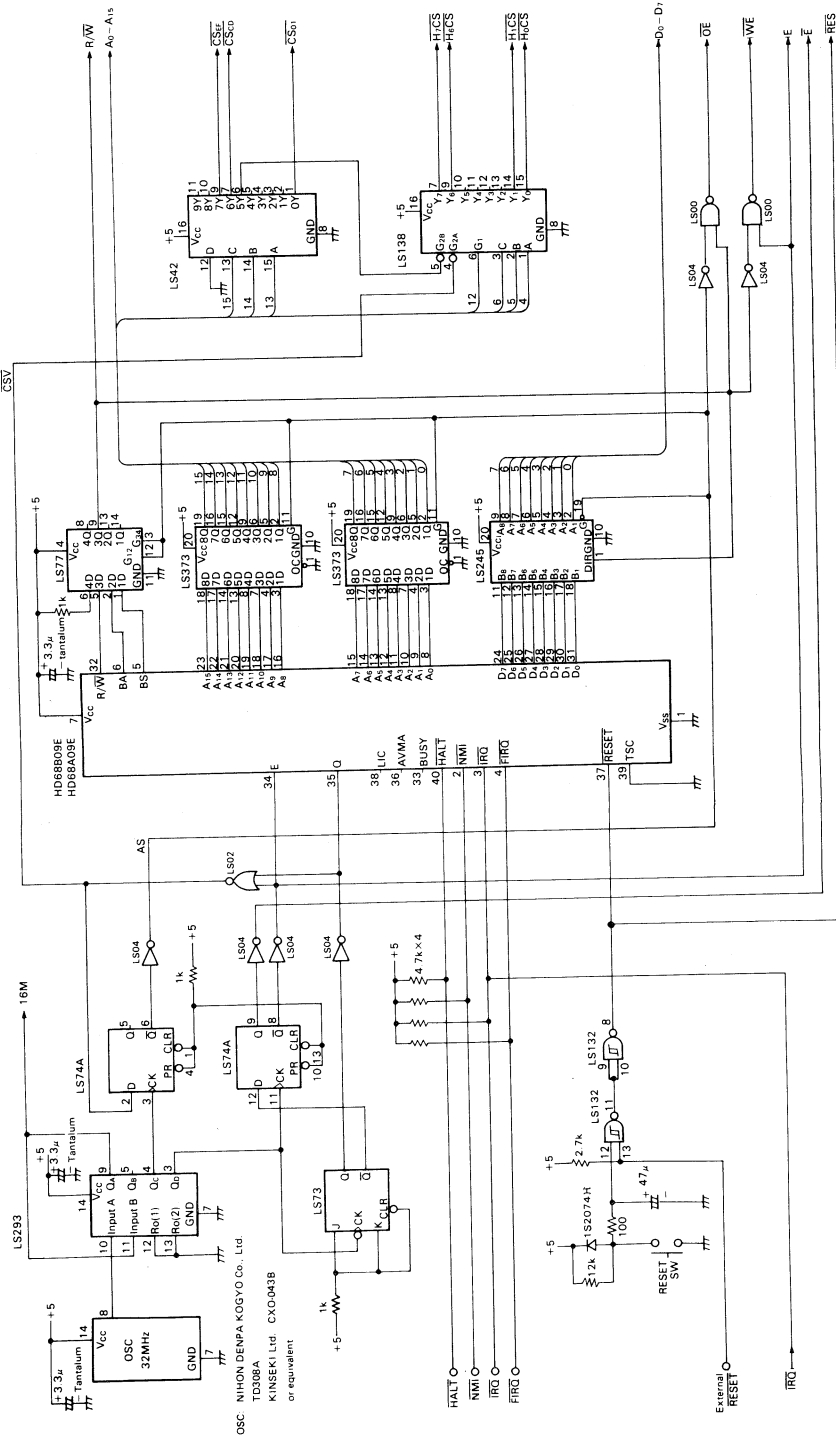


Fig. 22 Application Circuit Diagram

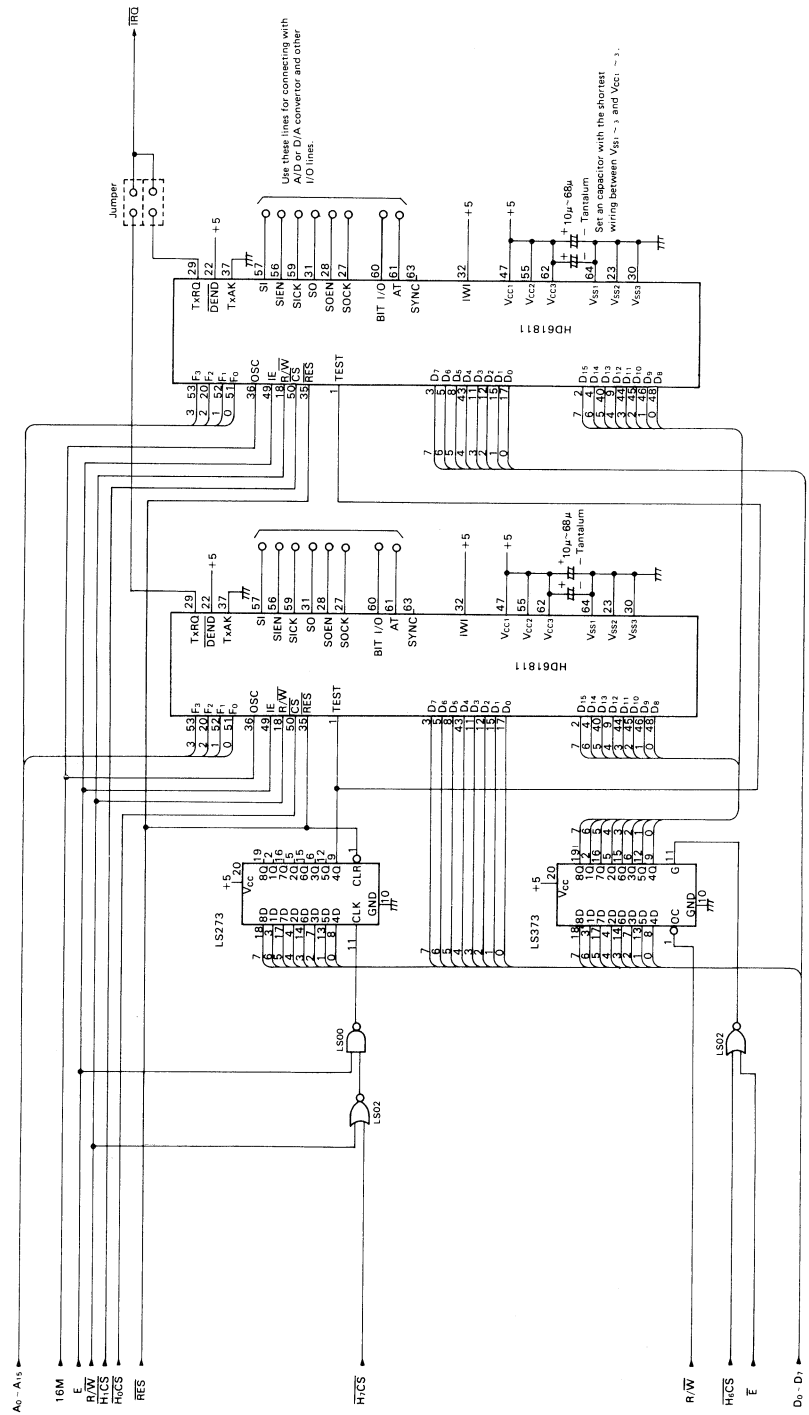


Fig. 22 Application Circuit Diagram (Cont'd)

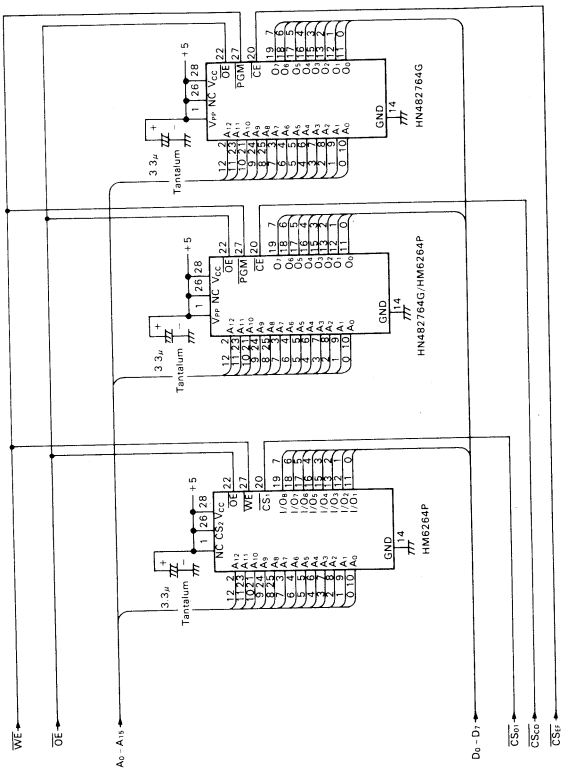
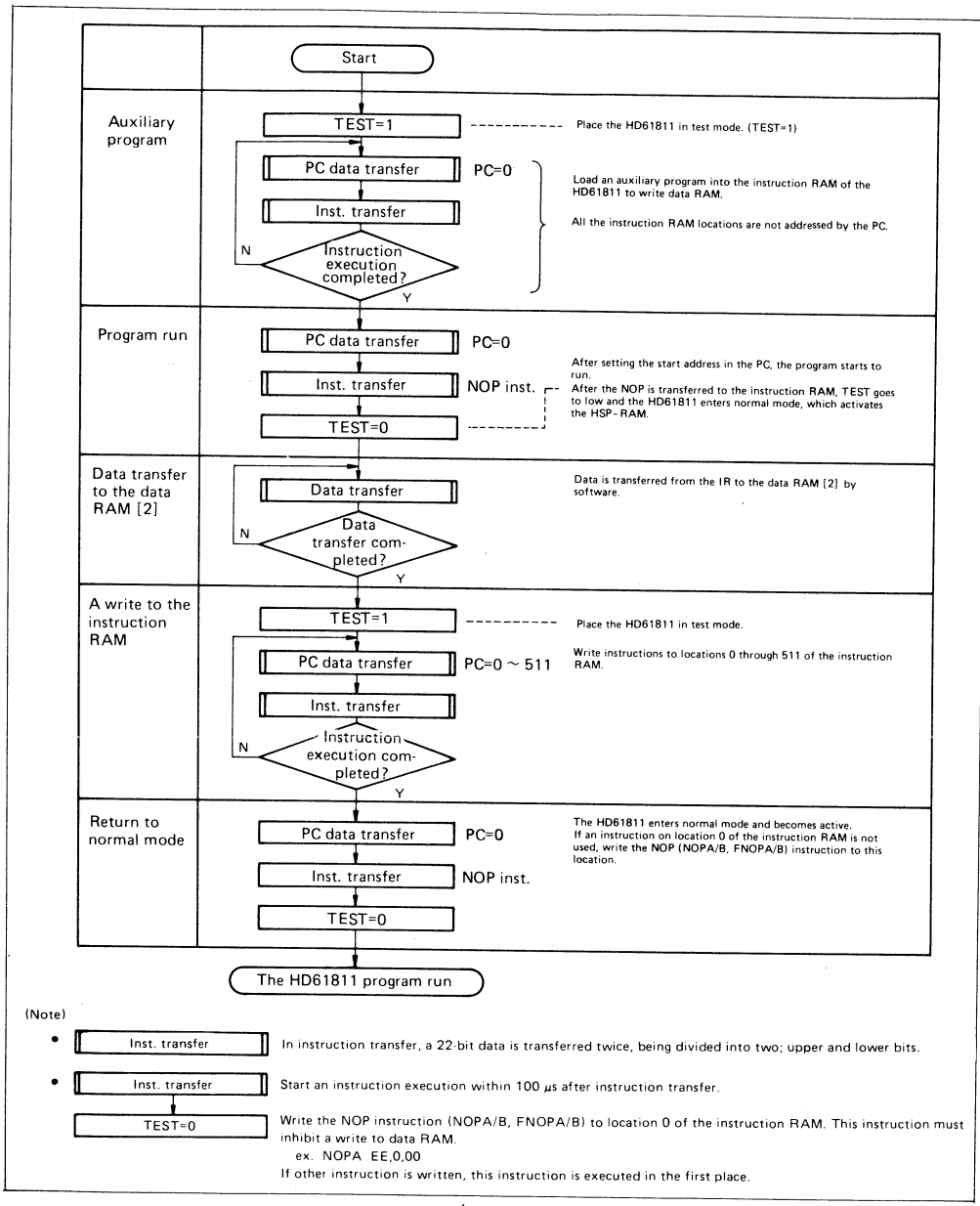


Fig. 22 Application Circuit Diagram (Cont'd)

- **Microcomputer Procedure**



(Note)

- Inst. transfer — In instruction transfer, a 22-bit data is transferred twice, being divided into two; upper and lower bits.
- Inst. transfer / TEST=0 — Start an instruction execution within 100 μs after instruction transfer. Write the NOP instruction (NOPA/B, FNOPA/B) to location 0 of the instruction RAM. This instruction must inhibit a write to data RAM.
  ex. NOPA EE,0,00
  If other instruction is written, this instruction is executed in the first place.

Fig. 23 Initial Procedure of Using the HD61811

- **An Example of Auxiliary Program**

```
HSPSUB.SRC        ***HSP CROSS ASSEMBLER VER 1.0***HSP SUB PROGRAM        PAGE 0001

SEQ LOC OBJECT                    PROGRAM        HSP SUB PROGRAM
0001                                    NAM     HSP SUB PROGRAM
0002                              ;
0003                              ;     PROGRAM FOR HSP DATA ROM(RAM) SETUP
0004                              ;
0005  0001                              ORG     $01
0006                              ; REGISTER INITIALIZE
0007  0001  3C  C0  00                  NOPA    EE,0,00           ; DUMMY
0008  0002  24  00  00                  LIRO    0                 ; RO=0
0009  0003  20  00  FC                  LIA     $00FC             ; WORD TRANSFER MODE
0010  0004  30  40  00                  TFR     A,CTR
0011  0005  20  00  F8                  LIA     $00F8             ; INTERRUPT MASK
0012  0006  30  00  00                  TFR     A,STR
0013                              ; ROM DATA ACCEPT LOOP
0014  0007  2A  00  10            LOOP  JSR     WAIT              ; ROM DATA ACCEPT
ILLEGAL MEMORY ADDRESS- 00000
0015  0008  3C  CC  20                  NOPA    A,XY(0,4),RA,RO   ; PAGE4 DATA WRITE
0016  0009  2A  00  10                  JSR     WAIT              ; ROM DATA ACCEPT
ILLEGAL MEMORY ADDRESS- 00015
0017  000A  3C  CC  28                  NOPA    A,XY(0,5),RA,RO   ; PAGE5 DATA WRITE
0018  000B  2A  00  10                  JSR     WAIT              ; ROM DATA ACCEPT
ILLEGAL MEMORY ADDRESS- 00017
0019  000C  3C  CC  30                  NOPA    A,XY(0,6),RA,RO   ; PAGE6 DATA WRITE
0020  000D  2A  00  10                  JSR     WAIT              ; ROM DATA ACCEPT
ILLEGAL MEMORY ADDRESS- 00019
0021  000E  3C  CC  3A                  NOPA    A,XY(0,7),RA,RO+  ; PAGE7 WRITE & RO+
0022  000F  28  00  07                  JMP     LOOP              ; TO NEXT POINTER ADD.
0023                              ; DATA ACCEPT ROUTINE
0024  0010  34  00  00            WAIT  TFR     STR,A             ; DATA TRANSFERD ?
0025  0011  14  40  00                  SRA     EE,0,00           ; STATUS(PF) TEST
0026  0012  28  80  14                  JCS     TRNS              ; JMP IF PF=1
0027  0013  28  00  10                  JMP     WAIT              ; WAIT UNTIL TRANS
0028  0014  34  C0  00            TRNS  TFR     IR,A              ; DATA ACCEPT
0029  0015  3E  40  00                  RTN                       ; RETURN
0030                                    END

***TOTAL ERRORS 0004 - 0021
```

In this program data in the IR is transferred to the following data RAM [2] address in order of being latched:

4,00 5,00 6,00 7,00 4,01 5,01 6,01 7,01 4,02 .....

The HD61811 uses the HSP assembler including an instruction which performs a write to data ROM. This leads an error to be found.

Fig. 24 An Example of the HSP-RAM Program for Data Load

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

(V_{SS} = 0V)

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	$V_{CC1} = V_{CC2} = V_{CC3} = V_{CC}$
Input Voltage	V_{in}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature Range	T_{opr}	0 to +70	°C	
Storage Temperature Range	T_{stg}	−55 to +150	°C	

2. Electrical Characteristics

- **DC characteristics (Vcc=5.0V±5%, Vss=0V, Ta =0 to +70°C unless otherwise specified)**

Item	Functional Pin	Symbol	Condition	min	typ	max	Unit
Input "High" Voltage	OSC, IE, SICK SOCK	V_{IH}		2.4	–	Vcc+0.3	V
	All others			2.2	–	Vcc+0.3	V
Input "Low" Voltage	OSC, IE, SICK, SOCK	V_{IL}		-0.3	–	0.4	V
	All others			-0.3	–	0.8	V
Input Leakage Current	TEST, TxAK, IE, R/$\overline{W}$, $\overline{CS}$, F_0–F_3, $\overline{DEND}$, SI, SIEN, SOCK, $\overline{SOEN}$, SICK, $\overline{RES}$, OSC, IWI	$\lvert I_{IN} \rvert$	Vin = 0.4 to 2.4V	–	–	10	μA
Three State Current (Off State)	D_0–D_{15}, SO	$\lvert I_{TSI} \rvert$	Vin = 0.4 to 2.4V	–	–	10	μA
Open Drain Current (Off State)	TxRQ, BITI/O, AT	$\lvert I_{LOH} \rvert$	Vin = 0.4 to 2.4V	–	–	10	μA
Output "High" Voltage	D_0–D_{15}, SO, SYNC	V_{OH}	$-I_{OH}$ = 400μA	2.4	–	–	V
Output "Low" Voltage	All output pins	V_{OL}	I_{OL} = 1.6mA	–	–	0.8	V
Input Capacitance	All input pins	Cin	V_{in}=0V, f=1MHz, Ta=25°C	–	–	12.5	pF
Current Dissipation		Icc	Not port loading	–	150	300	mA

- **AC characteristics (Vcc = 5.0V±5%, Vss=0V, Ta=0 to +70°C unless otherwise specified)**

System Clock

Item	Symbol	Condition	min	typ	max	Unit
Clock (OSC) Period	ϕ_{cyc}	See Fig. 25	61.5	62.5	70.0	ns
Clock (OSC) Pulse Width	ϕ_{WH}		20	–	–	ns
	ϕ_{WL}		20	–	–	ns
Clock (OSC) Rise Time	ϕr		–	–	10	ns
Clock (OSC) Fall Time	ϕf		–	–	10	ns

Reset Timing

Item	Symbol	Condition	min	typ	max	Unit
Power-on Reset Timing	t_{RC}	See Fig. 26	20	–	–	ms
Reset Pulse Width	t_{RST}		1.0	–	–	μs

Serial I/O Timing

Item	Symbol	Condition	min	typ	max	Unit
Clock (SICK, SOCK) Period	Scyc	See Fig. 27	1.0	–	10.0	μs
Clock (SICK, SOCK) Pulse Width	S_{WH}		450	–	–	ns
	S_{WL}		450	–	–	ns
Clock (SICK, SOCK) Rise Time	Sr		–	–	25	ns
Clock (SICK, SOCK) Fall Time	Sf		–	–	25	ns
Serial Input Data Set-up Time	t_{SDS}		100	–	–	ns
Serial Input Data Hold Time	t_{SDH}		100	–	–	ns
Serial Output Data Delay Time	t_{SDD}		–	–	300	ns
Enable Delay Time	t_{ED}		50	–	–	ns
Enable Set-up Time	t_{ES}		200	–	–	ns

DMA Timing

Item	Symbol	Condition	min	typ	max	Unit
TxAK Set-up Time	t_{AS}	See Fig. 28	140	–	–	ns
TxAK Hold Time	t_{AH}		–	–	600	ns
TxRQ Delay Time	t_{TR}		–	–	470	ns

Parallel I/O Timing In Normal Mode

Item	Symbol	Condition	min	typ	max	Unit
IE Period	t_{cyc}	See Fig. 29	1.0	–	10.0	μs
IE Pulse Width	t_{WH}		450	–	–	ns
	t_{WL}		450	–	–	ns
IE Rise Time	t_r		–	–	25	ns
IE Fall Time	t_f		–	–	25	ns
$\overline{CS}$ Set-up Time	t_{cs1}		140	–	–	ns
$\overline{CS}$ Hold Time	t_{CH1}		10	–	–	ns
Address Set-up Time	t_{AC}		10	–	–	ns
Address Hold Time	t_{CA}		20	–	–	ns
Input Data Set-up Time	t_{DSW1}		190	–	–	ns
Input Data Hold Time	t_{DHW1}		10	–	–	ns
Output Data Delay Time	t_{DDR1}		–	–	220	ns
Output Data Hold Time	t_{DHR1}		10	–	–	ns

Parallel I/O Timing In Test Mode

Item	Symbol	Condition	min	typ	max	Unit
IE Period	t_{cyc}	See Fig. 30	1.0	–	10.0	μs
IE Pulse Width	t_{WH}		450	–	–	ns
	t_{WL}		450	–	–	ns
IE Rise Time	t_r		–	–	25	ns
IE Fall Time	t_f		–	–	25	ns
$\overline{CS}$ Set-up Time	t_{cs2}		200	–	–	ns
$\overline{CS}$ Hold Time	t_{CH2}		10	–	–	ns
Address Set-up Time	t_{AC}		10	–	–	ns
Address Hold Time	t_{CA}		20	–	–	ns
Input Data Set-up Time	t_{DSW2}		200	–	–	ns
Input Data Hold Time	t_{DHW2}		10	–	–	ns
Output Data Delay Time	t_{DDR2}		–	–	550	ns
Output Data Hold Time	t_{DHR2}		10	–	–	ns

Test Run Timing

Item	Symbol	Condition	min	typ	max	Unit
Test Run IE Delay Time	t_{TED}	See Fig. 31	0	–		ns
Test Run $\overline{CS}$ Hold Time	t_{TCH}		500	–	–	ns
Address Set-up Time	t_{AC}		10	–	–	ns
Address Hold Time	t_{CA}		20	–	–	ns

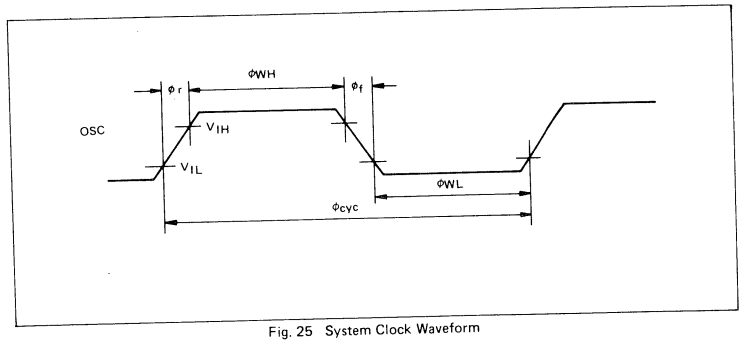


Fig. 25 System Clock Waveform

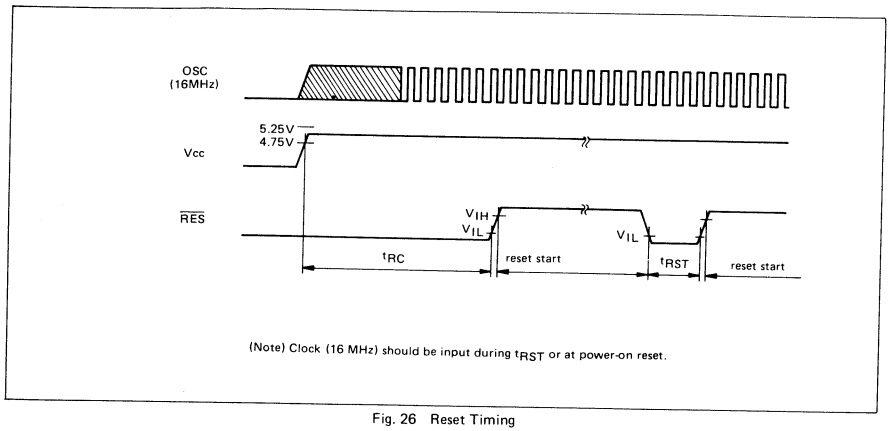


Fig. 26 Reset Timing

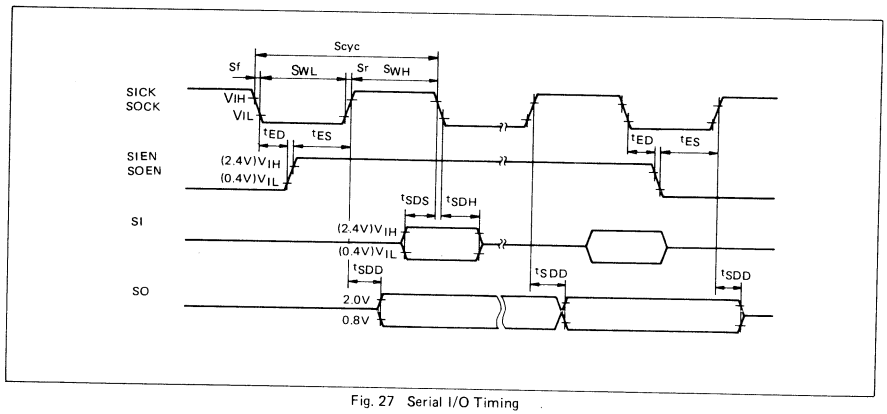


Fig. 27 Serial I/O Timing

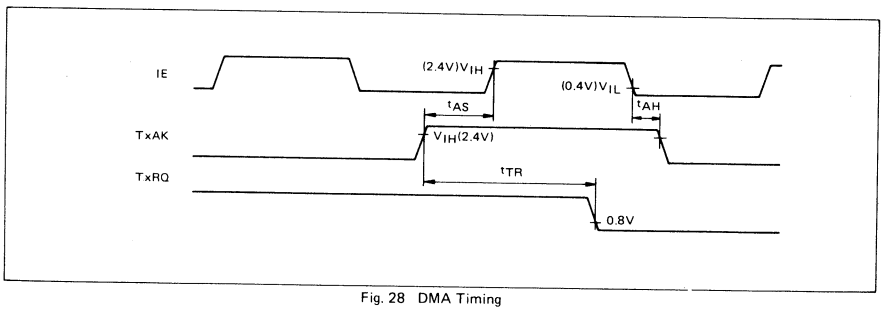
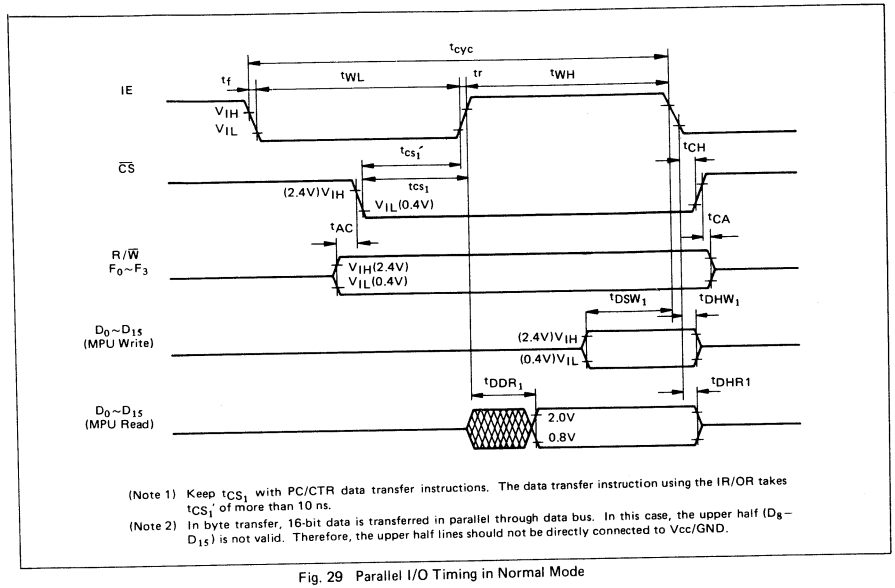


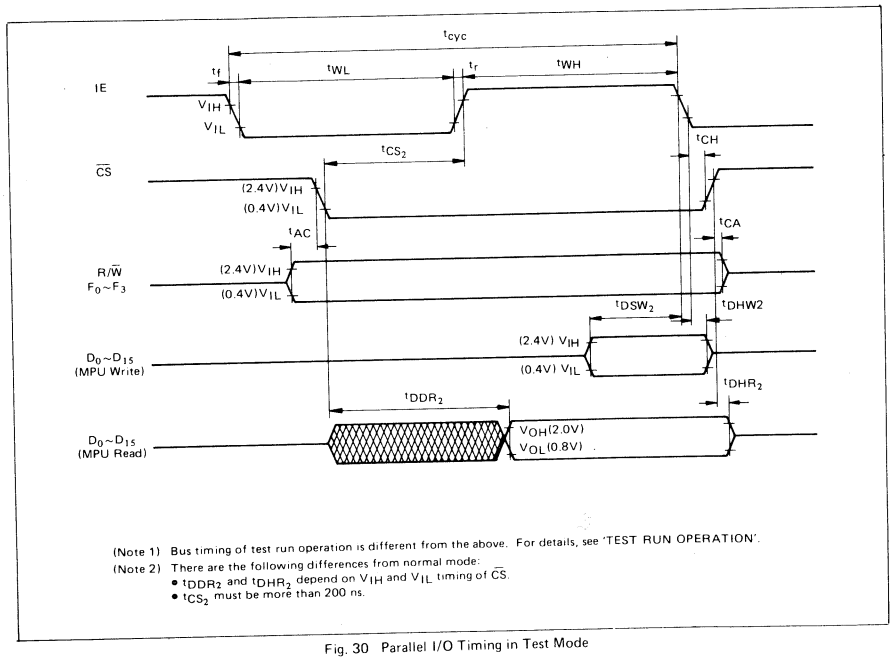
Fig. 28 DMA Timing



(Note 1) Keep t_{CS_1} with PC/CTR data transfer instructions. The data transfer instruction using the IR/OR takes t_{CS_1}' of more than 10 ns.

(Note 2) In byte transfer, 16-bit data is transferred in parallel through data bus. In this case, the upper half (D_8–D_{15}) is not valid. Therefore, the upper half lines should not be directly connected to Vcc/GND.

Fig. 29 Parallel I/O Timing in Normal Mode



(Note 1) Bus timing of test run operation is different from the above. For details, see 'TEST RUN OPERATION'.

(Note 2) There are the following differences from normal mode:
- t_{DDR_2} and t_{DHR_2} depend on V_{IH} and V_{IL} timing of $\overline{CS}$.
- t_{CS_2} must be more than 200 ns.

Fig. 30 Parallel I/O Timing in Test Mode

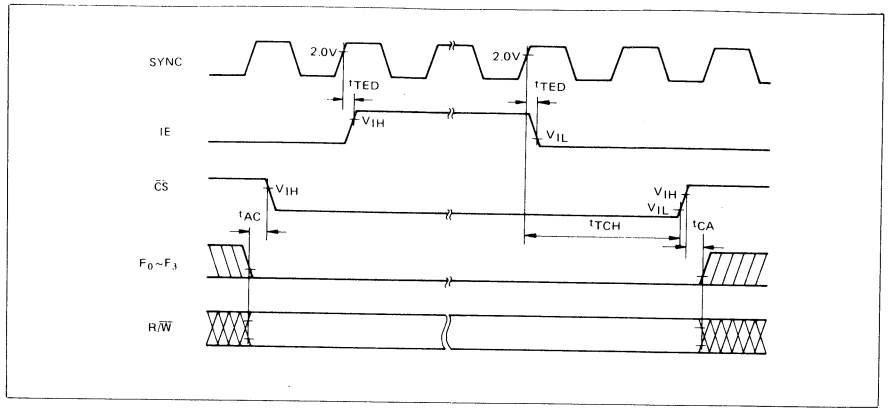
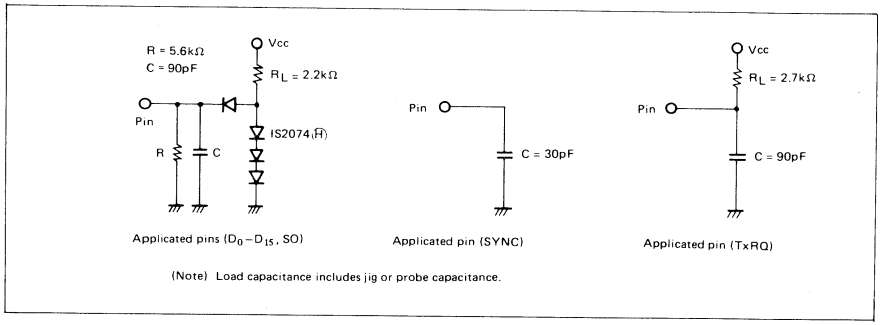


Fig. 31 Test Run Timing



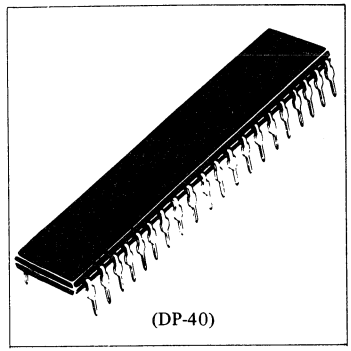
(Note) Load capacitance includes jig or probe capacitance.

Fig. 32 Load Circuit (For Timing Test)

HD81810

High Performance Signal Processor (Wide Operating Temperature Range)

The HD81810 is a single chip processor with a stored program designed for a high speed digital signal processing in WTR (Wide Operating Temperature Range) version. The HSP contains a high speed floating point aritmetic unit and performs an operation (addition/subtruction/multiplication) with an instruction in a single cycle of only 250 ns. Moreover, the HD81810 provides the same instruction set and functions as the HD61810, and employs a CMOS process to realize a low power consumption.


(DP-40)

■KEY FEATURES

- 3 μm CMOS technology
- Arithmetic
  - Floating point arithmetic
  - Pipeline control
  - Horizontal microinstructions
- Large capacity memories
  - 200 × 16-bit data RAM (2-port accessible)
  - 128 × 16-bit data ROM
  - 512 × 22-bit instruction ROM
- System bus compatible with 8/16-bit microcomputer
- DMA operation between the HSP and external memory
- Serial I/O interface for up to 16 bits
- Operation speed
  - Input clock ; 16 MHz
  - Internal clock ; 4 MHz
  - Instruction cycle; 250 ns
  - MULT, ALU ; 250 ns (throughput with pipeline control)
- A single power supply of +5V
- Low power dissipation of 250 mW typ.
- Two levels of subroutine and interrupt
- Interrupt by three factors (end of three kinds of data I/O transfer)

■ARCHITECTURE

● Floating Point Arithmetic

The floating point arithmetic expresses a number with a mantissa and an exponent as follows;

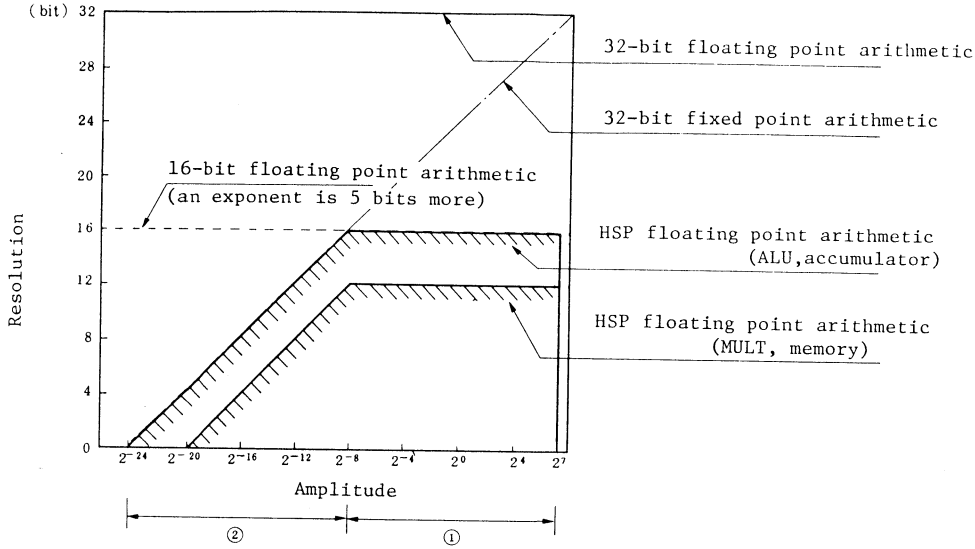
$$n = a \cdot 2^b \quad (a;\ \text{mantissa},\ b;\ \text{exponent})$$

The floating point arithmetic allows a wide range of numbers to be expressed with less bits, and realizes an easy programming without digit adjustment.

The HSP provides 16 bits for mantissa and 4 bits for exponent and can always work in the maximum precision (16 bits).

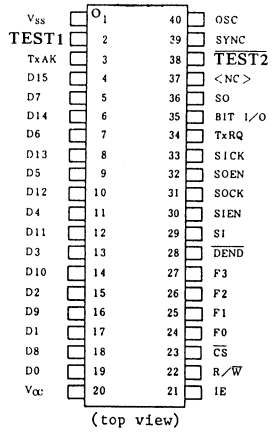
In the ALU and an accumulator, the mantissa is 16 bits and the exponent is 4 bits, while in multiplier and memory, the mantissa is 12 bits and the exponent is 4 bits. These data formats allow the HSP to have the precision given by the hatches in next figure in the floating point operation. As the exponent is 4 bits, it is fixed to -8 when the data amplitude is low. Therefore, the effective bit length varies in proportion to the data amplitude. When the data exceeds 2^{-8}, the mantissa is normalized and the exponent varies; the effective bit length is fixed to 16 bits maximum.

As described above, the HSP realizes a 32-bit dynamic range with 16 bits of the mantissa and 4 bits of the exponent.



HSP FLOATING POINT ARITHMETIC

■PIN ARRANGEMENT



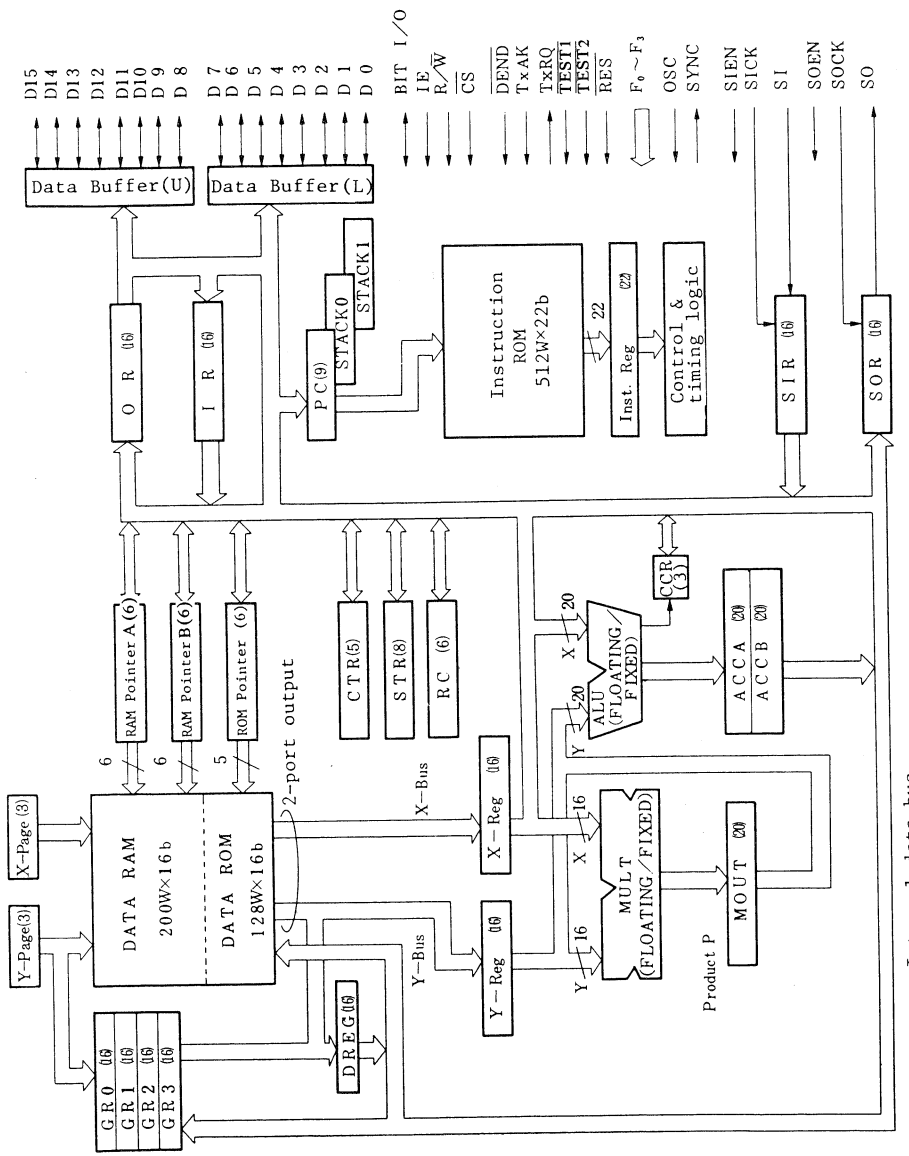
■PIN FUNCTIONS

Signal	Pin	I/O	Functions
			Power Supply
Vcc	20		5V
Vss	1		0V
			Clocks
OSC	40	I	The external clock used to operate the HSP. Clock rate; 16 MHz
SYNC	39	O	The internal clock of the HSP. Clock rate; 4 MHz
			Serial I/O
SICK	33	I	Serial input clock. The serial data is input synchronously with this clock.
SIEN	30	I	Serial input enable. The serial input data is fetched into the serial input register with high level of SIEN. After the completion of a fetch, an interrupt can be generated in the HSP.
SI	29	I	Serial data input. Enters the serial data into the serial input register on the negative edge of SICK.
SOCK	31	I	Serial output clock. The serial data is output synchronously with this clock.
SOEN	32	I	Serial output enable. The serial output data is output from the serial output register with high level of SOEN. After the completion of output, an interrupt can be generated in the HSP on the negative edge of SOEN.
SO	36	O	Serial data output. Three states. Outputs the serial data from the serial output register on the positive edge of SOCK. When SOEN is low, this pin goes to the high-impedance state.
			DMA Operation
TxAK	3	I	Transfer acknowledge. DMA data transfer acknowledge input signal.
TxRQ	34	O	Transfer request, open drain output. Used mainly in the DMA operation mode. This signal requests the external device (DMAC) to transfer data. If TxRQ (DMA transfer request bit) in the control register (CTR) is set, this pin goes to the high level, which requests a DMA service. This signal is automatically cleared with an input of TxAK. Even in the DMA operation mode, internal data transfer among the input/output register (IR/OR), an accumulator and memory is controlled by software. TxRQ can be used as just an output pin in the non-DMA operation mode, and the status of TxRQ is altered by software.
$\overline{\text{DEND}}$	28	I	DMA operation end signal. When $\overline{\text{DEND}}$ is active low, a DMA operation is completed.

(to be continued)

Signal	Pin	I/O	Functions
			Data Bus
D0	19	I/O	Three states, bidirectional I/O ports. The direction
D1	17		of data bus depends on Read/Write (R/$\overline{W}$) control
D2	15		signal. When $\overline{CS}$ (Chip Select) is high, these pins
D3	13		are placed in the high-impedance state.
D4	11		The contents of the CTR and the function control pins
D5	9		(F0 to F3) select 8-bit or 16-bit transfer mode.
D6	7		
D7	5		
D8	18		
D9	16		
D10	14		
D11	12		
D12	10		
D13	8		
D14	6		
D15	4	I/O	
			Parallel I/O Control
F0	24	I	Function control. These signals select an internal
F1	25	I	register for the parallel data I/O. Connected to
F2	26	I	address buses of the microcomputer (6800/68000).
$\overline{F3}$	27	I	
$\overline{CS}$	23	I	Chip select. The chip select signal enables the parallel I/O. When $\overline{CS}$ is active low, D0 to D15, F0 to F3, R/$\overline{W}$ and IE are valid.
R/$\overline{W}$	22	I	Read/Write signal of the microcomputer. Data is read from the HSP with high level of this pin, and is written into the HSP with low level. Valid only when $\overline{CS}$ is active low.
IE	21	I	Interface enable. Data transfer timing signal on data bus (D0 to D15). The data on the data bus is transferred to the internal shift register with this signal. Valid only when $\overline{CS}$ is active low.
$\overline{TEST2}$	37	I	**Chip test pin (please use OPEN)**
TEST	2	I	Chip test pin (tied to GND).
$\overline{RES}$	38	I	Reset pin. The low level input of $\overline{RES}$ clears the program counter (PC). In the status register (STR), interrupt mask flag I_M is set to disable an interrupt, and the I/O data transfer end flags (PF, SIF and SOF) are cleared. In the control register, DMA and TxRQ bits for DMA operation are cleared. When $\overline{RES}$ goes to high level, the program is executed from location 1. The instruction of location 0 is not executed. (note) To reset, $\overline{RES}$ should remain low for more than 1 µs when OSC is applied.
BIT I/O	35	I/O	Open drain output, 1-bit bidirectional I/O pin. The status of BIT I/O depends on software. Set the internal flip-flop of BIT I/O to a one before data input.

■BLOCK DIAGRAM



Input/Output Registers		
Input Register	IR	16-bit register. Data is input to this register through the external data bus (D0-D15).
Output Register	OR	16-bit register. Data is output from this register to the external data bus (D0-D15).
Serial Input Register	SIR	16-bit shift register for serial data input. After a serial data is transferred from the SIR to an accumulator (ACCA or ACCB), the SIR is cleared.
Serial Output Register	SOR	16-bit shift register for serial data output. If data has been transferred to the SOR through the internal data bus, the data is output to peripherals on a bit basis.
Control Registers		
Condition Code Register	CCR	The CCR contains three flag bits; Carry (C), Negative (N), and Zero (Z). They indicate the results of ALU operation.
Status Register	STR	The STR flags are individually set or cleared depending on the status of the HSP. The contents of the STR can be transferred to an accumulator.
Control Register	CTR	The CTR is used to select the desired operating modes for the HSP. The CTR contents are determined by either the HSP instructions or the MPU.
Instruction Controllers		
Instruction ROM		A 512 word by 22 bit ROM. The instruction ROM stores instructions for the HSP. 22-bit instruction is transferred to the instruction register in parallel in a single instruction cycle.
Program Counter	PC	The PC is a 9-bit address counter that is used to address the Instruction ROM. The PC generates the instruction ROM addresses 0 through 511.
Stack Registers	STACK0 STACK1	The stack registers are 9-bit registers that are used to save the PC contents. The contents of the PC is pushed onto these registers when a subroutine jump or an interrupt occurs.
Repeat Counter	RC	6-bit down counter. The RC is used for repeated execution of an instruction and for the control of loops.
Instruction Register	Inst. Reg.	22-bit buffer register. This register temporarily stores the instruction transferred from the instruction ROM.

Internal Memory Controllers		
Data RAM		A 200 word by 16 bit RAM. 50 ward x 4 pages (page 0 through 3)
Data ROM		A 128 word by 16 bit ROM. 32 word x 4 pages (page 4 through 7)
RAM Pointer A RAM Pointer B	RA RB	These are 6-bit address pointers which are used to generate the data RAM address, combining with the contents of page address.
ROM Pointer	RO	This is a 6-bit address pointer which is used to generate the data ROM address, combining with the contents of page address.
X and Y page Address Pointers	X/Y-Page	These are 3-bit buffer registers for a page address. The effective address for the data RAM or the data ROM consists of this address and the contents of the RAM/ROM pointer.
General Registers	GR0-3	16-bit general purpose registers. The GRs can be used as working registers. Data is transferred to or from the GRs through the Y-Bus.
Delay Register	DREG	16-bit register. The DREG holds the data to be transferred through the Y-but for a single instruction cycle period.
Arithmetic Elements		
Accumulator A Accumulator B	ACCA ACCB	20-bit accumulators. The accumulators store the output from the ALU. Either the ACCA or ACCB is selected in response to the instructions.
Arithmetic Logic Unit	ALU	The ALU performs arithmetic and logical operations. Either the fixed point operation or the floating point operation is selected depending on the instructions.
Multiplier	MULT	The MULT performs a multiply operation. Either the fixed point operation or the floating point operation is selected depending on the instructions.
Multiplier Input X-Register	X-Reg.	16-bit register. The X-Reg. holds the data transferred from the X-bus or the internal data bus during a multiply operation.
Multiplier Input Y-Register	Y-Reg.	16-bit register. The Y-Reg. holds the data transferred from the Y-bus or the internal data bus during a multiply operation.
Multiplier Output Register	MOUT	This is a 20-bit buffer register which holds the output from the MULT for a single instruction cycle period. This register consists of a mantissa (16 bits) and an exponent (4 bits).

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Value	Unit
Supply Voltage	V_{cc}	−0.3 to 7.0	V
Input Voltage	V_{in}	−0.3 to V_{cc} + 0 3	V
Operating Temperature Range	T_{opr}	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{cc} = 5.0V ± 5%, V_{ss} = 0V, Ta = −40 to +85°C unless otherwise specified.)

Item		Symbol	Test Condition	Min	Typ	Max	Unit
Input "High" Voltage	OSC,IE,SICK,SOCK	V_{IH}		2.4	−	V_{cc}+0.3	V
	All others			2.2	−	V_{cc}+0.3	V
Input "Low" Voltage	OSC,IE,SICK,SOCK	V_{IL}		−0.3	−	0.4	V
	All others			−0.3	−	0.8	V
Input Leak Current	$\overline{TEST}$,TxAK,IE,R/$\overline{W}$, $\overline{CS}$, F_0∿F_3,$\overline{DEND}$,SI SIEN,$\overline{SOCK}$,SOEN SICK,$\overline{RES}$,OSC	$\lvert I_{IN} \rvert$	V_{IN}=0.4 to 2.4V	−	−	10	µA
Three State Current (OFF State)	D_0∿D_{15}, SO	$\lvert I_{TSI} \rvert$	V_{IN}=0.4 to 2.4V	−	−	10	µA
Open Drain Current (OFF State)	TxRQ,BIT I/O	$\lvert I_{LOH} \rvert$	V_{IN}=0.4 to 2.4V	−	−	10	µA
Output "High" Voltage	D_0∿D_{15},SO,SYNC	V_{OH}	$-I_{OH}$=400µA	2.4	−	−	V
Output "Low" Voltage	All output pins	V_{OL}	I_{OL}=1.6 mA	−	−	0.8	V
Input Capacitance	All output pins	C_{IN}	V_{IN}=0V, f=1MHz T_a=25°C	−	−	12.5	pF
Current Dissipation		I_{CC}	Not port loading	−	50	100	mA

- **AC Characteristics**

System Clock (V_{cc}=5.0V±5%, V_{ss}=0V, T_a=–40 to +85°C unless otherwise specified.)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Clock (OSC) cycle	ϕ_{cyc}	Fig. 1	61.5	62.5	70.0	ns
Clock (OSC) Pulse Width	ϕ_{WH}		20	–	–	ns
	ϕ_{WL}		20	–	–	ns
Clock (OSC) Rise Time	ϕ_r		–	–	10	ns
Clock (OSC) Fall Time	ϕ_f		–	–	10	ns

Serial I/O Timing (V_{cc}=5.0V±5%, V_{ss}=0V, T_a=–40 to +85°C unless otherwise specified.)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Clock (SICK, SOCK) cycle	S_{cyc}	Fig. 2 Fig. 5	1.0	–	10.0	µs
Clock (SICK, SOCK) Pulse Width	S_{WH}		450	–	–	ns
	S_{WL}		450	–	–	ns
Clock (SICK, SOCK) Rise Time	S_r		–	–	25	ns
Clock (SICK, SOCK) Fall Time	S_f		–	–	25	ns
Serial Input Data Set-up Time	t_{SDS}		100	–	–	ns
Serial Input Data Hold Time	t_{SDH}		100	–	–	ns
Serial Output Data Delay Time	t_{SDD}		–	–	300	ns
Enable Delay Time	t_{ED}		50	–	–	ns
Enable Set-up Time	t_{ES}		100	–	–	ns

Parallel I/O (Bus Interface) Timing (V_{cc}=5.0V±5%, V_{ss}=0V, T_a=–40 to +85°C unless otherwise specified.)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
IE cycle	t_{cyc}	Fig. 3 Fig. 5	1.0	–	10.0	µs
IE Pulse Width	t_{WH}		450	–	–	ns
	t_{WL}		450	–	–	ns
IE Rise Time	t_r		–	–	25	ns
IE Fall Time	t_f		–	–	25	ns
$\overline{CS}$ Set-up Time	t_{CS}		140	–	–	ns
$\overline{CS}$ Hold Time	t_{CH}		10	–	–	ns
Address Set-up Time	t_{AC}		10	–	–	ns
Address Hold Time	t_{CA}		20	–	–	ns
Input Data Set-up Time	t_{DSW}		190	–	–	ns
Input Data Hold Time	t_{DHW}		10	–	–	ns
Output Data Delay Time	t_{DDR}		–	–	220	ns
Output Data Hold Time	t_{DHR}		10	–	–	ns

DMA Interface Timing (V_{cc}=5.0V±5%, V_{ss}=0V, T_a=–40 to +85°C unless otherwise specified.)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
TxAK Set-up Time	t_{AS}	Fig. 4 Fig. 5	140	–	–	ns
TxAK Hold Time	t_{AH}		–	–	600	ns
TxRQ Delay Time	t_{TR}		–	–	470	ns

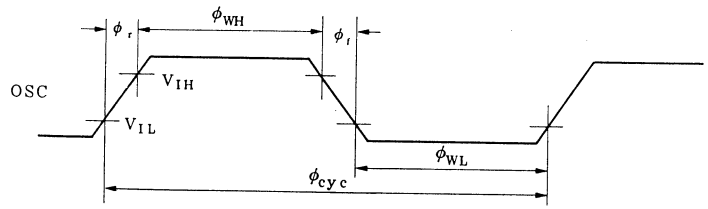
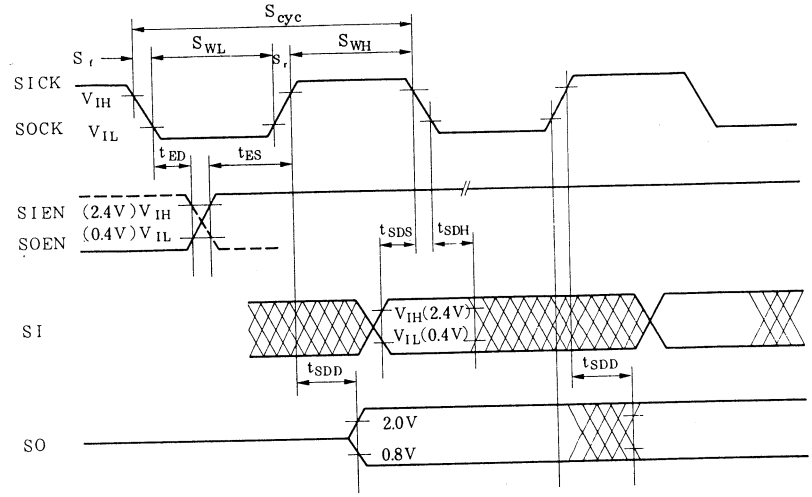
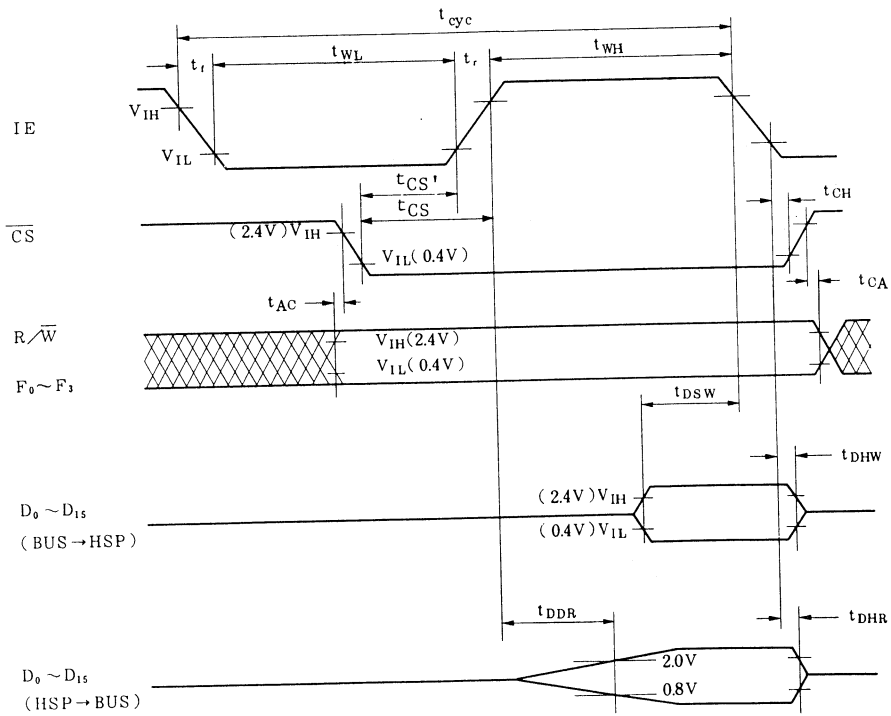


Fig. 1 SYSTEM CLOCK WAVEFORM



(Note) The SO pin goes to the high-impedence state by latching SOEN with SOCK.

Fig. 2 SERIAL I/O WAVEFORM



(Note 1) Keep t_{CS} (min. 140ns) with CTR/PC transfer instructions.

The data transfer instruction using the IR/OR takes t_{CS} of more than 10 ns.

(Note 2) The data bus output in the byte transfer mode is 16 bit ($D_0 - D_{15}$). In this case, the upper half ($D_8 - D_{15}$) is not valid. Therefore, $D_8 - D_{15}$ should not be directly connected to V_{CC}/GND.

Fig. 3 PARALLEL I/O TIMING

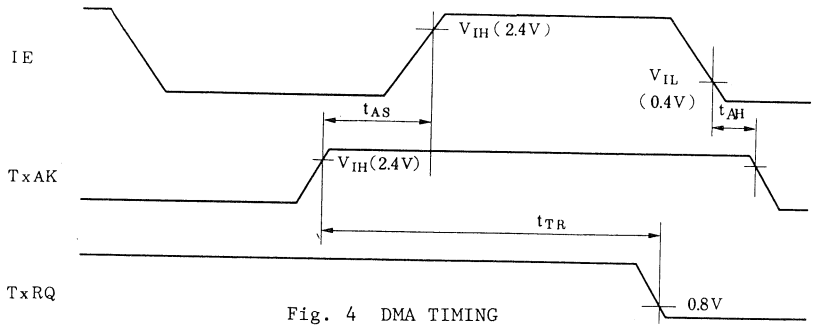
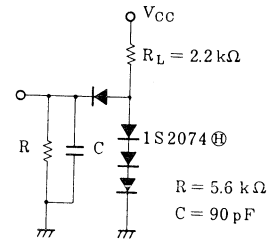
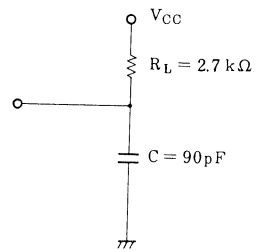


Fig. 4 DMA TIMING



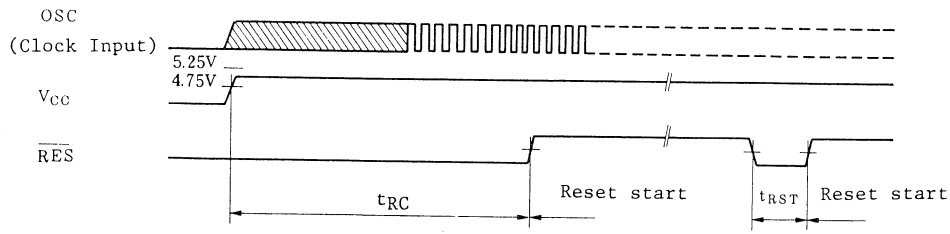
Applicable terminal ($D_0 - D_{15}$, SO)



Applicable terminal (TxRQ)

C : includes probe and jig capacitance

Fig. 5 LOAD CIRCUIT (FOR TIMING TEST)



Power-ON reset t_{RC} = 20ms (min)

Reset during operation t_{RST} = 1μs (min)

(Note) Clock (16 MHz) should be input during t_{RST} or the power-ON rest start.

Fig. 6 RESET Timing

Data Communications

HD6350P Series

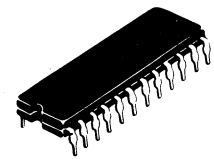
CMOS ACIA (Asynchronous Communications Interface Adapter)

The HD6350 CMOS Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the HMCS6800 Microprocessing Unit.

The bus interface of the HD6350 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking.

The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation three control lines are provided. Exceeding Low Power dissipation is realized due to adopting CMOS process.

HD6350P, HD63A50P, HD63B50P

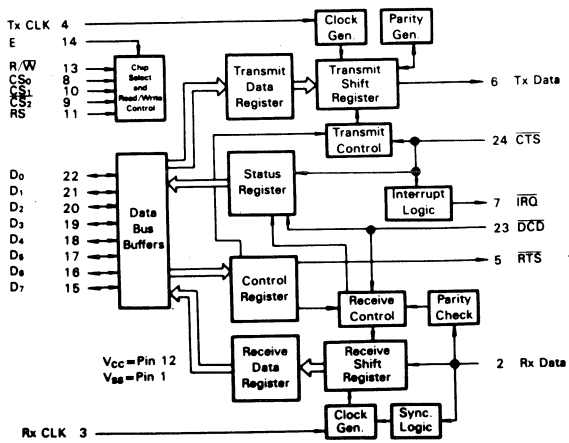


(DP-24)

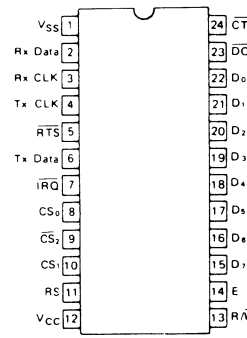
■ FEATURES

- Low-Power, High-Speed, High-Density CMOS
- Compatible with NMOS ACIA (HD6850)
- Serial/Parallel Conversion of Data
- Seven and Eight-bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Peripheral/Modem Control Functions (Clear to Send $\overline{CTS}$, Request to Send $\overline{RTS}$, Data Carrier Detect $\overline{DCD}$)
- Optional ÷ 1, ÷ 16, and ÷ 64 Clock Modes
- Up to IM bps Transmission (HD63B50)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TYPE OF PRODUCTS

Type No.	Bus Timing
HD6350P	1 MHz
HD63A50P	1.5 MHz
HD63B50P	2 MHz

This data only introduces an outline of the function.
Please see the data book for details.

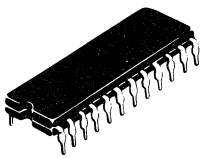
HD6850P Series

ACIA (Asynchronous Communications Interface Adapter)

The HD6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the HMCS6800 Microprocessing Unit.

The bus interface of the HD6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking.

HD6850P, HD68A50P

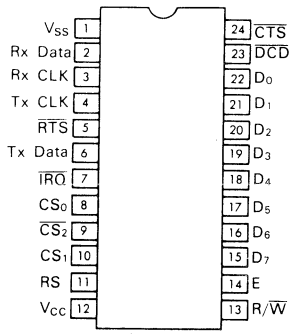


(DP-24)

■ FEATURES

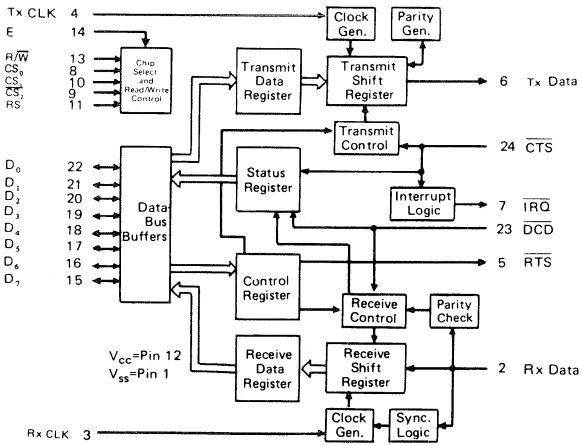
- Serial/Parallel Conversion of Data
- Seven and Eight-bit Transmission
- Insertion and Deleting of Start and Stop Bit
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Peripheral/Modem Control Functions (Clear to Send $\overline{CTS}$, Request to Send $\overline{RTS}$, Data Carier Detect $\overline{DCD}$)
- Optional ÷ 1, ÷ 16, and ÷ 64 Clock Modes
- Up to 500kbps Transmission
- Programmable Control Register
- N-channel Silicon Gate Process
- Compatible with MC6850 and MC68A50

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ TYPE OF PRODUCTS

Type No.	Bus Timing
HD6850P	1 MHz
HD68A50P	1.5 MHz

This data only introduces an outline of the function.
Please see the data book for details.

HD6852P Series

SSDA (Synchronous Serial Data Adapter)

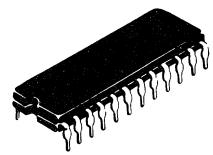
The HD6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the HMCS6800 Microprocessor systems.

The bus interface of the HD6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization.

Programmable control registers provide control for variable word length, transmit control, receive control, synchronization control and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include data communications terminals, floppy disk controllers, cassette or cartridge tape controllers and numerical control systems.

HD6852P, HD68A52P



(DP-24)

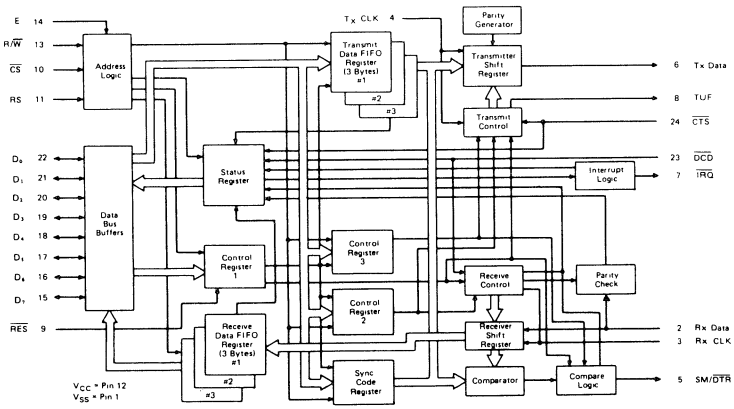
■ FEATURES

- Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- Character Synchronization on One or Two Sync Codes
- External Synchronization Available for Parallel-Serial Operation
- Programmable Sync Code Register
- Up to 1M bps Transmitter
- Peripheral/Modem Control Functions
- Three Bytes of FIFO Buffering on Both Transmit and Receive
- 6, 7, or 8 Bit Data Transmission
- Optional Even and Odd Parity
- Parity, Overrun, and Underflow Status
- Compatible with MC6852 and MC68A52

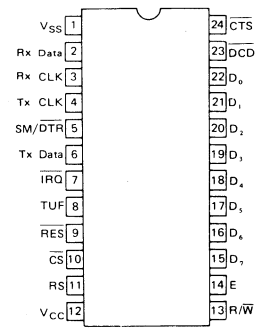
■ TYPE OF PRODUCTS

Type No.	Bus Timing
HD6825P	1 MHz
HD68A52P	1.5 MHz

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

This data only introduces an outline of the function.
Please see the data book for details.

HD63310P Series

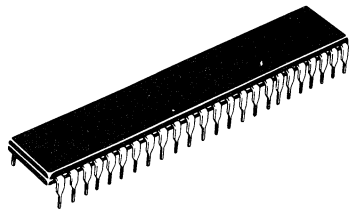
S-DPRAM (Smart Dual Port RAM)

The HD63310 (S-DPRAM) is a high intelligent DPRAM, which provide a communication path between multiprocessor systems.

The HD63310 has 1024 x 8 bit RAM, 62 x 8 bit registers and individual dual I/O ports. The dual ports perform read/write operations independently and simultaneously.

User can select one of the two mode (DPRAM or FIFO mode) by the program. This architecture makes it possible to communicate efficiently according to applications.

HD63310

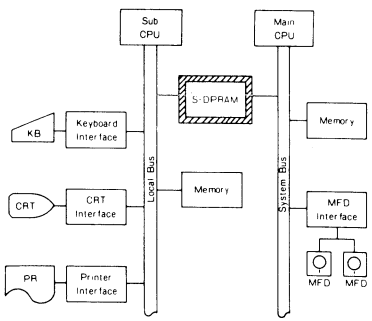


(DP-48)

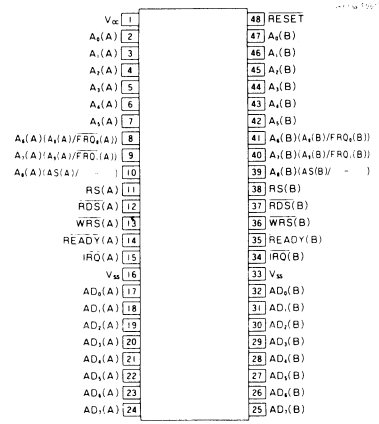
■ FEATURES

- 2 independent asynchronous bus operation Address/Data bus configurable as multiplexed or non-multiplexed bus.
- Dual port large scale data buffer space
  - Dual port RAM mode: 1024 byte
  - FIFO mode: 2 FIFOs for 1024 byte
- 62 internal registers
  - Semaphore registers which support multi-processing (8 bit)
  - 32 registers which user can use freely
- Access Time
  150 ns/200 ns
- Low power consumption
  2 μm full CMOS circuit

■ SYSTEM BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TYPE OF PRODUCTS

Type No.	Access time
HD63310P-15	150 ns
HD63310P-20	200 ns

This data only introduces an outline of the function.
Please see the data book for details.

HD64941

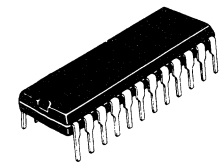
ACI (Asynchronous Communications Interface)

Description

The HITACHI HD64941 is a universal asynchronous data communications controller chip that interfaces directly to most 8-bit microprocessors and may be used in a polled or interrupt-driven system environment. The HD64941 accepts programmed instructions from the microprocessor while supporting asynchronous serial data communications in full- or half-duplex mode.

The HD64941 serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The HD64941 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

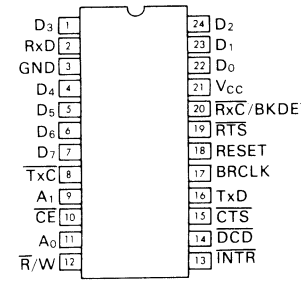


(DP-24N)

Features

- 5- to 8-bit characters plus parity
- 1, 1.5 or 2 stop bits transmitted
- Odd, even or no parity
- Parity, overrun and framing error detection
- Line break detection and generation
- False start bit detection
- Automatic serial echo mode (echoplex)
- Local or remote maintenance loopback mode
- Baud rate:
  - DC to 1M bps (1 x clock)
  - DC to 62.5k bps (16 x clock)
  - DC to 15.625k bps (64 x clock)
- Internal or external baud rate clock
- 16 internal rates
- Double-buffered transmitter and receiver
- Single +5V power supply

Pin Arrangement



(Top View)

Type of Products

Type No.	External Clock	Package
HD64941	3.6864 MHz (Typ.)	24-Pin Plastic Skinny DIP

Interface Signals

The HD64941 interface signals can be grouped into two types: the CPU-related signals (shown in Table 1), which interface the HD64941 to the microprocessor system and the device-related signals (shown in Table 2), which are used to interface to the communications device or system.

CPU Interface Signals

Table 1 CPU Interface Signals

Pin Name	Pin Number	Input/ Output	Function
RESET	18	I	Reset
$\overline{R}/W$	12	I	Read/write
$\overline{CE}$	10	I	Chip enable
D_0-D_7	22, 23, 24 1, 4–7	I/O	Data bus
A_0, A_1	11, 9	I	Address 0, 1
$\overline{INTR}$	13	I	Interrupt request
V_{CC}	21	I	+5V power supply
GND	3	I	Ground

RESET – A high on this input performs a master reset on the ACI. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with appropriate control words.

$\overline{R}/W$ – Read command when low, write command when high.

$\overline{CE}$ – Chip enable command. When low, indicates that control and data lines to the ACI are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the three-state condition.

D_0-D_7 – 8-bit, three-state data bus used to transfer commands, data and status between the HD64941 and the CPU. D_0 is the least significant bit; D_7 the most significant bit. At RESET, these terminals are three-state.

A_0-A_1 – Address lines used to select internal ACI registers.

$\overline{INTR}$ – Interrupt request output (open drain). This output is asserted (low) under the following conditions.

(1) When the transmitter holding register (THR) is ready to accept a data character from the CPU. This corresponds to assertion of status bit SR0. If this is the only condition asserting the output, the output will be negated (high) when the THR is loaded by the CPU, or if the transmitter is disabled via command register bit CR0.

(2) When the receiver holding register (RHR) has a character ready to be read by the CPU. This corresponds to assertion of status bit SR1. If this is the only condition asserting the output, the output will be negated (high) when the RHR is read by the CPU, or if the receiver is disabled via command register bit CR2.

(3) When the transmitter has completed serialization of the last character loaded by the CPU. This corresponds to assertion of status bit SR2. If this is the only condition asserting the output, the output will be negated (high) when the THR is loaded by the CPU.

(4) When a change of state has occurred at the $\overline{DCD}$ input while either the receiver or the transmitter are enabled. This corresponds to assertion of status bit SR2. If this is the only condition asserting the output, the output will be negated (high) when the status register is read by the CPU. At RESET, this terminal is high.

V_{CC}, GND V_{CC} and GND are the +5V power supply and ground pins.

Device Related Signals

Table 2 Device Related Signals

Pin Name	Pin Number	Input/ Output	Function
BRCLK	17	I	Baud rate clock
$\overline{RxC}$/ BKDET	20	I/O	Receiver clock Break detect
RxD	2	I	Receiver data
$\overline{TxC}$	8	I/O	Transmitter clock
TxD	16	O	Transmitter data
$\overline{DCD}$	14	I	Data carrier detect
$\overline{CTS}$	15	I	Clear to send
$\overline{RTS}$	19	O	Request to send

BRCLK – Clock input to the internal baud rate generator (see Table 6). Not required if external receiver and transmitter clocks are used.

$\overline{RxC}$/BKDET – Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1x, 16x or 64x the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1x/16x clock or a break detect output pin. At RESET, this terminal is received-state.

RxD – Serial data input to the receiver. "Mark" is high, "space" is low.

$\overline{TxC}$ – Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1x, 16x or 64x the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1x/16x clock output. At RESET, this terminal is received-state.

TxD – Serial data output from the transmitter. "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled. At RESET, this terminal is high.

$\overline{DCD}$ – Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{INTR}$ when its state changes if CR2 or CR0 – 1. If $\overline{DCD}$ goes high while receiving, the $\overline{RxC}$ is internally inhibited. Operation of the receiver resumes on the second RxC rising edge following assertion of $\overline{DCD}$.

$\overline{CTS}$ – Clear to send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.

$\overline{RTS}$ – General-purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. See Command Register (CR5) for details. At RESET, this terminal is high.

Internal Block Diagram

The ACI consists of five major sections. These are the transmitter, receiver, timing, operation control and modem control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

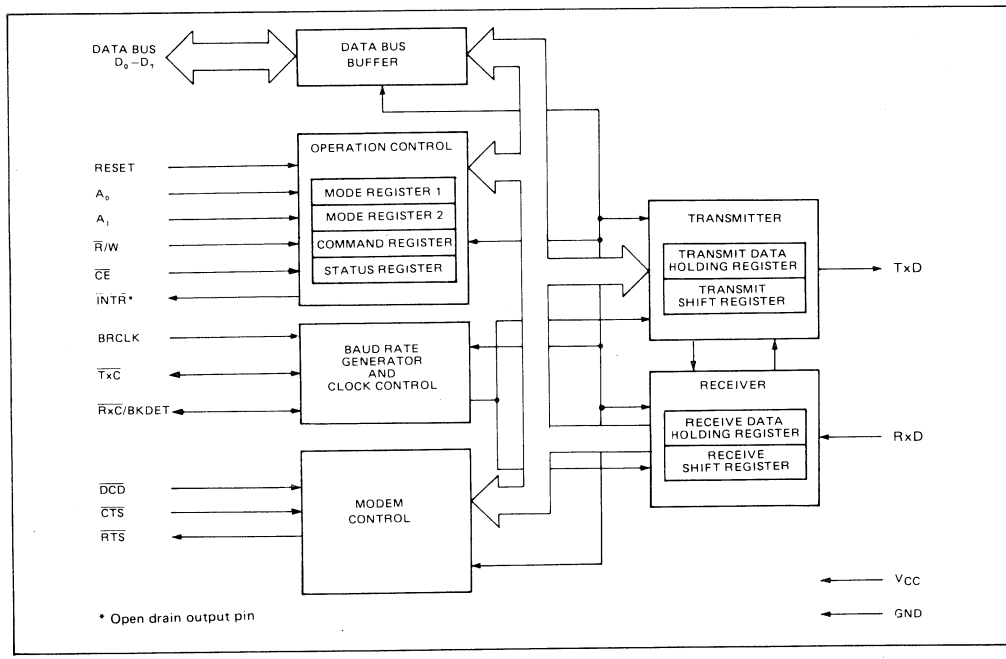
Operation Control
This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing are presented in the ACI programming section of this data sheet.

Timing
The ACI contains a baud rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation. See Table 6.

Receiver
The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for certain errors and sends an "assembled" character to the CPU.

Transmitter
The transmitter accepts parallel data from the CPU, appends start and stop bits, and, optionally, a parity bit, and outputs a composite serial stream of data on the TxD output pin.

Modem Control
The modem control section provides interfacing for two input signals and one output signal used for "handshaking" and status indication between the CPU and a modem.



Operation

The functional operation of the ACI is programmed by a set of control words supplied by the CPU. These control words specify items such as baud rate, number of bits per character, etc. The programming procedure is described in the ACI programming section of this data sheet.
After programming, the ACI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver
The ACI is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. The receiver looks for a high-to-low transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data is then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{INTR}$ output is asserted. If the character length is less than 8 bits, the high-order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive-going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediate-

ly begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins.
Pin 20 can be programmed to be a break detect output by appropriate setting of MR27 MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 20 will go low. Refer to the break detection timing diagram.

Transmitter
The ACI is conditioned to transmit data when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The ACI indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{INTR}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data is transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.
The transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG status bit and the $\overline{INTR}$ output are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the send break command bit (CR3) high.

Programming

Prior to initiating data communications, the ACI operational mode must be programmed by performing write operations to the mode and command registers. The ACI can be reconfigured at any time during program execution. A flowchart of the initialization process appears in Figure 1.

The internal registers of the ACI are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in Table 3.

Reading or loading the mode registers is done as follows: the first write (or read) operation addresses mode register 1 and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointer is reset to mode register 1 by a RESET input or by performing a read command register operation, but is unaffected by any other read or write operation.

The ACI register formats are summarized in Tables 4, 5, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the ACI while the command register controls the operation within this basic framework. The ACI indicates its status in the status register. These registers are cleared when a RESET input is applied.

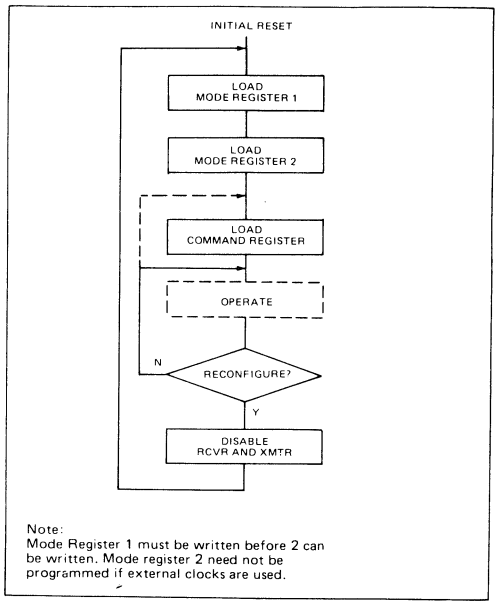


Figure 1 ACI Initialization Flowchart

Table 3 Register Addressing

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	Function
1	X	X	X	Three-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Invalid
0	1	0	0	Read mode registers 1, 2
0	1	0	1	Write mode registers 1, 2
0	1	1	0	Read command register
0	1	1	1	Write command register

(Note) See AC characteristics section for timing requirements.

Internal Registers

Mode Register 1 (MR1)
Table 5 illustrates mode register 1. Bits MR11 and MR10 select the baud rate multiplier. 1x, 16x and 64x multipliers are programmable if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7 or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.
MR17 and MR16 select character framing of 1, 1.5 or 2 stop bits. (If 1x baud rate is programmed, 1.5 stop bits default to 1 stop bit on transmit.)

The bits in the mode register affecting character assembly and disassembly (MR12 – MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver, therefore,

character changes should be made when RxEN and TxEN = 0 or when TxEN = 1 and the transmitter is marking in half-duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12 – MR15 must be changed within n-bit times of the assertion of RxRDY/TxRDY. (n = smaller of the new and old character lengths.)

Mode Register 2 (MR2)

Table 5 illustrates mode register 2. MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable as per Table 6. MR23 – MR20 are don't cares if external clocks are selected (MR25 – MR24 = 0). The individual rates are given in Table 6.

MR24 – MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 8 and 20. Refer to Table 5.

Table 4 Mode Register 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Stop Bit Length		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
00 = Invalid 01 = 1 stop bit 10 = 1 1/2 stop bits 11 = 2 stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits		00 = Invalid 01 = 1x rate 10 = 16x rate 11 = 64x rate	

(Note) Baud rate factor applies only if external clock is selected. Factor is 16x if internal clock is selected.

Table 5 Mode Register 2 (MR2)

MR27 – MR24										MR23 – MR20
	TxC	RxC	Pin 8	Pin 20		TxC	RxC	Pin 8	Pin 20	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	NF	RxC/TxC	See baud rates in Table 6
0001	E	I	TxC	1x	1001	E	I	TxC	BKDET	
0010	I	E	1x	RxC	1010	I	E	NF	RxC	
0011	I	I	1x	1x	1011	I	I	1X	BKDET	
0100	E	E	TxC	RxC	1100	E	E	NF	RxC/TxC	
0101	E	I	TxC	16x	1101	E	I	TxC	BKDET	
0110	I	E	16x	RxC	1110	I	E	NF	RxC	
0111	I	I	16x	16x	1111	I	I	16X	BKDET	

(Notes) E = External clock NF = No function; output not valid I = Internal clock (BRG) 1x and 16x are clock outputs

Table 6 Baud Rate Generator Characteristics (BRCLK = 3.6864MHz)

MR23 – 20	Baud Rate	Actual Frequency 16x Clock	Percent Error	Divisor
0000	50	0.8kHz	–	4608
0001	75	1.2	–	3072
0010	110	1.7596	-0.022	2095
0011	134.5	2.152	–	1713
0100	150	2.4	–	1536
0101	300	4.8	–	768
0110	600	9.6	–	384
0111	1200	19.2	–	192
1000	1800	28.8	–	128
1001	2000	32.055	0.174	115
1010	2400	38.4	–	96
1011	3600	57.6	–	64
1100	4800	76.8	–	48
1101	7200	115.2	–	32
1110	9600	153.6	–	24
1111	19200	307.2	–	12

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high), while the TxRDY and TxEMT status bits go low. Disabling the receiver causes the RxRDY status bit to go low. If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be negated. A 0-to-1 transition of CR2 will initiate start bit search on the second $\overline{RxC}$ rising edge following the transition.

Bit CR5 (RTS) controls the RTS output. Data at the output is the logical complement of the register data.

Setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The user should wait at least one bit time after terminating the break before loading the THR with the next character to be transmitted.

Setting CR4 causes the error flags in the status register (SR3, SR4 and SR5) to be cleared. This is a one-time command. There is no internal latch for this bit.

When CR5 (RTS) is set, the RTS pin is forced low. A 1-to-0 transition of CR5 will cause $\overline{RTS}$ to go high (inactive) one TxC time after the last serial bit has been transmitted. If a 1-to-0 transition of CR5 occurs while data is being transmitted, $\overline{RTS}$ will remain low (active) until both the THR and the transmit shift register are empty and then go high one TxC time later.

The ACI can operate in one of four submodes. The operational submode is determined by CR7 and CR6. CR7 – CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the mode and status register instructions.

CR7 – CR6 = 01 places the ACI in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU-to-receiver communications continue normally, but the CPU-to-transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode:

(1) Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
(2) The transmitter is clocked by the receive clock.
(3) The $\overline{INTR}$ pin will reflect only the data set change condition.
(4) The TxEN command (CR0) is ignored.

Two diagnostic submodes can also be configured. In local loopback mode (CR7 – CR6 = 10), the following loops are connected internally:

(1) The transmitter output is connected to the receiver input.
(2) $\overline{RTS}$ is connected to $\overline{CTS}$.
(3) The receiver is clocked by the transmitter clock.
(4) The $\overline{RTS}$ and TxD outputs are held high.
(5) The $\overline{CTS}$, $\overline{DCD}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the ACI.

The second diagnostic mode is the remote loopback mode (CR7 – CR6 = 11). In this mode:

(1) Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
(2) The transmitter is clocked by the receive clock.
(3) No data is sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
(4) The $\overline{INTR}$ output is held high.
(5) CR0 (TxEN) is ignored.
(6) All other signals operate normally.

Status Register

The data contained in the status register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It is valid only when the transmitter is enabled. If equal to 0, it indicates that the transmit holding register has been loaded by the CPU and the data has not been transferred to the transmit shift register. If set equal to 1, it indicates that the holding register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{INTR}$ output pin is low, except in the automatic echo and remote loopback modes.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be ready by the CPU. If equal to 0, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{INTR}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{DCD}$ input (when CR2 or CR0 = 1) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG condition is enabled when the TxEN = 1 or RxEN = 1. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 = 1 while SR6 remains unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{INTR}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. This bit is cleared when the receiver is disabled and by a reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not read

Table 7 Command Register (CR)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error	Force Break	Receive Control (RxEN)		Transmit Control (TxEN)
00 = Normal operation 01 = Automatic echo mode 10 = Local loopback 11 = Remote loopback		0 = Force $\overline{RTS}$ output high after TxSR serialization 1 = Force $\overline{RTS}$ output low	0 = Normal 1 = Reset error flags in status register (FE, OE, PE)	0 = Normal 1 = Force break	0 = Disable 1 = Enable	Not used. Must be programmed to "1"	0 = Disable 1 = Enable

Table 8 Status Register (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
	Data Carrier Detect	Framing Error	Overrun Error	Parity Error	TxEMT/ DSCHG	RxRDY	TxRDY
Not used	0 = $\overline{DCD}$ input is high 1 = $\overline{DCD}$ input is low	0 = Normal 1 = Framing Error	0 = Normal 1 = Overrun Error	0 = Normal 1 = Parity Error	0 = Normal 1 = Change in $\overline{DCD}$ or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register busy

by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the reset error command, CR4.

Bit SR5 signifies that the received character was not framed by a stop bit; i.e., only the first stop bit is checked. If RHR = 0 when SR5 = 1, a break condition is present. The bit is reset when the receiver is disabled and when the reset error command is given.

SR6 reflects the condition of the DCD input. A low input sets the status bit and a high input clears it.

Absolute Maximum Ratings[1]

Item	Rating	Unit
Operating ambient temperature[2]	0 to + 70	°C
Storage temperature	−65 to + 150	°C
All voltages with respect to ground[3]	−0.5 to + 6.0	V

Electrical Characteristics

DC Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, Ta = 0 to +70°C unless otherwise noted)[4,5,6]

Item		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage					V	
V_{IL}	Low	−0.3	–	0.8		
V_{IH}	High	2.0	–	V_{CC}		
Output voltage					V	
V_{OL}	Low	–	–	0.4		I_{OL} = 2.2mA
V_{OH}[7]	High	2.4	–	–		I_{OH} = −400μA
I_{IL}	Input leakage current	−10	–	10	μA	V_{IN} = 0 to V_{CC}
3-state output leakage current					μA	
I_{LH}	Data bus high	–	–	10		V_O = 4.0V
I_{LL}	Data bus low	−10	–			V_O = 0.45V
I_{CC}	Power supply current	–	70	150	mA	
Capacitance					pF	
C_{IN}	Input	–	–	20		fc = 1MHz
C_{OUT}	Output	–	–	20		Unmeasured pins tied to ground
$C_{I/O}$	Input/Output	–	–	20		

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}*	4.75	5.0	5.25	V
Input voltage "High"	V_{IH}*	2.0	–	V_{CC}	V
Input voltage "Low"	V_{IL}*	−0.3	–	0.8	V
Operating ambient temperature	Topr	0	25	70	°C

* All voltage measurements are referenced to ground.

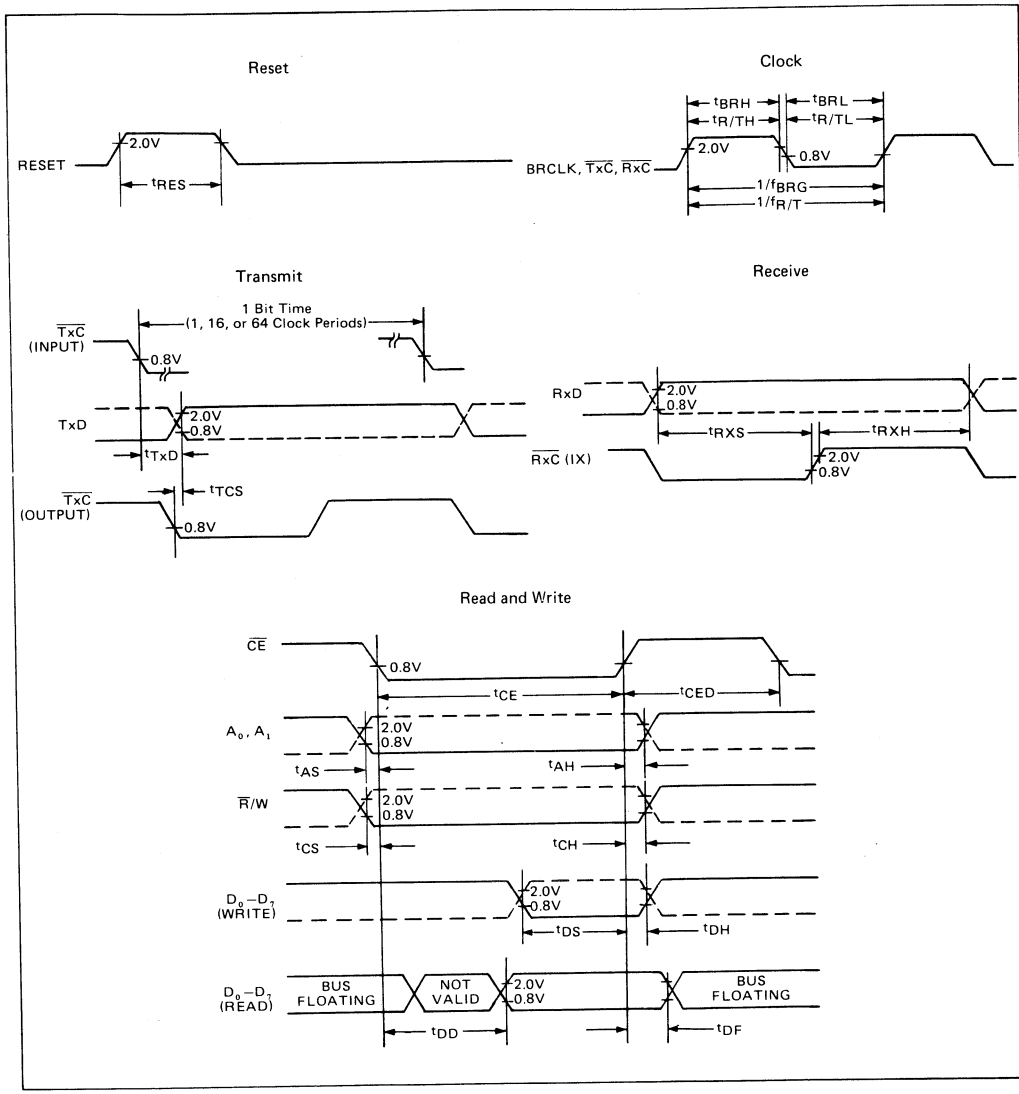
AC Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, Ta = 0 to 70°C unless otherwise noted)[4,5,6]

Item		Limits			Unit	Test Conditions
		Min	Typ	Max		
Pulse widht		1000			ns	
t_{RES}	Reset	250			ns	
t_{CE}	Chip enable	250			ns	
t_{CED}	CE to CE delay	600			ns	
Set-up and hold time					ns	
t_{AS}	Address set-up	10			ns	
t_{AH}	Address hold	10			ns	
t_{CS}	R/W control set-up	10			ns	
t_{CH}	R/W control hold	10			ns	
t_{DS}	Data set-up for write	150			ns	
t_{DH}	Data hold for write	10			ns	
t_{RXS}	Rx data set-up	300			ns	
t_{RXH}	Rx data hold	350			ns	
t_{DD}	Data delay time for read			200	ns	C_L = 150pF
t_{DF}	Data bus floating time for read			100	ns	C_L = 150pF
Input clock frequency					MHz	
f_{BRG}	Baud rate generator	1.0	3.6864	4.0		
$f_{R/T}$[10]	$\overline{TxC}$ or $\overline{RxC}$	–		1.0		
Clock state					ns	
t_{BRH}[9]	Baud rate high	90			ns	
t_{BRL}[9]	Baud rate low	90			ns	
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ high	480			ns	
$t_{R/TL}$[10]	$\overline{TxC}$ or $\overline{RxC}$ low	480			ns	
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$			650	ns	C_L = 150pF
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[8]		0		ns	C_L = 150pF

(Notes)

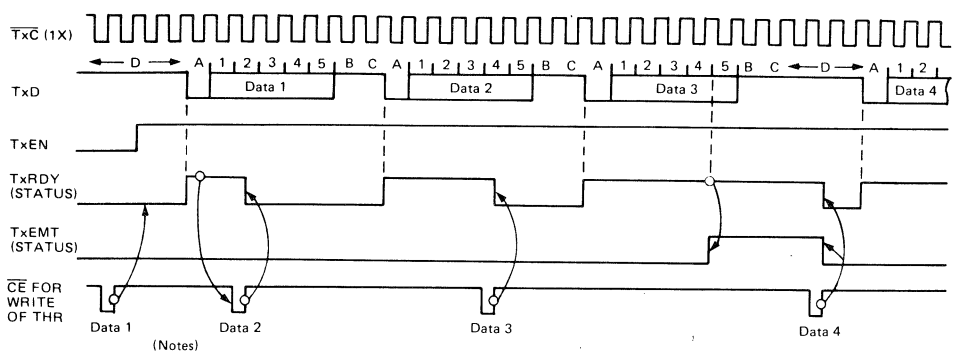
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on + 150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of 20ns maximum.
6. Typical values are at + 25°C, typical supply voltages and typical processing parameters.
7. $\overline{INTR}$ output is open drain.
8. Parameter applies when internal transmitter clock is used.
9. t_{BRH} and t_{BRL} measured at V_{IH} and V_{IL} respectively.
10. In asynchronous local loopback mode, using 1X clock, the following parameters apply:
    $f_{R/T}$ = 0.83MHz max
    $f_{R/TL}$ = 700ns min

Timing Diagrams



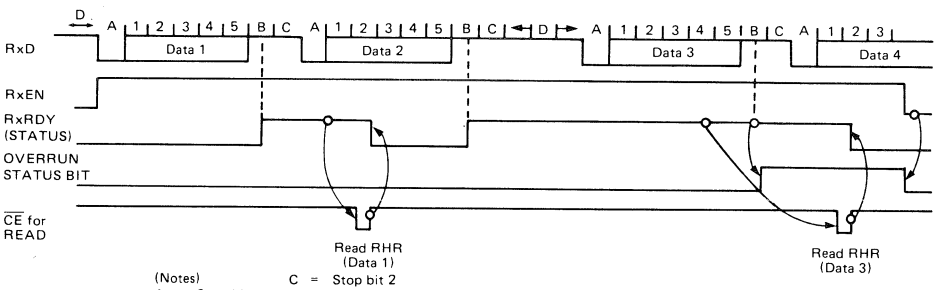
Timing Diagrams (Continued)

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits)



(Notes)
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit or, if parity is enabled at the beginning of the parity bit.

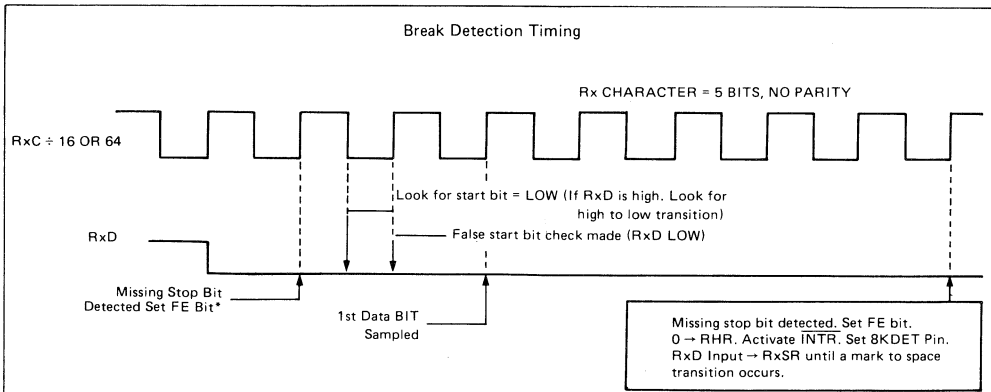
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits)



(Notes)
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
Only one stop bit is detected.

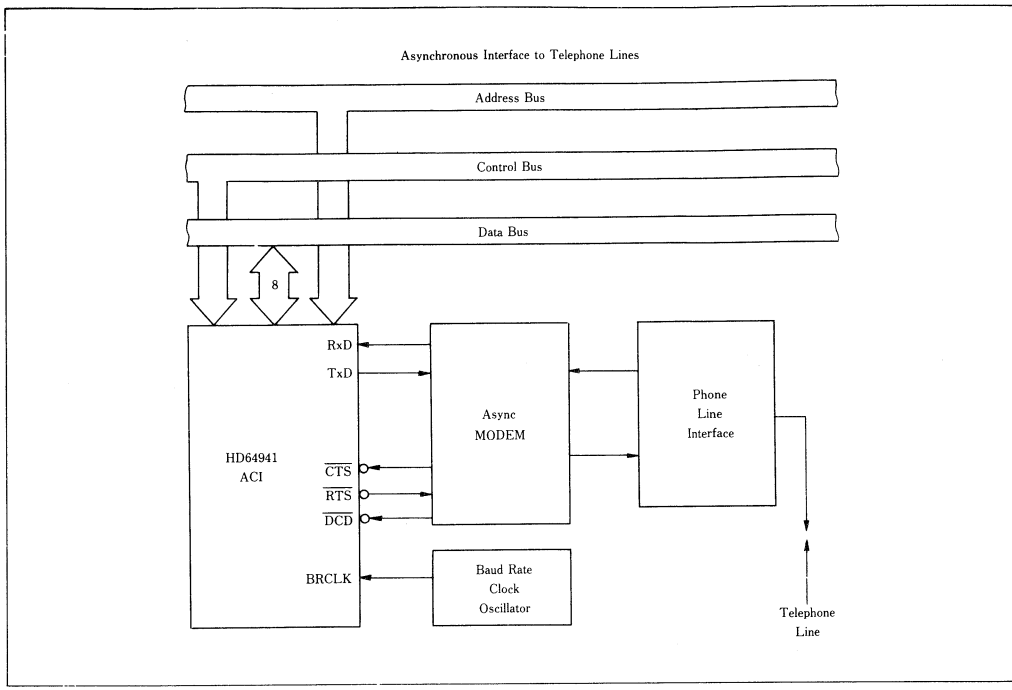
Timing Diagrams (Continued)

Break Detection Timing

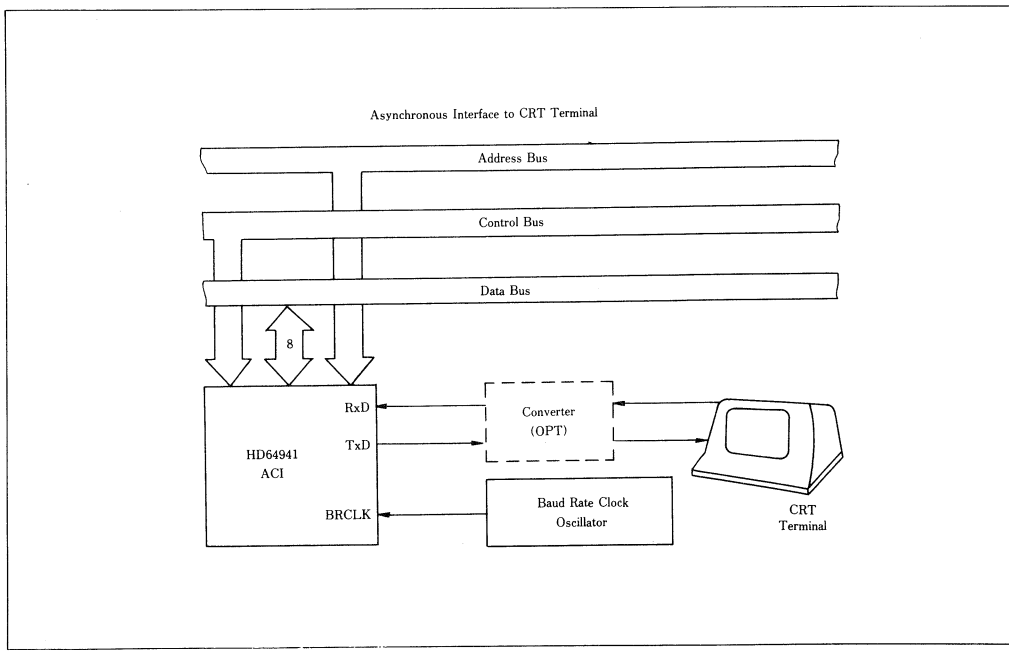


* If the stop bit is present, the start bit search will commence immediately.

Typical Applications



Typical Applications (Continued)

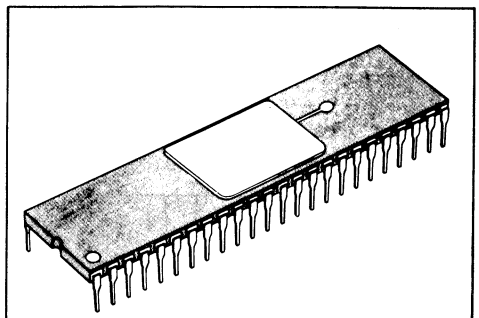


Dual Universal Serial Communications Controller (DUSCC)

Description

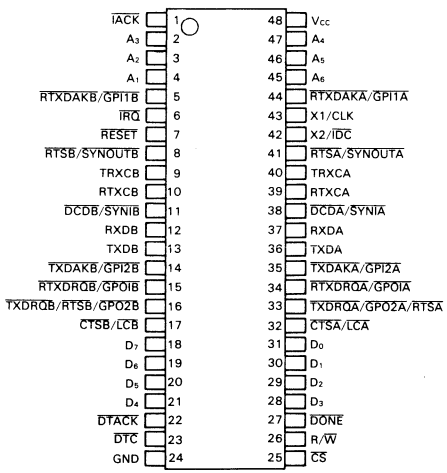
The Hitachi HD68562 dual universal serial communications controller is a MOS-LSI communication device with two independent, multiprotocol, full-duplex receiver/transmitter channels on chip. It supports bit-oriented and character-oriented as well as asynchronous protocols. The HD68562 interfaces to the 68000 microprocessor unit (MPU) via asynchronous bus control signals. It is capable of program-polled, interrupt-driven, block-move, or DMA data transfers.

The operating mode and data format of each channel are independent. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a bit rate generator (BRG), a parity/CRC generator/checker, and associated control circuits. The transmitter and receiver each contain a four-deep FIFO queue, reducing the chance of receiver overrun or transmitter underrun, and reducing the interrupt or DMA overhead. The DUSCC has two modem control inputs ($\overline{DCD}$ and $\overline{CTS}$) and three modem control outputs ($\overline{RTS}$ and two general purpose outputs). These inputs and outputs can be programmed for other functions as well as modem control.



(DC-48)

Pin Arrangement



(Top View)

Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - — Bit-oriented protocols (BOP): HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc
  - — Character-oriented protocols (COP): BISYNC, DDCMP, X.21
  - — ASYNC: 5-8 bits plus optional parity
- Four-character receiver and transmitter FIFOs
- Programmable bit rate for each receiver and transmitter selectable from:
  - — Internal bit rate generator: 16 fixed rates (50 baud to 38.4 k baud)
  - — Internal counter/timer: Programable (Up to 250 k baud)
  - — Internal digital phase-locked loop (Up to 250 k baud)
  - — External clock (Up to 4 M baud)
- DC to 4 MHz data rate
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full/half duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, wait, DMA
- DMA interface
  - — Compatible with Hitachi HD68450/HD63450 DMAC and other DMA controllers
  - — Half-or full-duplex operation
  - — Single or dual address data transfers
  - — Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - — Daisy chain option
  - — Vector output (fixed or modified by status)
  - — Programmable internal priorities
  - — Maskable interrupt conditions
- Multifunction programmable counter/timer (C/T)
  - — Bit-rate generator
  - — Event counter
  - — Count received or transmitted characters

  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD auto-enable for TX and RX
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5 V power supply

Pin Function

Table 1 shows the names and mnemonics for the pins of the DUSCC. Table 2 shows their state at reset.

Data Bus

D_0 -D_7 (Data Bus): Bit 0 of the bidirectional data bus is the LSB and bit 7 is the MSB. All data, command, and status transfers take place over this bus. The data bus is enabled when $\overline{CS}$ is low, during interrupt acknowledge cycles, and single-address DMA acknowlege cycles. Active high, three state.

Bus Control

A_1 -A_6 (Address): The address inputs specify which of the internal registers is being accessed for read/write operations. Active high.

R/$\overline{W}$ (Read/Write): Read/write input high indicates a read cycle and R/$\overline{W}$ low indicates a write cycle when a cycle is initiated by the $\overline{CS}$ input going low.

$\overline{CS}$ (Chip Select): When the $\overline{CS}$ input is low, it enables data transfers between the MPU and DUSCC on D_0 -D_7 , controlled by the R/$\overline{W}$ and A_1 - A_6 inputs. When $\overline{CS}$ is high, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single-address DMA transfers) and D_0 -D_7 are high-impedance. Active low.

$\overline{DTACK}$ (Data Transfer Acknowledge): The DUSCC asserts the $\overline{DTACK}$ output low on a write cycle when the data on the bus has been latched. It asserts $\overline{DTACK}$ on a read cycle or interrupt acknowledge cycle when valid data is on the bus. It negates $\overline{DTACK}$ when the $\overline{CS}$ or $\overline{IACK}$ input is negated indicating the completion of the cycle. It goes to high impedance state a short period after it is negated.

In single-address DMA mode, the $\overline{DTACK}$ operates the same except that it is negated when the completion of a cycle is indicated by the assertion of $\overline{DTC}$ or the negation of the DMA acknowledge inputs (whichever comes first).

When negated, $\overline{DTACK}$ is an open-drain output, and requires an external pull-up resistor. Active low, three-state.

Reset

$\overline{RESET}$ (Reset): When the reset input is asserted low, it resets the transmitters and receivers, and resets the registers shown in table 2. Reset is asynchronous, that is, it requires no clock. Active low.

Interrupt Control

$\overline{IRQ}$ (Interrupt Request): The DUSCC asserts the interrupt request output on any enabled interrupting condition. The MPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle, which causes the DUSCC to output an interrupt vector on the data bus. Active low, open-drain.

$\overline{IACK}$ (Interrupt Acknowledge): When the interrupt acknowledge input is asserted low, the DUSCC places the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserts $\overline{DTACK}$. If there is no active interrupt pending, the DUSCC does not assert $\overline{DTACK}$. Active low.

$\overline{IDC}$ (Interrupt Daisy Chain): The interrupt daisy chain output can be programmed to propagate the $\overline{IACK}$ to lower priority devices if there is no active interrupt pending. Active low.

Clock

X1, X2 (Crystal): Connect the timing crystal between X1 and X2, if a crystal is used.

CLK (Clock): If a crystal is not used, supply an external clock signal to this input.

Synchronizing Control

RTXCA, RTXCB (Receiver/Transmitter Clock, A and B)

As inputs, RTXCA and RTXCB can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, they can output the signal from the counter/timer, the transmitter shift clock (1×), or the receiver sampling clock (1×). The maximum external RTXC frequency is 4 MHz.

TRXCA, TRXCB (Transmitter/Receiver Clock, A and B): As inputs, TRXCA and TRXCB can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As outputs, they can output the signal from the counter/timer, the DPLL, the transmitter shift clock (1×), the transmitter BRG clock (16×), the receiver BRG clock (16×), or the internal system clock (X1, X2). The maximum external TRXC frequency is 4 MHz.

$\overline{LCA}$, $\overline{LCB}$ (Loop Control Outputs, A and B): In the BOP loop mode (SDLC loop mode), these outputs are asserted and negated by DUSCC commands. $\overline{LCA}$ and $\overline{LCB}$ can control external loop hardware, to bring the DUSCC on-loop and off-loop without disturbing loop operation.

Table 1. Pin Description

Symbol	Pin No.	I/O	Name
$\overline{IACK}$	1	I	Interrupt acknowledge
A_1 -A_6	4-2, 45-47	I	Address bus
$\overline{RTXDAKB}$/ $\overline{GPI1B}$	5	I	Receiver/transmitter DMA acknowledge B/ General purpose input
$\overline{IRQ}$	6	O	Interrupt request
$\overline{RESET}$	7	I	Master reset
$\overline{RTSB}$/ $\overline{SYNOUTB}$	8	O	Request to send B/ Sync detect B
TRXCB	9	I/O	Transmitter/receiver clock B
RTXCB	10	I/O	Receiver/transmitter clock B
$\overline{DCDB}$/ $\overline{SYNIB}$	11	I	Data carrier detect B/ External sync B
RXDB	12	I	Receiver serial data input B
TXDB	13	O	Transmitter serial data output B
$\overline{TXDAKB}$/ $\overline{GPI2B}$	14	I	Transmitter DMA acknowledge B/ General purpose input
$\overline{RTXDRQB}$/ $\overline{GPO1B}$	15	O	Receiver/transmitter DMA service request B/ General purpose output
$\overline{TXDRQB}$/ $\overline{GPO2B}$/ $\overline{RTSB}$	16	O	Transmitter DMA service request B/ General purpose output/ Request to send B
$\overline{CTSB}$/$\overline{LCB}$	17	I/O	Clear to send B/Loop control output B
D_0 -D_7	31-28, 21-18	I/O	Data bus
$\overline{DTACK}$	22	O	Data transfer acknowledge
$\overline{DTC}$	23	I	Device transfer complete
GND	24		Ground
$\overline{CS}$	25	I	Chip select
R/$\overline{W}$	26	I	Read/Write
$\overline{DONE}$	27	I/O	DMA done
$\overline{CTSA}$/$\overline{LCA}$	32	I/O	Clear to send A/Loop control output A
$\overline{TXDRQA}$/ $\overline{GPO2A}$/ $\overline{RTSA}$	33	O	Transmitter DMA service request A/General purpose output/Request to send A
$\overline{RTXDRQA}$/ $\overline{GPO1A}$	34	O	Receiver/transmitter DMA service request A/ General purpose output
$\overline{TXDAKA}$/ $\overline{GPI2A}$	35	I	Transmitter DMA acknowledge A/ General purpose input
TXDA	36	O	Transmitter serial data output A
RXDA	37	I	Receiver serial data input A
$\overline{DCDA}$/ $\overline{SYNIA}$	38	I	Data carrier detect A/ External sync A
RTXCA	39	I/O	Receiver/transmitter clock A
TRXCA	40	I/O	Transmitter/receiver clock A
$\overline{RTSA}$/ $\overline{SYNOUTA}$	41	O	Request to send A/ Sync detect A
X2/$\overline{IDC}$	42	I/O	Crystal/Interrupt daisy chain
X1/CLK	43	I	Crystal/External clock
$\overline{RTXDAKA}$/ $\overline{GPI1A}$	44	I	Reciver/transmitter DMA acknowlege A/ General purpose input
V_{CC}	48		+5 V power supply

$\overline{\text{SYNIA}}$, $\overline{\text{SYNIB}}$ (External Sync Input, A and B): $\overline{\text{SYNIA}}$ and $\overline{\text{SYNIB}}$ inputs are used in COP and BOP modes to obtain character synchronization without receipt of a SYN or FLAG character. This method can be used by disk or tape controllers, or for the optional byte timing lead in X.21. Active low.

$\overline{\text{SYNOUTA}}$, $\overline{\text{SYNOUTB}}$ (Sync Detect, A and B): The $\overline{\text{SYNOUT}}$ outputs are asserted one bit time after the receiver detects the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes). Active low.

Receiver/Transmitter Serial Data

RXDA, RXDB (Receiver Serial Data Input, A and B): The first bit received is the least significant bit. If the external receiver clock is specified for the channel, the input is sampled at the rising edge of the clock.

TXDA, TXDB (Transmitter Serial Data Output, A and B): The least significant bit is transmitted first. The TXD outputs are held in the marking (high) state when the transmitter is disabled or when the channel is operating in local loopback mode. If an external transmitter clock is specified for the channel, the data is shifted out on

Table 2. Reset State of Pins

Symbol	Pin No.	I/O	State	Selected Function
$\overline{\text{IACK}}$	1	I	–	–
A_1 -A_6	4-2, 45-47	I	–	–
$\overline{\text{RTXDAKB}}$/ $\overline{\text{GPI1B}}$	5	I	–	$\overline{\text{RTXDAKB}}$
$\overline{\text{IRQ}}$	6	O	High Impedance	–
$\overline{\text{RESET}}$	7	I	–	–
$\overline{\text{RTSB}}$/ $\overline{\text{SYNOUTB}}$	8	O	High	$\overline{\text{SYNOUTB}}$
TRXCB	9	I/O	Low	–
RTXCB	10	I/O	Low	–
$\overline{\text{DCDB}}$/ $\overline{\text{SYNIB}}$	11	I	–	Depend on RPR
RXDB	12	I	–	–
TXDB	13	O	High	–
$\overline{\text{TXDAKB}}$/ $\overline{\text{GPI2B}}$	14	I	–	$\overline{\text{TXDAKB}}$
$\overline{\text{RTXDRQB}}$/ $\overline{\text{GPO1B}}$	15	O	High	$\overline{\text{RTXDRQB}}$
$\overline{\text{TXDRQB}}$/ $\overline{\text{GPO2B}}$/ $\overline{\text{RTSB}}$	16	O	High	$\overline{\text{GPO2B}}$
$\overline{\text{CTSB}}$/$\overline{\text{LCB}}$	17	I/O	High	$\overline{\text{CTSB}}$
D_0 -D_7	31-28, 21-18	I/O	–	–
$\overline{\text{DTACK}}$	22	O	High Impedance	–
$\overline{\text{DTC}}$	23	I	–	–
GND	24		Low	–
$\overline{\text{CS}}$	25	I	–	–
R/$\overline{\text{W}}$	26	I	–	–
$\overline{\text{DONE}}$	27	I/O	High Impedance	–
$\overline{\text{CTSA}}$/$\overline{\text{LCA}}$	32	I/O	High	$\overline{\text{CTSA}}$
$\overline{\text{TXDRQA}}$/ $\overline{\text{GPO2A}}$/ $\overline{\text{RTSA}}$	33	O	High	$\overline{\text{GPO2A}}$
$\overline{\text{RTXDRQA}}$/ $\overline{\text{GPO1A}}$	34	O	High	$\overline{\text{RTXDRQA}}$
$\overline{\text{TXDAKA}}$/ $\overline{\text{GPI2A}}$	35	I	–	$\overline{\text{TXDAKA}}$
TXDA	36	O	High	–
RXDA	37	I	–	
$\overline{\text{DCDA}}$/ $\overline{\text{SYNIA}}$	38	I	–	Depend on RPR
RTXCA	39	I/O	–	–
TRXCA	40	I/O	–	–
$\overline{\text{RTSA}}$/ $\overline{\text{SYNOUTA}}$	41	O	High	$\overline{\text{SYNOUTA}}$
X2/$\overline{\text{IDC}}$	42	I/O	–	X2
X1/CLK	43	I	–	
$\overline{\text{RTXDAKA}}$/ $\overline{\text{GPI1A}}$	44	I	–	$\overline{\text{RTXDAKA}}$
V_{CC}	48		High	–

the falling edge of the clock.

Modem Control

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$ (Clear to Send, A and B): The $\overline{\text{CTS}}$ signals can be programmed to enable the transmitter. The DUSCC detects logic level transitions on the $\overline{\text{CTS}}$ inputs and can generate an interrupt when a transition occurs. Active low.

$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$ (Data Carrier Detected, A and B) : The $\overline{\text{DCD}}$ inputs can be used as an enable for the receiver or as a general purpose input. The DUSCC detects logic level transitions on the $\overline{\text{DCD}}$ inputs and can generate an interrupt when a transition occurs. Active low.

DMA Control

$\overline{\text{RTXDRQA}}$, $\overline{\text{RTXDRQB}}$ (Receiver/Transmitter DMA Service Request, A and B): For half-duplex DMA operation, the $\overline{\text{RTXDRQ}}$ outputs indicate to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, $\overline{\text{RTXDRQ}}$ indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, these pins are general purpose outputs.

$\overline{\text{TXDRQA}}$, $\overline{\text{TXDRQB}}$ (Transmitter DMA Service Request, A and B): For full-duplex DMA operation, the $\overline{\text{TXDRQ}}$ outputs indicate to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, these pins are request-to-send or general purpose outputs. Active low.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$ (Request to Send, A and B): $\overline{\text{RTSA}}$ and $\overline{\text{RTSB}}$ are the request-to-send modem control outputs. They can be asserted and negated under program control. Active low.

$\overline{\text{RTXDAKA}}$, $\overline{\text{RTXDAKB}}$ (Receiver/Transmitter DMA Acknowledge, A and B): For half-duplex, single-address DMA operation, the $\overline{\text{RTXDAK}}$ inputs indicate to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full-duplex, single-address DMA operation, $\overline{\text{RTXDAK}}$ indicates that the DMA controller has acquired the bus and the requested read receiver FIFO bus cycle is beginning. When not in the single-address DMA mode, these pins can be used as general purpose inputs. Active low.

$\overline{\text{TXDAKA}}$, $\overline{\text{TXDAKB}}$ (Transmitter DMA Acknowledge, A and B): For full-duplex, single-address DMA operation, the $\overline{\text{TXDAK}}$ inputs indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. When not in the full-duplex, single-address DMA mode, these pins can be used as general purpose inputs. Active low.

$\overline{\text{DTC}}$ (Device Transfer Complete): The DMA controller asserts the $\overline{\text{DTC}}$ input to indicate that the requested data transfer is complete. Active low.

$\overline{\text{DONE}}$ (Done): As an input, $\overline{\text{DONE}}$ low indicates a normal termination of DMA transmission. As an input it indicates that the DMA controller has finished the transfer. Active low.

General Purpose Control

$\overline{\text{GPO1A}}$, $\overline{\text{GPO1B}}$, $\overline{\text{GPO2A}}$, $\overline{\text{GPO2B}}$ (General Purpose Outputs): The $\overline{\text{GPO}}$ pins can be asserted or negated by the program, so they can be used as general purpose outputs when they are not being used for other functions. The $\overline{\text{GPO1}}$ pins are also used as $\overline{\text{RTXDRQ}}$ outputs in DMA mode. The $\overline{\text{GPO2}}$ pins are also used as $\overline{\text{TXDRQ}}$ and $\overline{\text{RTS}}$ outputs in full-duplex DMA mode.

$\overline{\text{GPI1A}}$, $\overline{\text{GPI1B}}$, $\overline{\text{GPI2A}}$, $\overline{\text{GPI2B}}$ (General Purpose Inputs): The $\overline{\text{GPI}}$ pins can be read by the program, so they can be used as general purpose inputs when they are not being used for other functions. The $\overline{\text{GPI1}}$ pins are also used as $\overline{\text{RTXDAK}}$ pins in single-address DMA mode . The $\overline{\text{GPI2}}$ pins are also used as $\overline{\text{TXDAK}}$ pins in full-duplex, single-address DMA mode.

Power Supply

V_{CC} (Power Supply): + 5 V ± 5 % power supply.

GND (Ground): Signal and power ground.

Block Diagram

The DUSCC consists of interface and operational controls, a timing section, and two receivers and transmitters. See figure 1.

Registers

The DUSCC is programmed by writing control words into the control and command registers. Operational status information is provided by the status registers, which can be read by the MPU. The contents of some control registers are initialized to zero on reset. Excercise caution if the contents of a register are changed during an operation. Certain changes may cause malfunctions. For example, changing the channel mode at an inappropriate time may cause transmission or reception of an incorrect character. In general, only change the contents of a register which controls transmitter, receiver, or counter/timer function when it is disabled.

Table 3 and figure 2 show the DUSCC addressable registers.

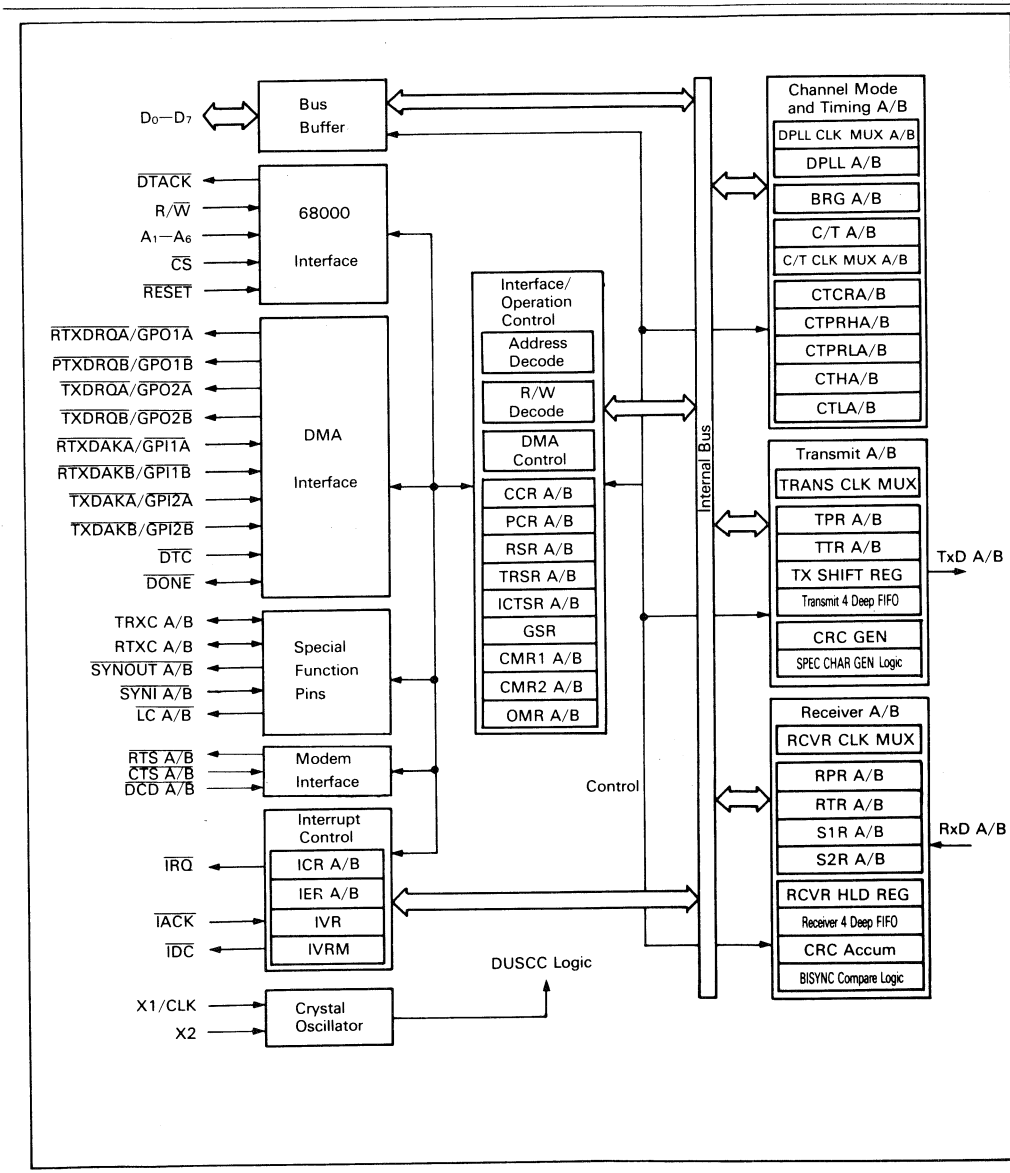


Figure 1. Block Diagram

Table 3. Control Registers

Address	Acronym	Register Name	R/W	Function
C00000 C00001	CMR1 CMR2	Channel Mode Register 1 Channel Mode Register 2	R/W R/W	Select channel protocol, transmission mode, message format, checking sequence, and overall system interface.
C00010 C00011	S1R S2R	SYN 1/Secondary Address 1 Register SYN 2/Secondary Address 2 Register	R/W R/W	Holds bit pattern which is compared with received characters (SYN, address, etc)
C00100 C00101	TPR TTR	Transmitter Parameter Register Transmitter Timing Register	R/W R/W	Define transmitter operation.
C00110 C00111	RPR RTR	Receiver Parameter Register Receiver Timing Register	R/W R/W	Define receiver operation.
C01000 C01001	CTPRH CTPRL	Counter/Timer Preset Register High Counter/Timer Reset Register Low	R/W R/W	High and low bytes of value loaded into counter/timer
C01010	CTCR	Counter/Timer Control Register	R/W	Selects counter/timer clock source, prescaling factor, and operating mode
C01011	OMR	Output and Miscellaneous Register	R/W	Controls point at which FIFO is read.
C01100 C01101	CTH CTL	Counter/Timer High Counter/Timer Low	R R	High and low bytes of current value in counter/timer
C01110	PCR	Pin Configuration Register	R/W	Programs multifunction pins.
C01111	CCR	Channel Command Register	R/W	Accepts DUSCC commands from MPU
C100nn	TXFIFO	Transmitter FIFO	W	48-bit holding registers that accept data from the system bus
C101nn	RXFIFO	Receiver FIFO	R	48bit holding registers with appended status bits, loaded with received characters as they are assembled
C11000 C11001 C11010	RSR TRSR ICTSR	Receiver Status Register Transmitter/Receiver Status Register Input and Counter/Timer Status Register	R/W R/W R/W	Precisely indicate controller's status.
X11011	GSR	General Status Register	R/W	Summary status for both channels.
C11100 011111	IER ICR	Interrupt Enable Register Interrupt Control Register	R/W R/W	Determine interrupt process.
011110 111110	IVR IVRM	Interrupt Vector Register-Unmodified Interrupt Vector Register-Modified	R/W R	Contents are output on data bus when DUSCC isssues interrupt request.

Note: C = 0 for channel A,C = 1 for channel B
X = Don't care; register may be accessed as either channel
nn = 0-3; FIFO's are addressable at four adjacent addresses so they can be addressed as byte/word/long word by 68000 MOVEP instruction

Table 4. Register State After Reset

Register	State
CMR1	00H
CMR2	00H
S1R	Not affected
S2R	Not affected
TPR	00H
TTR	Not affected
CTPRH	Not affected
CTPRL	Not affected
CTCR	00H
OMR	00H
CTH	Not affected
CTL	Not affected
PCR	00H
CCR	Not affected
TXFIFO	Not affected
RXFIFO	Not affected
RSR	00H (note)
TRSR	00H (note)
ICTSR	$ICTSR_4$ -$ICTSR_6$ flags reset to 0. Other bits not affected (note)
GSR	00H (note)
IER	00H
ICR	00H
IVR	0FH
IVRM	0FH

Note: Write to this register may affect reset status.

Channel Mode Register 1 (CMR1A, CMR1B)

7	6	5	4	3	2	1	0
Data Encoding		Extended Control (BOP)	Address Mode (BOP)		Channel Protocol Mode		
00-NRZ (DPLL=NRZI) Manchester (DPLL=FM) 01-NRZI 10-FM0 11-FM1		0-1 octet control 1-2 octet control	00-8bit addr 01-extended addr 10-16 bit addr 11-16 bit addr with group		000-BOP primary 001-BOP secondary 010-BOP loop 011-BOP loop, no addr comp		
		Parity	Parity Mode (COP/ASYNC)		100-COP dual SYN 101-COP dual SYN (BISYNC) 110-COP single SYN 111-ASYNC		
		0-even 1-odd (for Forced Parity: 0-0 1-1) (See Note)	00-no parity 01-reserved 10-with parity 11-force parity to $CMR1_5$				

Note: In BISYNC mode, 0 = EBCDIC, 1 = 8-bit ASCII

Channel Mode Register 2 (CMR2A, CMR2B)

7	6	5	4	3	2	1	0
Channel Connection		Data Transfer Interface			FCS Sequence Select		
00-normal 01-auto echo 10-local loop 11-reserved		000-half-dup, sing-addr DMA 001-half-dup, dual-addr DMA 010-full-dup, sing-addr DMA 011-full-dup, dual-addr DMA 100-wait on Rx only 101-wait on Tx only 110-wait on Rx or Tx 111-polled or interrupt			000-none 001-reserved 010-LRC 8 preset 0s 011-LRC 8 preset 1s 100-CRC 16 preset 0s 101-CRC 16 preset 1s 110-CRC CCITT preset 0s 111-CRC CCITT preset 1s		

SYN1/Secondary Address Register 1 (S1RA, S1RB)

7	6	5	4	3	2	1	0
ASYNC-character to compare (5-8 bits) COP-SYN1 (5-8bits) BOP-first address octet							

SYN2/Secondary Address Register 2 (S2RA, S2RB)

7	6	5	4	3	2	1	0
ASYNC-not used COP (dual sync)-SYN2 (5-8 bits) BOP (secondary address)-second address octet							

Figure 2. Register Format

Transmitter Parameter Register (TPRA, TPRB)

7	6	5	4	3	2	1	0
ASYNC				TX $\overline{\text{RTS}}$ Control	$\overline{\text{CTS}}$ Enable TX	TX Character Length	
Stop Bits per Character				0-no 1-yes	0-disable 1-enable	00-5 bits 01-6 bits 10-7 bits 11-8 bits	
	5 Bits/Char	6-8 Bits/Char					
0000-	1-1/16	9/16					
0001-	1-2/16	10/16					
0010-	1-3/16	11/16					
0011-	1-4/16	12/16					
0100-	1-5/16	13/16					
0101-	1-6/16	14/16					
0110-	1-7/16	15/16					
0111-	1-8/16	1					
1000-	1-9/16	1-9/16					
1001-	1-10/16	1-10/16					
1010-	1-11/16	1-11/16					
1011-	1-12/16	1-12/16					
1100-	1-13/16	1-13/16					
1101-	1-14/16	1-14/16					
1110-	1-15/16	1-15/16					
1111-	2	2					
COP							
Underrun Control		Idle	TEOM on Zero Cnt or Done				
00-FCS-idle 01-reserved 10-MARKs 11-SYNs		0-MARKs 1-SYNs	0-no 1-yes				
BOP							
Underrun Control		Idle	TEOM on Zero Cnt or Done				
00-FCS-FLAG-idle 01-reserved 10-ABORT-MARKs 11-ABORT-FLAGs		0-MARKs 1-FLAGs	0-no 1-yes				

Transmitter Timing Register (TTRA, TTRB)

7	6	5	4	3	2	1	0
External Source	Transmitter Clock Select			Bit Rate Select (Baud)			
0-RTXC 1-TRXC	000-1x external 001-16x external 010-DPLL 011-BRG 100-2x other channel C/T 101-32x other channel C/T 110-2x own channel C/T 111-32x own channel C/T			0000-50 0001-75 0010-110 0011-134.5 0100-150 0101-200 0110-300 0111-600 (14.7456 MHz crystal)		1000-1050 1001-1200 1010-2000 1011-2400 1100-4800 1101-9600 1110-19.2k 1111-38.4k	

Figure 2. Register Format (cont)

Receiver Parameter Register (RPRA, RPRB)

7	6	5	4	3	2	1	0
ASYNC					$\overline{DCD}$ Enable RX	RX Character Length	
Reserved			RX $\overline{RTS}$ Control	Strip Parity	0-disable 1-enable	00-5 bits 01-6 bits 10-7 bits 11-8 bits	
			0-no 1-yes	0-no 1-yes			
COP							
SYN Strip	FCS to FIFO	Auto Hunt & Pad Chk	Ext Sync	Strip Parity			
0-leading 1-all	0-no 1-yes	0-no 1-yes	0-no 1-yes	0-no 1-yes			
BOP							
Reserved	FCS to FIFO	Overrun Mode	Reserved	All Parity Address			
	0-no 1-yes	0-hunt 1-cont		0-no 1-yes			

Receiver Timing Register (RTRA, RTRB)

7	6	5	4	3	2	1	0
External Source	Receiver Clock Select			Bit Rate Select (Baud)			
0-RTXC 1-TRXC	000-1x external 001-16x external 010-BRG } ASYNC 011-C/T of channel 100-DPLL, source=64x X1/CLK 101-DPLL, source=32x ext 110-DPLL, source=32x BRG 111-DPLL, source=32x C/T			0000-50 0001-75 0010-110 0011-134.5 0100-150 0101-200 0110-300 0111-600		1000-1050 1001-1200 1010-2000 1011-2400 1100-4800 1101-9600 1110-19.2k 1111-38.4k	
				(14.7456 MHz crystal)			

Counter/ Timer Preset Register High (CTPRHA, CTPRHB)

7	6	5	4	3	2	1	0
Most significant 8 bits of C/T preset value							

Counter/Timer Preset Register Low (CTPRLA, CTPRLB)

7	6	5	4	3	2	1	0
Least siginificant 8 bits of C/T preset value (minimum value = 2)							

Figure 2. Register Format (cont)

Counter/Timer Control Register (CTCRA, CTCRB)

7	6	5	4	3	2	1	0
Zero Detect Interrupt	Zero Detect Control	Output Control	Prescaler		Clock Source		
0-disable 1-enable	0-preset 1-cont from FFFF	0-square 1-pulse	00- ÷ 1 01- ÷ 16 10- ÷ 32 11- ÷ 64		000-RTXC pin 001-TRXC pin 010-X1/CLK divided by 4 011-X1/CLK divided by 4 gated by RXD 100-Rx BRG 101-Tx BRG 110-Rx characters 111-Tx characters		

Output and Miscellaneous Register (OMRA, OMRB)

7	6	5	4	3	2	1	0
TX Residual Character Length			TXRDY Activate	RXRDY Activate	GPO2	GPO1	RTS
000-1 bit 001-2 bits 010-3 bits 011-4 bits 100-5 bits 101-6 bits 110-7 bits 111-same as TPR1, TPR0			0-FIFO not full 1-FIFO empty	0-FIFO not empty 1-FIFO full	0-0 1-1	0-0 1-1	0-0 1-1

Counter/Timer High (CTHA, CTHB)

7	6	5	4	3	2	1	0
Most significant 8 bits of C/T							

Note: Stop C/T when reading CTH

Counter/Timer Low (CTLA, CTLB)

7	6	5	4	3	2	1	0
Least significant 8 bits of C/T							

Note: Stop C/T when reading CTL

Figure 2. Register Format (cont)

Pin Configuration Register (PCRA, PCRB)

7	6	5	4	3	2	1	0
X2/$\overline{IDC}$	$\overline{GPO2}$/$\overline{RTS}$	SYNOUT/ $\overline{RTS}$	RTXC		TRXC		
0-X2 1-$\overline{IDC}$ (PCRA only)	0-$\overline{GPO2}$ 1-$\overline{RTS}$	0-$\overline{SYNOUT}$ 1-$\overline{RTS}$	00-input 01-C/T 10-TXCLK 1x 11-RXCLK 1x		000-input 001-XTAL/2 010-DPLL 011-C/T	100-TXCLK 16x 101-RXCLK 16x 110-TXCLK 1x 111-TXCLK 1x	

Channel Command Register (CCRA, CCRB)

7	6	5	4	3	2	1	0
00-transmitter command		Don't care		Transmitter command			
				0000-reset Tx 0001-reset TxCRC (FIFO'ed command) 0010-enable Tx 0011-disable Tx 0100-transmit SOM (TSOM) 0101-transmit SOM with PAD (TSOMP) 0110-transmit EOM (TEOM) (FIFO'ed cmd) 0111-transmit ABORT/BREAK (TABRK) 1000-transmit DLE (FIFO'ed command) 1001-go active on poll 1010-reset go active on poll 1011-go on loop 1100-go off loop 1101-exclude from CRC (FIFO'ed command)			
01-receiver command		Don't care		Receiver command			
				0000-reset Rx 0001-reserved 0010-enable Rx 0011-disable Rx			
10-C/T command		Don't care		C/T command			
				0000-start 0001-stop 0010-preset to FFFF 0011-preset from CTPRH/CTPRL			
11-DPLL command		Don't care		DPLL command			
				0000-enter search mode 0001-disable DPLL 0010-set FM mode 0011-set NRZI mode 0100-reserved for test 0101-reserved for test			

Figure 2. Register Format (cont)

Receiver Status Register (RSRA, RSRB)

7	6	5	4	3	2	1	0
ASYNC							
Character Compare (Note 1)	RTS Negated	Overrun Error	Reserved	BRK End Detect	BRK Start Detect	Framing Error (Note 1)	Parity Error (Note 1)
COP							
EOM Detect (Note 1,2)	Pad Error (Note 2)	Overrun Error	Reserved	Reserved	SYN Detect	CRC Error (Note 1)	Parity Error (Note 1)
BOP							
EOM Detect (Note 1)	Abort Detect	Overrun Error	Short Frame Det	Idle Detect	Flag Detect	CRC Error (Note 1)	RCL Not Zero (Note 1,4)
BOP Loop							
EOM Detect (Note 1)	Abort/ EOP Detect	Overrun Error	Short Frame Det	Turn-Around Detect	Flag Detect	CRC Error (Note 1)	RCL Not Zero (Note 1,4)

Note: 1: Status bit is in RXFIFO
Note: 2: COP, BISYNC mode only
Note: 3: Bit 7 indicates character count complete in all modes
Note: 4: RCL = Receive character length

Transmitter and Receiver Status Register (TRSRA, TRSRB)

7	6	5	4	3	2	1	0
ASYNC							
Transmit Empty	CTS Underrun	Reserved	Send Break Ack	DPLL Error	Reserved	Reserved	Reserved
COP							
Transmit Empty	CTS Underrun	Frame Complete	Send SOM Ack	DPLL Error	Reserved	RxHunt mode	RxXPNT mode
BOP							
Transmit Empty	CTS Underrun	Frame Complete	Send SOM Abort Ack	DPLL Error	Residual RX Character Length		
	BOP Loop				000-0 bits	100-4 bits	
	Loop Sending				001-1 bit	101-5 bits	
					010-2 bits	110-6 bits	
					011-3 bits	111-7 bits	

Figure 2. Register Format (Cont)

Input and Counter/Timer Status Register (ICTSRA, ICTSRB)

7	6	5	4	3	2	1	0
C/T Running	C/T Zero Count	Delta $\overline{DCD}$	Delta $\overline{CTS}/\overline{LC}$	$\overline{DCD}$	$\overline{CTS}/\overline{LC}$	$\overline{GPI2}$	$\overline{GPI1}$

General Status Register (GSR)

7	6	5	4	3	2	1	0
Channel B				Channel A			
External or C/T Status	RX/TX Status	TXRDY	RXRDY	External or C/T Status	RX/TX Status	TXRDY	RXRDY

Interrupt Enable Register (IERA, IERB)

7	6	5	4	3	2	1	0
$\overline{DCD}/\overline{CTS}$	TXRDY	TRSR7, TRSR3	RXRDY	RSR7, RSR6	RSR5, RSR4	RSR3, RSR2	RSR1, RSR0
0-no 1-yes	0-no 1-yes	0-no 1-yes	0-no 1-yes	0-no 1-yes	0-no 1-yes	0-no 1-yes	0-no 1-yes

Interrupt Control Register (ICR)

7	6	5	4	3	2	1	0
A/B Interrupt Priority		Vector Mode		Bits to Modify	Vector Includes Status	Master Interrupt Enable A	Master Interrupt Enable B
00-channel A 01-interleaved A 10-channel B 11-interleaved B		00-vectored 01-vectored 10-vectored 11-nonvectored		0-[2-0] 1-[4-2]	0-no 1-yes	0-disable 1-enable	0-disable 1-enable

Interrupt Vector Register and Interrupt Vector Modified Register (IVR, IVRM)

7	6	5	4	3	2	1	0
8-bit interrupt vector							

Figure 2. Register Format (cont)

Function Description

Operating Mode

As normal mode, the transmitter and receiver operate independently in either half or full duplex, controlled by the respective enable commands. In half duplex mode, data is transferred alternating between two stations. On one-way-at-a-time. In full duplex mode, simultaneous data transmitting and reception is possible.
In automatic echo mode, automatically retransmits the received data with a half-bit time delay (ASYNC, 16X clock mode) or a one-bit time delay (all other modes).
In local loopback mode, the transmitter output is internally connected to the receiver input. The TXD output is held high, and the RXD input is ignored.

Modes of Operation

The DUSCC operates in ASYNC. COP and BOP modes. Data formats for these modes are defined according to the each protocols.

Asynchronous Mode Features
- 5 to 8 bit character lengths
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16 bit increments.
- 1x or 16x receive and transmit clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2 bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match

Character Oriented Protocol Features
- 5 to 8 bit character lengths
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection
- BISYNC features
  - EBCDIC or ASCII header, text and control messages

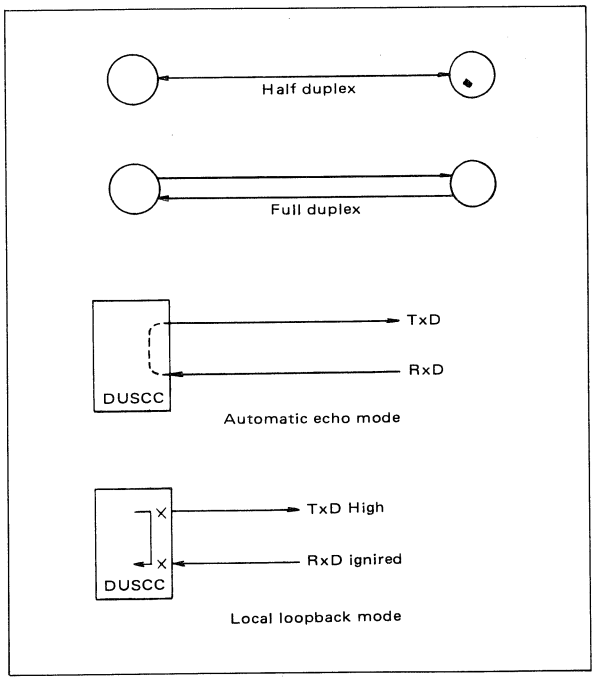


Figure 3. Operating Mode

- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Automatic transparency mode switching
- Automatic hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit Oriented Protocol Features

- Detection and transmission of residual character 0-7 bits
- Automatic switch to programmed character length for 1 field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs.
- ABORT, ABORT-FLAGs, or FSC-FLAGs line fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single or dual octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

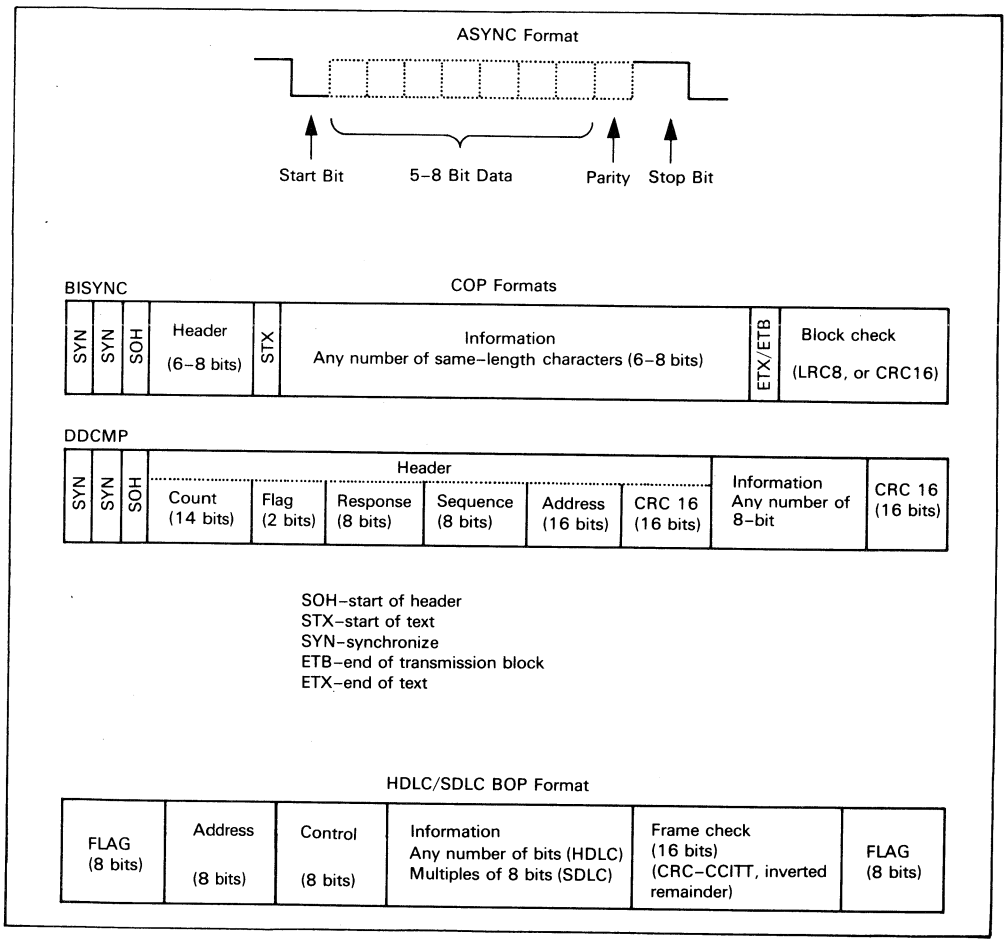


Figure 4. Data Formats

Error detection

The DUSCC sets status bits on status registers (RSR, TRSR) and shows the error to CPU when errors are occurred.

Parity Error (ASYNC/COP): The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated.

Framing Error (ASYNC): At the first stop bit position the RxD input was in the low (space) state.

CRC Error (COP/BOP): This is set upon receipt of the FCS byte(s), if any, to indicate that the received FCS was in error.

Overrun Error (All modes): A new character was received while the receive FIFO was full and a character was already waiting in the receive shift register to be transferred to the FIFO. The DUSCC protects the five characters previously assembled (four in RxFIFO, one in the Rx shift register) and discards the overrunning character(s).

Underrrun Error (All modes): This indicates that the transmit shift register was ready to begin serializing a character and found the $\overline{CTS}$ input negated.

PAD Error (BISYNC): After the EOT and NAK sequences, the receiver does not detect closing PAD of four 1's.

DPLL Error (All modes): While the DPLL is operating in FM mode to indicate that a data transition was to indicate that a data transition was not detected within the detection window for two consecutive bits and that the DPLL was forced into search mode.

Data Encoding/Decoding

The DUSCC supports the following five code- NRZ, NRZI, FM 0 , FM1, Manchester.

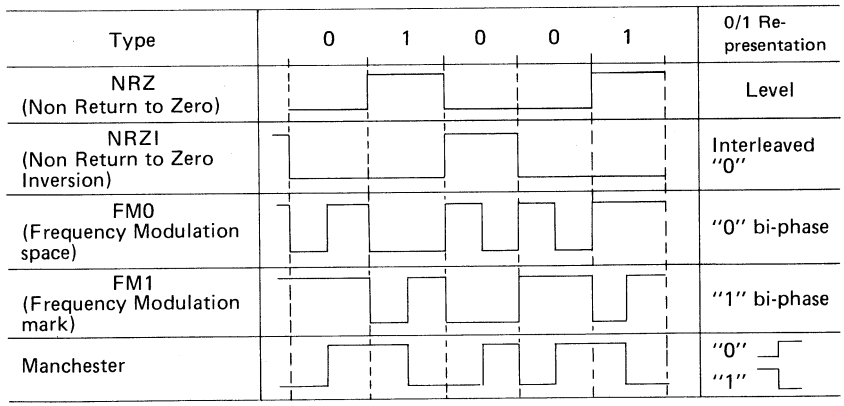


Figure 5. Data Encoding/Decoding

Transmit Timing

The A and B channels of DUSCC support ASYNC, COP, BOP full duplex transmission. The baud rate for transmitter and receiver can be selected independently from baud rate generator, counter/timer DPLL, external clock input.

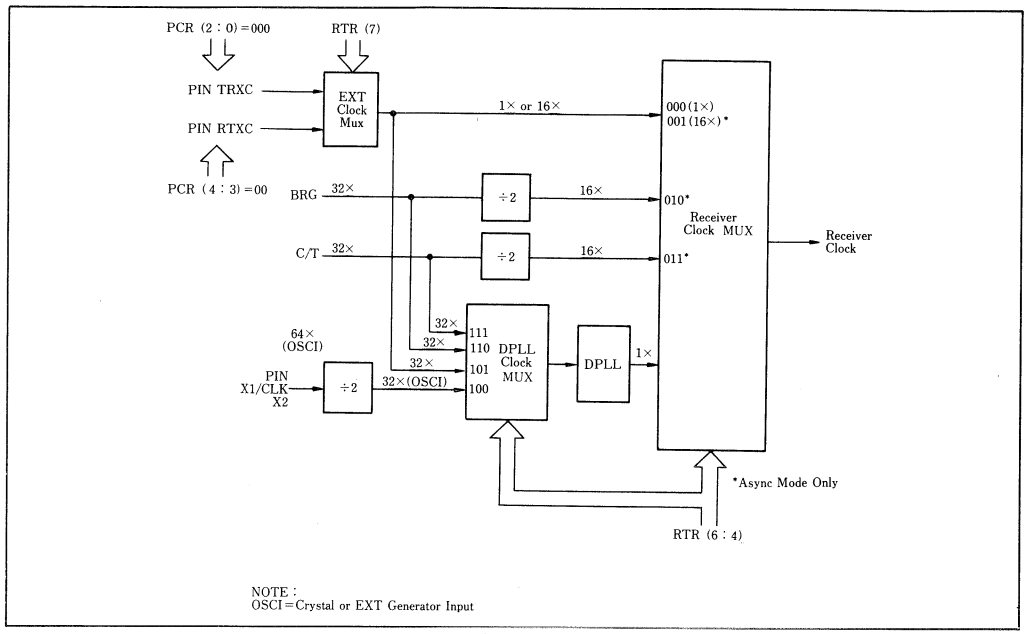


Figure 6. Receiver Clock Sources

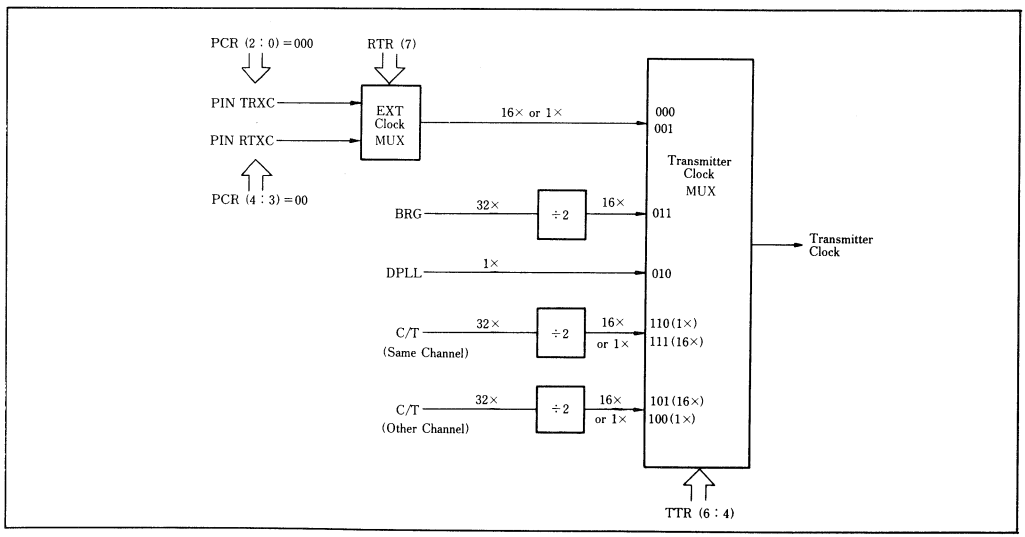


Figure 7. Transmitter Clock Sources

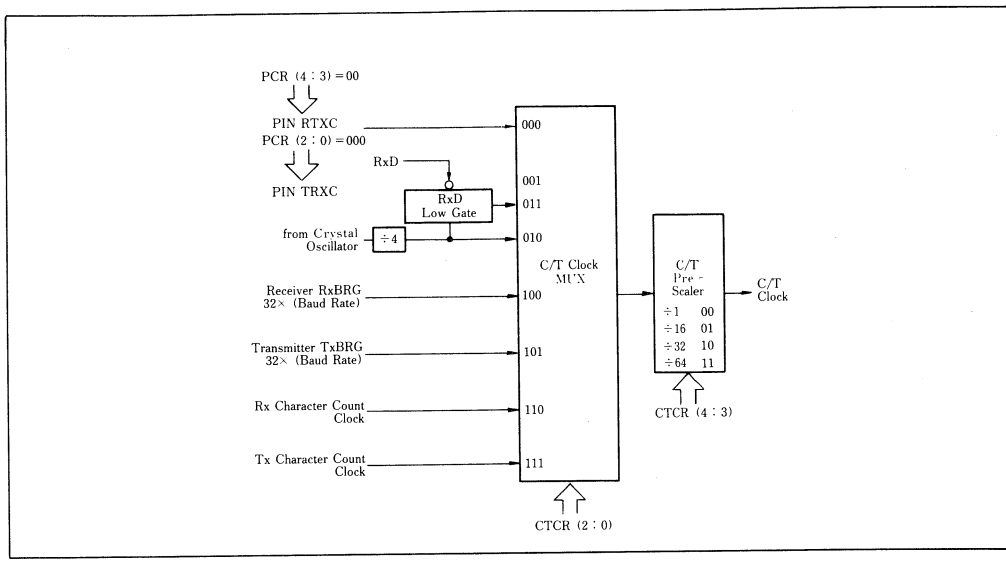


Figure 8. Counter/Timer Clock Source

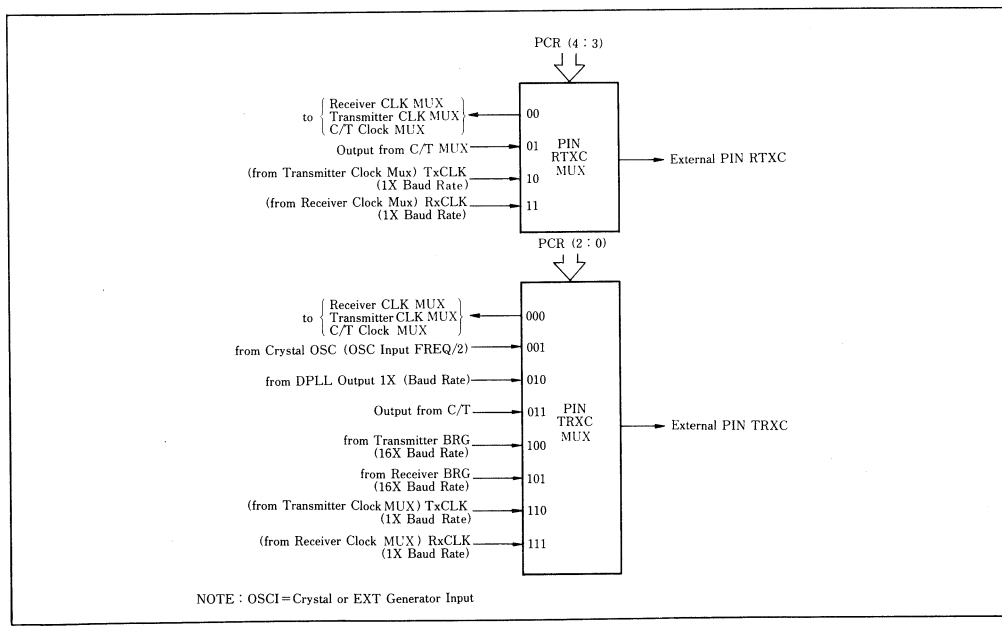


Figure 9. TRXC and RTXC Function Select

Transmit Data

The transmitter accepts parallel data from the data bus and loads it into the TxFIFO, which consists of four 8-bit holding registers. This data is then moved to the transmitter shift register, TxSR, which serializes the data according to the transmission format programmed. TxSR is loaded from the TxFIFO, from special character logic, or from the CRC/LRC generator. The LSB is transmitted first, which requires right justification of characters by CPU.

Receive Data

The receiver converts received serial data on RxD (LSB first) into parallel data according to transmission format programmed. Data is shifted through a synchronizing flip flop and one or more shift registers, the last of which is the 8-bit receiver shift register (RxSR). Bits are shifted into RxSR on the rising edge of each 1x receive clock until the LSB is in RxSR. Hence, the received character is right justified, with all unused bits in the RxSR cleared to zero.

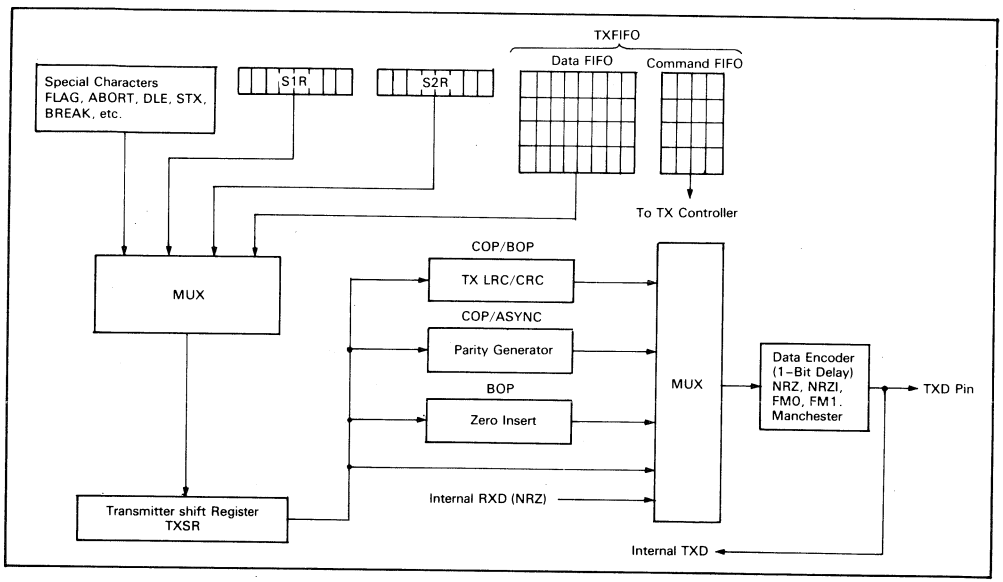


Figure 10. Transmitter Data Path

Digital Phase Locked Loop

Each channel of the DUSCC includes a DPLL used in synchronous modes to recover clock information from a received data stream. The DPLL is driven by a clock at nominally 32 times the data rate. This clock can be programmed, via RTR (7:4), to be supplied from an external input, from the receiver BRG, from the C/T, or directly from the crystal oscillator.

The DPLL uses this clock, along with the data stream to construct a data clock which may then be used as the DUSCC receive clock, transmit clock, or both. The output of the DPLL is a square wave at 1X the data rate. The derived clock can also be programmed to be output on a DUSCC pin; only the DPLL receiver output clock is available at the TRXC pin.

Four commands are associated with DPLL operation: Enter search mode, set FM mode, set NRZI mode, and disable DPLL. The commands are described in the command register description. Waveforms associated with the DPLL are illustrated in figure.

NRZI Mode Operation

NRZI mode includes NRZ and NRZI data encoding. With this type of encoding, the transitions of the data stream occur at the beginning of the bit cell (See figure 12). The DPLL has a six bit counter which is incremented by a 32× clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL output clock then rises at a count of 0 and falls at 16. Data is sampled on the rising edge of the clock. When a transition in the data stream is detected, the count length is adjusted by one or two counts, depending on the counter value when the transition occurs (see Table 5). A transition detection at the rollover point is treated as a transition occurring at zero count.

The count length adjustments cause the rising edge of the DPLL output clock to converge to the nominal center of the bit cell. In the worst case, which occurs when a DPLL pulse is coincident with the data edge, the DPLL converges after 12 data transitions.

For NRZ encoded data, a stream of alternating ones and zeros should be used as a synchronizing pattern. For NRZI encoded data, a stream of zeros should be used.

FM Mode Operation

FM mode includes FM0, FM1, and Manchester data

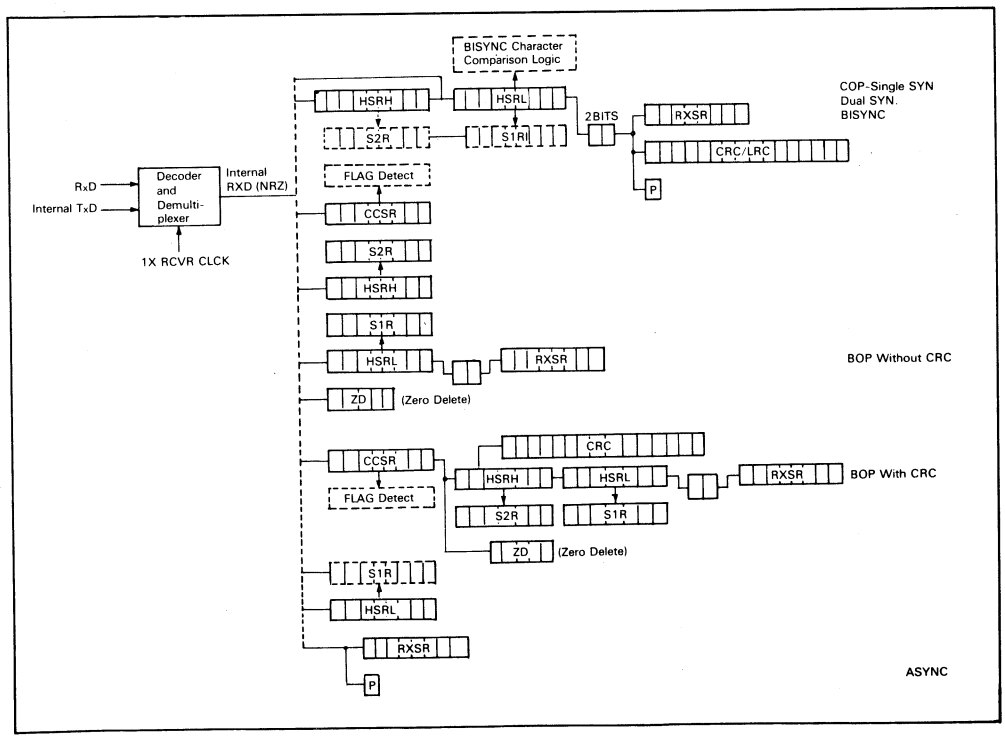


Figure 11. Receiver Data Path

encoding. With this type of encoding, transitions in the data stream always occur at the beginning of the bit cell for FM0 and FM1, or at the center of the bit cell for Manchester. The DPLL 6-bit counter is incremented by a 32x clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL receiver clock then rises on a count of 8 and falls on 24. (The DPLL transmitter clock output falls on a count of 16. It rises on a count of 0 if a transition has been detected between counts of 16 and 23. For other cases, it rises 1/2 count of the 32x input clock sooner). This provides a 1x clock with edges positioned at the nominal centers of the two halves of the bit cell. The transition detection circuit is enabled between counts of 8 and 23 inclusive. When a transition is detected, the count length is adjusted by one, depending on when the transition occurs (see table 6).

If a transition is not detected for two consecutive data bits, the DPLL is forced into search mode and the DPLL error status bit is asserted. This feature is disabled when the DPLL output is used only as the transmitter clock.

To prevent the DPLL from locking on the wrong edges of the data stream, an opening PAD sequence should be transmitted. For FM0, a stream of at least 16 ones should be sent initially. For FM1, a minimum stream of 16 zeros should be sent and for Manchester encoding the initial data stream should consist of alternating ones and zeros.

Table 5. NRZI Mode Count Length

Count When Transition Detected	Count Length Adjustment	Counter Reset After Count Reaches
0 – 7	-2	29
8 – 15	-1	30
16 – 23	+1	32
24 – 30	+2	33
None detected	0	31

Table 6. FM Mode Count Length

Count When Transition Detected	Count Length Adjustment	Counter Reset After Count Reaches
8 – 15	-1	30
16 – 23	+1	32
24 – 7	Disabled	
None detected	0	31

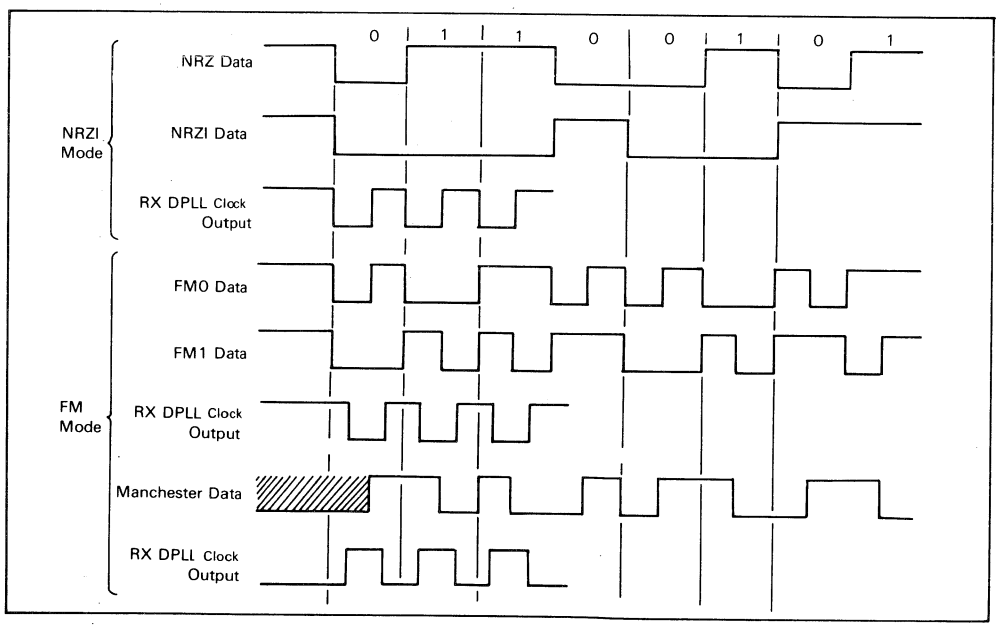


Figure 12. DPLL Waveforms

DMA Control

The DMA control section provides the interface to allow the DUSCC to operate with an external DMA controller. One of four modes of DMA can be programmed for each channel independently via CMR2[5 : 3]:

- Half duplex single address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via a single DMA acknowledge pin. The data transfer is accomplished in a single bus cycle — the DMA controller places the memory address of the source or destination of the data on the address bus and then issues the acknowledge signal, which causes the DUSCC to either write the data into its transmit FIFO (write request) or to output the contents of the top of the receive FIFO (read request). The cycle is completed when the $\overline{DTC}$ input is asserted by the DMA controller. This mode can be used when channel operation is half duplex (e.g., BISYNC). It allows a single DMA channel to service the receiver and transmitter.
- Half duplex dual address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via normal bus read and write cycles. The data transfer requires two bus cycles — the DMA controller acquires the data from the source (memory for a TX DMA or DUSCC for a RX DMA) on the first cycle and deposits it at the destination (DUSCC for a TX DMA or memory for a RX DMA) on the second bus cycle. This mode is used when channel operation is half duplex (e.g., BISYNC) and allows a single DMA channel to servicer and transmitter.
- Full duplex single address. This mode is similar to half duplex single address mode but provides separate request and acknowledge pins for the receiver and transmitter.

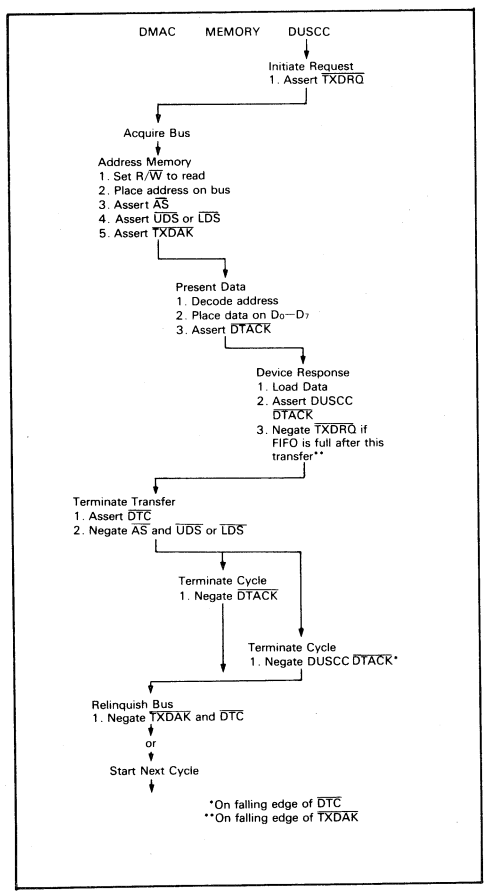


Figure 13. Transmitter DMA Request Operation — Single Address Mode

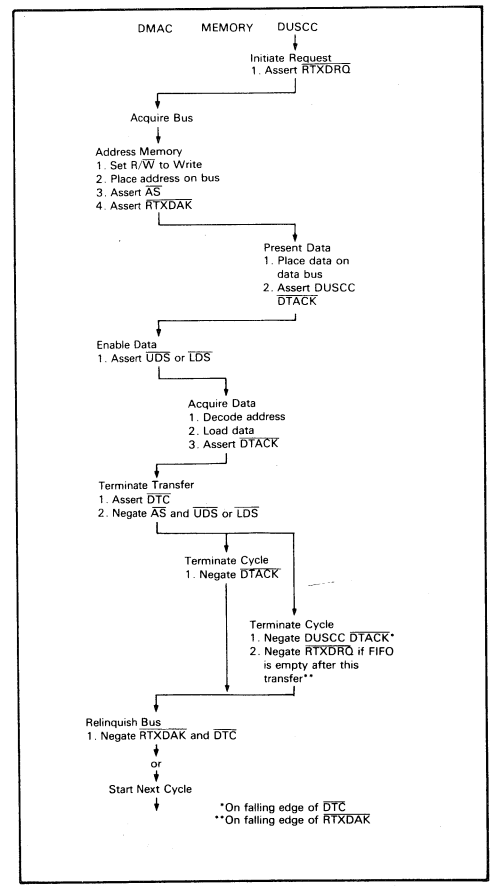


Figure 14. Receiver DMA Request Operation — Single Address Mode

— Full duplex dual address. This mode is similar to half duplex dual address mode but provides separate request pins for the receiver and transmitter.

Interrupt Control

The interrupt of DUSCC is caused by the ICR which contains the master interrupt enables for each channel (ICR[1] and ICR[0]). ICR[1], [0] must be set if the corresponding channel is to cause an interrupt. The CPU vector mode is specified by IRC [5 : 4] which selects either vectored or non-vectored operation. If vectored mode is selected, the content of the IVR or IVRM is placed on the data bus when IACK is activated. If ICR[2] is set, the content of IVRM is output which contains the content of IVR and the encoded status of the interrupting condition. The IER is programmed to enable specified conditions or groups of conditions to cause an interrupt by asseting the corresponding bit.

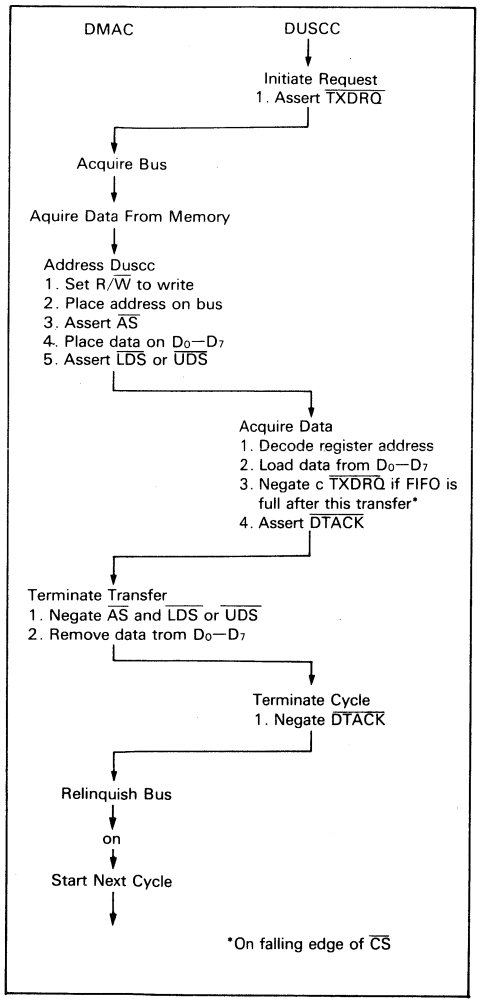


Figure 15. Transmitter DMA Request Operation — Dual Address Mode

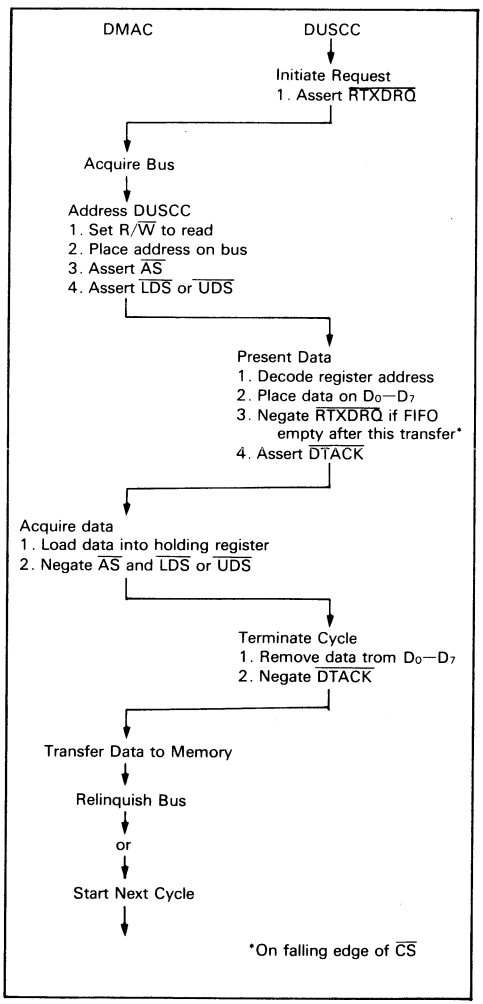


Figure 16. Receiver DMA Request Operation — Dual Address Mode

Counter/Timer

Each channel of the DUSCC contains a counter/timer (C/T) consisting of a 16-bit down counter, a 16-bit preset register, and associated control circuits. Operation of the counter/timer is programmed via the counter/timer control register (CTCR). There are also four commands associated with C/T operation, as described in the command description section.

The C/T clock source, clock prescaling, and operating mode are programmed via CTCR[2 : 0], CTCR [4 : 3], and CTCR[6] respectively. The preset register is loaded with a minimum of 2 by the CPU and its contents can be transferred into the down counter by a command, or automatically upon reaching terminal count if CTCR[6] is negated. Commands are also available to stop and start the C/T and to preset it to an initial value of FFFF. Counting is triggered by the falling edge of the clocking input. The C/T zero count status bit, ICTSR[6], is set when the C/T reaches the terminal count of zero and ICTSR[7] indicates whether the counter is currently enabled or not.

An interrupt is generated upon reaching zero count if CTCR[7] and the channel's master interrupt enable are asserted. The output of the C/T can be programmed to be output on the channel's RTXC or TRXC pin (via PCR[4 : 0] as either a single pulse or a square wave, as programmed in CTCR[5]. The contents of C/T can be read at any time by the CPU, but the C/T should normally be stopped before this is done. Several C/T operating modes can be selected by programming of the counter/timer control register. Typical applications include:

1. Programmable divider. The selected clock source, optionally prescaled, is divided by the contents of the preset register. The counter automatically reloads itself each time the terminal count is reached. In this mode, the C/T may be programmed to be used as the RX or TX bit rate generator, as the input to the DPLL, or it may be output on a pin as either a pulse or a square wave. The C/T interrupt should be disabled in this mode.

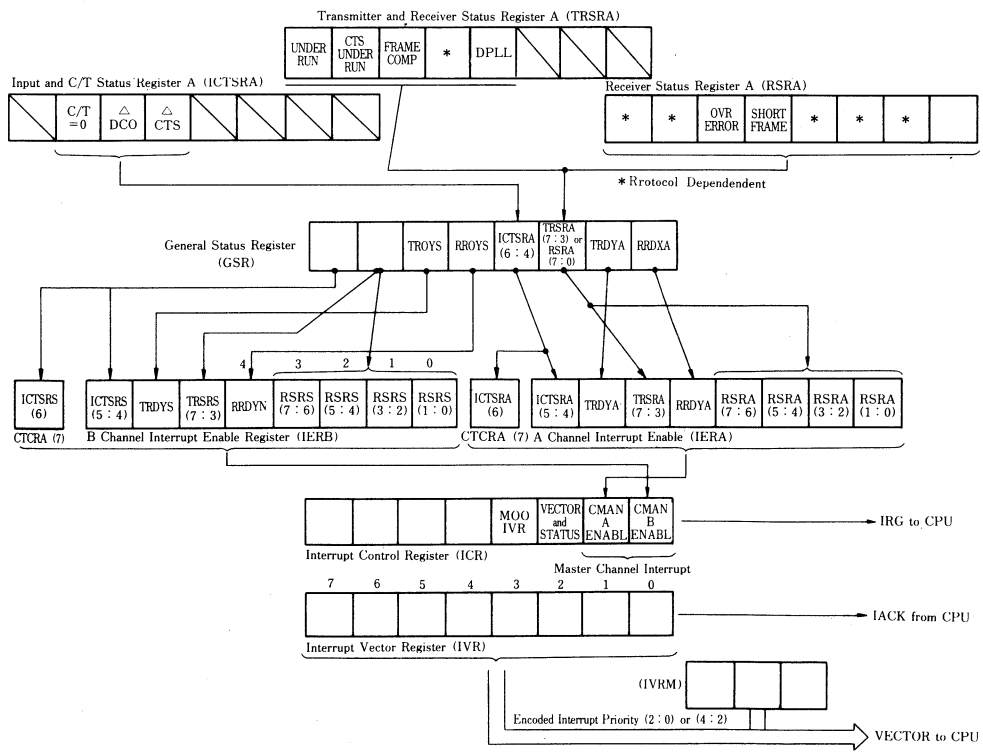


Figure 17. Interrupt Control and Status Register

2. Periodic interrupt generator. This mode is similar to the programmable divider mode, except that the C/T interrupt is enabled, resulting in a periodic interrupt to the CPU.

3. Delay timer. The counter is preset from the preset register and a clock source, optionally prescaled, is selected. An interrupt is generated upon reaching terminal count. The C/T continues counting without reloading itself and its contents may be read by the CPU to allow additional delay past the zero count to be determined.

4. Character counter. The counter is preset to FFFF by command and the clock source becomes the internal signal used to control loading of the RX or TX characters. This operation is selected by CTCR[2 : 0]. The C/T counts characters loaded into the RXFIFO by the receiver or loaded into the transmit FIFO by the CPU respectively. The current character count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted. When counting TX characters, the terminal count condition can be programmed through TRR[4] to cause an end of message sequence to be transmitted. When counting received characters, the FIFO'ed EOM status bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. The channel's 'reset TX' or 'reset RX' commands have no effect on the operation of the C/T.

5. External event counter. The counter is preset to FFFF by command and an external clock source is selected. The current count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted.

6. Bit length measurement. The counter is preset to FFFF by command and the X1/CLK/4 clock input gated by RXD mode (optionally prescaled) is programmed. The C/T starts counting when RXD goes low and stops counting when RXD goes high. At this time, status and an interrupt (if enabled) are generated. The resulting count in the counter can be read by the CPU to determine the bit rate of the input data. Normally this function is used for asynchronous operation.

Crystal Oscillator

The crystal oscillator operates directly from a crystal (normally 14.7456MHz if the internal BRG is to be used) connected across the X1/CLK and X2/IDCN pins with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to the X1/CLK pin. This signal is divided by two to provide the internal system clock (a maximum of 16MHz input is allowed).

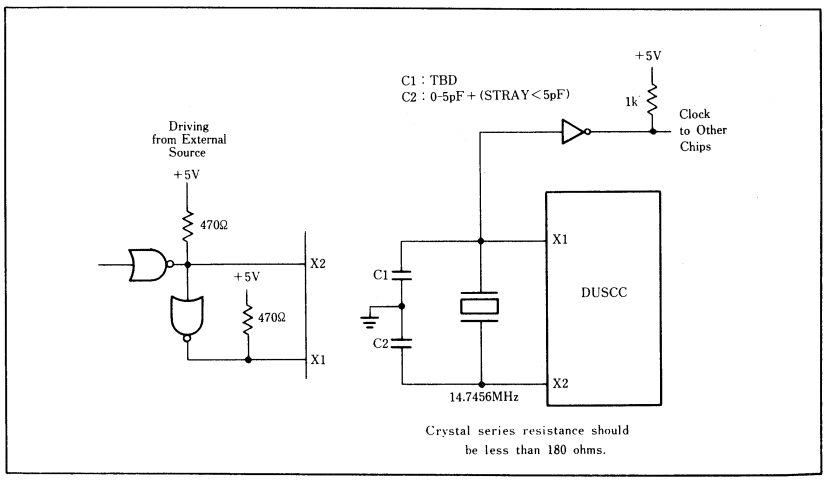


Figure 18. Clock Timing

Absolute Maximum Ratings

Parameter	Rating	Unit
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−55 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low level voltage	V_{IL}	0	0.4	0.8	V
Input high level voltage	V_{IH}	2.0	3.5	V_{CC}	V
Operating temperature	T_{OPr}	0	25	70	°C

Electrical Characteristics

DC Electrical Characteristics (V_{CC} = 5.0 V ± 5%[4,5,6], V_{SS} = 0 V, T_a = 0°C to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}			0.8	V	
Input high voltage	V_{IH}					
All except X1/CLK		2.0			V	
X1/CLK		$0.9V_{CC}$		V_{CC}	V	
Output low voltage	V_{OL}			0.4	V	I_{OL} = 2.4 mA
Output high voltage	V_{OH}					
(except o.c. outputs)		2.4			V	I_{OH} = −400 μA
X1/CLK low input current	I_{XIL}	−4.0	−2.0	0.0	mA	V_{in} = 0, X2 grounded
		−3.0	−1.5	0.0	mA	V_{in} = 0, X2 floated
X1/CLK high input current	I_{XIH}	−1.0	0.2	1.0	mA	V_{in} = V_{CC}, X2 grounded
		0.0	3.5	10.0	mA	V_{in} = V_{CC}, X2 floated
X2 low input current	I_{X2L}	−100	−30	0.0	μA	V_{in} = 0, X1/CLK floated
X2 high input current	I_{X2H}	0.0	+30	100	μA	V_{in} = V_{CC}, X1/CLK floated
Input leakage current	I_{IL}	−10		10	μA	V_{in} = 0 to V_{CC}
Data bus 3-state leakage current	I_{LL}	−10		10	μA	V_0 = 0 to V_{CC}
Open collector output leakage current	I_{OC}	−10		10	μA	V_0 = 0 to V_{CC}
Power supply current	I_{CC}			200	mA	

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the devices.

This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operation section of this specification is not implied.

2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4 V and 2.4 V with a transition time of 20 ns maximum. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input voltages of 0.8 V and 2.0 V and output voltages of 0.8 V and 2.0 V as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. Test condition for outputs: C_L = 150 pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50 pF, R_L = 2.7 kΩ to V_{CC}.
8. This specification will impose maximum 68000 CPU CLK to 6 MHz. Higher CPU CLK can be used if repeating bus reads are not performed.
9. Write data including commands are latched by either the rising edge of $\overline{CS}$ or the falling edge of $\overline{DTACK}$ whichever occurs first. Execution of the valid command (after it is latched) requires two complete periods of the PHI clock or three falling edges of X1 (see figure 18).
10. Tests for open drain outputs are intended to guarantee switching of the output transistor. Masurement of this response is referenced from the midpoint of the switching signal to a point 0.5 V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

AC Electrical Characteristics (V_{CC}=5.0 V ± 5%[4,5,6,7], V_{SS}= 0 V, T_a =0°C to + 70°C)

No.	Parameter	Symbol	Min	Typ	Max	Unit
①	$\overline{RESET}$ pulse width	t_{RES}	3.0			μs
②	A0–A6 set-up time to $\overline{CS}$ low	t_{AS}	10			ns
③	A0–A6 hold time from $\overline{CS}$ high	t_{AH}	0			ns
④	R/$\overline{W}$ set-up time to $\overline{CS}$ low	t_{RWS}	0			ns
⑤	R/$\overline{W}$ hold time to $\overline{CS}$ high	t_{RWH}	0			ns
⑥	$\overline{CS}$ high pulse, width[8]	t_{CSW}	160			ns
⑦	$\overline{CS}$ or $\overline{IACK}$ high from $\overline{DTACK}$ low	$t_{⊕SW}$	30			ns
⑧	Data valid from $\overline{CS}$ or $\overline{IACK}$ low	t_{RDD1}		125	300	ns
⑨	Data bus floating from $\overline{CS}$ high	t_{RDD2}		100	270	ns
⑩	Data hold time from $\overline{CS}$ high[9]	t_{WDH}	0			ns
⑪	$\overline{DTACK}$ low from read data ready	t_{DTKD1}	0			ns
⑫	$\overline{DTACK}$ low from $\overline{CS}$ low	t_{DTKD2}		200	360	ns
⑬	$\overline{DTACK}$ high from $\overline{CS}$ high	t_{DTKD3}			235	ns
⑭	$\overline{DTACK}$ high impedance from $\overline{CS}$ high	t_{DTKZ}			360	ns
⑮	$\overline{DTACK}$ low from $\overline{IACK}$ low	t_{DTKD}		300	650	ns
⑯	Port input set-up time to $\overline{CS}$ low	t_{PIS}	20			ns
⑰	Port input hold time from $\overline{CS}$ high	t_{PIH}	0			ns
⑱	Port output valid from $\overline{CS}$ high	t_{POD}			560	ns
⑲	$\overline{IRQ}$ high from:[10]					
	Read RXFIFO (RXRDY interrupt)	t_{RFD}			300	ns
	Write TXFIFO (TXRDY interrupt)	t_{TFD}			300	ns
	Write RSR (receiver condition interrupt)	t_{RSD}			650	ns
	Write TRSR (receiver/transmitter interrupt)	t_{TSD}			650	ns
	Write ICTSR (port change and timer/ counter interrupt)	t_{ICD}			650	ns

(to be continued)

No.	Parameter		Symbol	Min	Typ	Max	Unit
⑳	X1/CLK high or low time		t_{CYCH}, t_{CYCL}	25			ns
	X1/CLK frequency		f_C	2.0	14.7456	16	MHz
	CTCLK high or low time		t_{CTCH}, t_{CTCL}	100			ns
	CTCLK frequency		f_{CT}	0		4.0	MHz
	RXC high or low time		t_{RCH}, t_{RCL}	110			ns
	RXC frequency	(16X)	f_R	0		4.0	MHz
		(1X)		0		4.0	MHz
	TXC high or low time			110			ns
	TXC frequency	(16X)	t_{TCH}, t_{TCL}	0		4.0	MHz
		(1X)	f_T	0		4.0	MHz
㉑	TXD output from TXC input low		t_{TDD}			360	ns
㉒	TXD output from TXC output low		t_{TCD}	0		50	ns
㉓	RXD data set-up time to RXC high		t_{RDS}	50			ns
㉔	RXD data hold time from RXC high		t_{RDH}	0			ns
㉕	$\overline{IACK}$ low to daisy chain low		t_{IDCD}			350	ns
㉖	Data valid from receive DMA $\overline{ACK}$		t_{RDAD}			320	ns
㉗	$\overline{DTC}$ width		t_{DTCW}	100			ns
㉘	$\overline{RDY}$ low to $\overline{DTC}$ low		t_{DTCD}	80			ns
㉙	Data bus float from $\overline{DTC}$ low		t_{RDDH}			300	ns
㉚	DMA $\overline{ACK}$ low to $\overline{RDY}$ ($\overline{DTACK}$) low		t_{RADD}		450		ns
㉛	$\overline{RDY}$ high from $\overline{DTC}$ low		t_{DRDH}			420	ns
㉜	$\overline{RDY}$ high impedance from $\overline{DTC}$ low		t_{DRDZ}			530	ns
㉝	Receive DMA $\overline{REQ}$ high from DMA $\overline{ACK}$ low		t_{RDRH}			500	ns
㉞	Receive DMA $\overline{ACK}$ width		t_{RDAW}	150			ns
㉟	Receiver DMA $\overline{ACK}$ low to $\overline{DONE}$ low		t_{RDND}			250	ns
㊱	Data hold from $\overline{DTC}$ low[11]		t_{DTDH}			230	ns
㊲	Transmit DMA $\overline{REQ}$ high from $\overline{ACK}$ low		t_{TDRH}			550	ns
㊳	Transmit DMA $\overline{ACK}$ width		t_{TDAW}	150			ns
㊴	Transmit DMA $\overline{ACK}$ low to $\overline{DONE}$ low output		t_{TDND}			250	ns
㊵	$\overline{CS}$ low to transmit $\overline{DONE}$ low output		t_{CTDD}			400	ns
㊶	$\overline{CS}$ low to transmit DMA $\overline{REQ}$negated		t_{CTRD}			620	ns
㊷	$\overline{CS}$ low to receive DONE low		t_{CRDD}			400	ns
㊸	$\overline{CS}$ low to receive DMA $\overline{REQ}$ negated		t_{CRRD}			620	ns

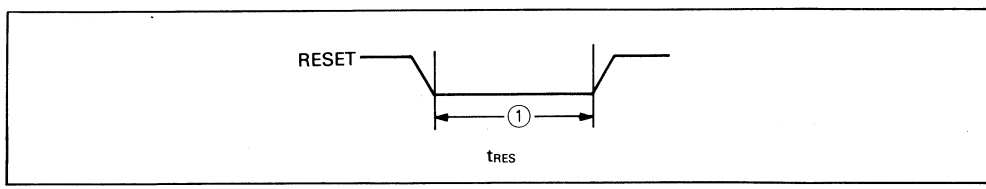


Figure 19. Reset Timing

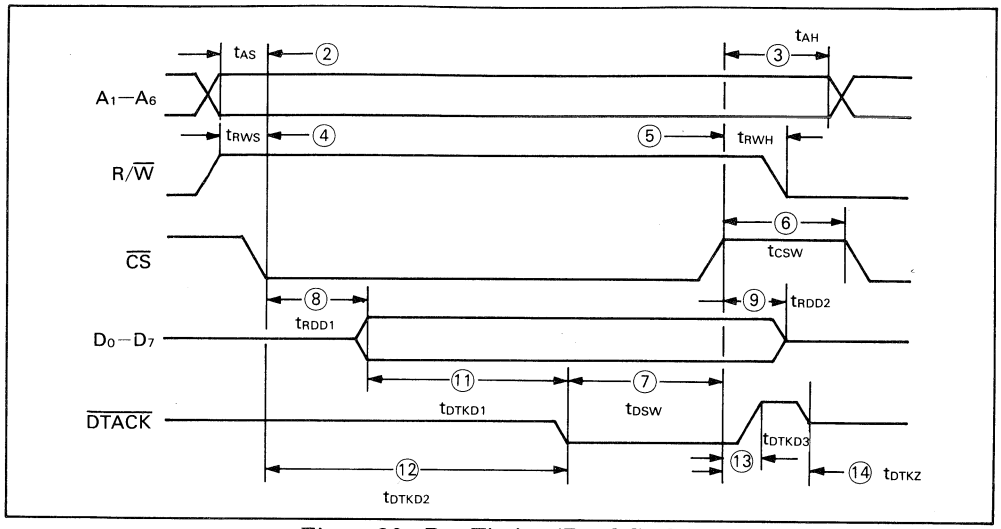


Figure 20. Bus Timing (Read Cycle)

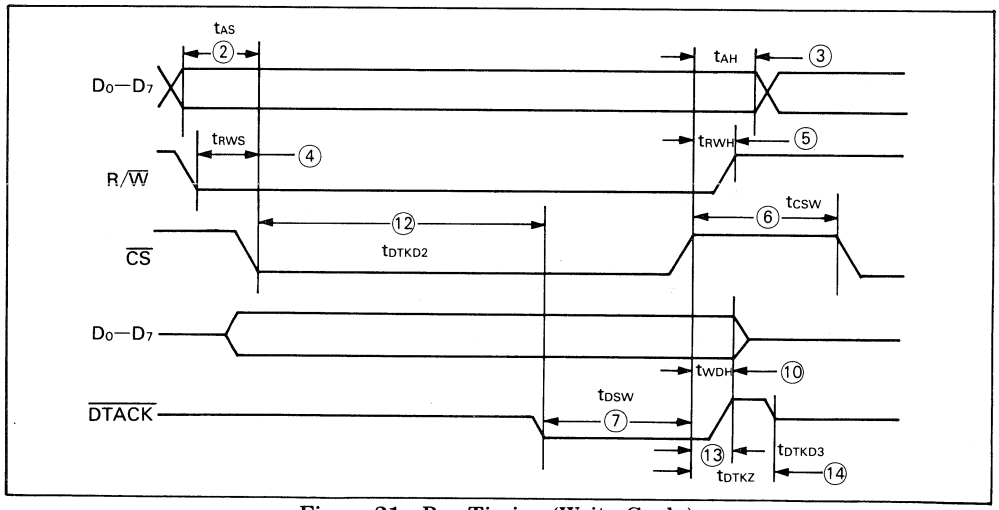


Figure 21. Bus Timing (Write Cycle)

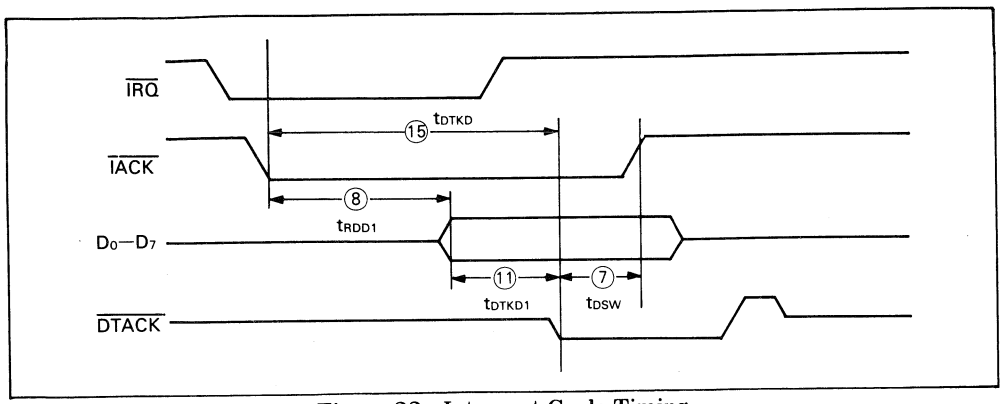


Figure 22. Interrupt Cycle Timing

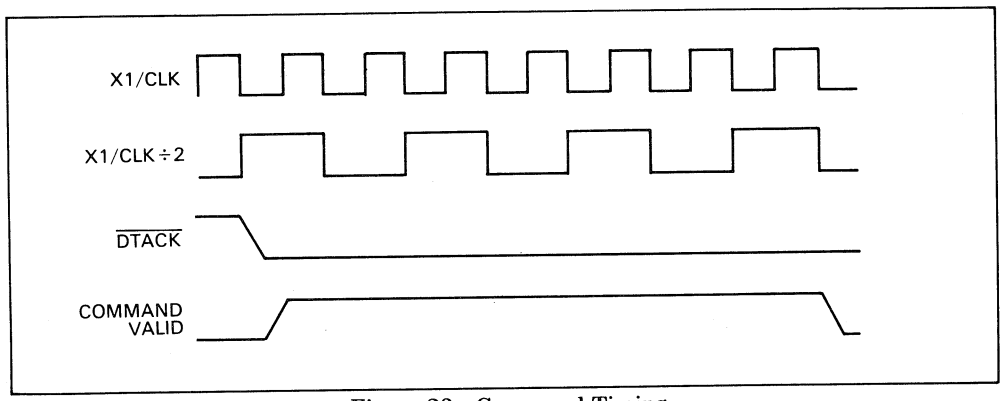


Figure 23. Command Timing

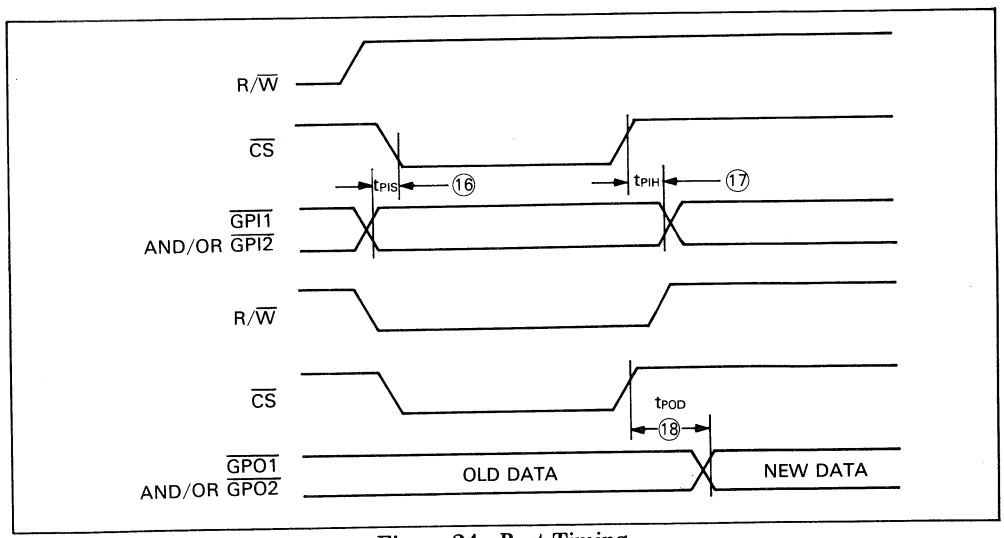


Figure 24. Port Timing

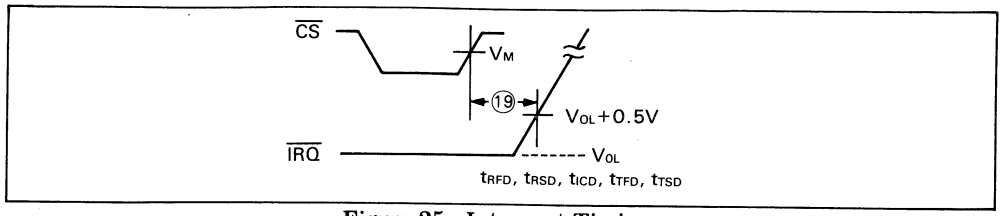


Figure 25. Interrupt Timing

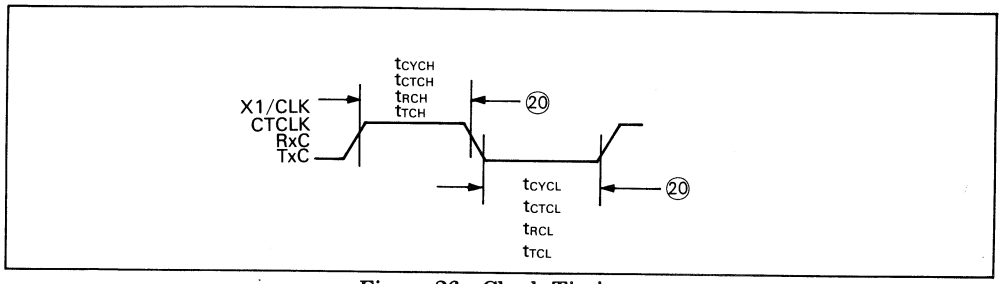


Figure 26. Clock Timing

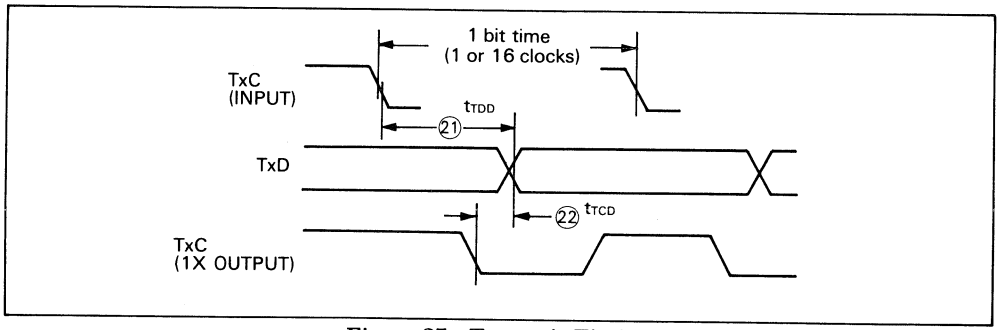


Figure 27. Transmit Timing

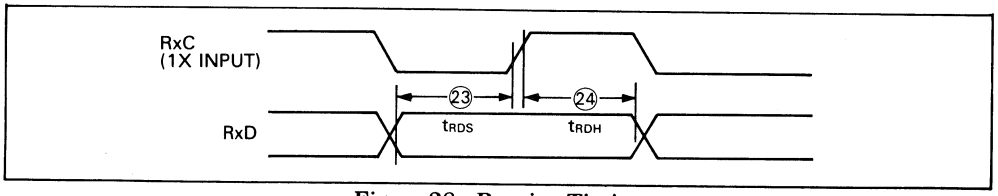


Figure 28. Receive Timing

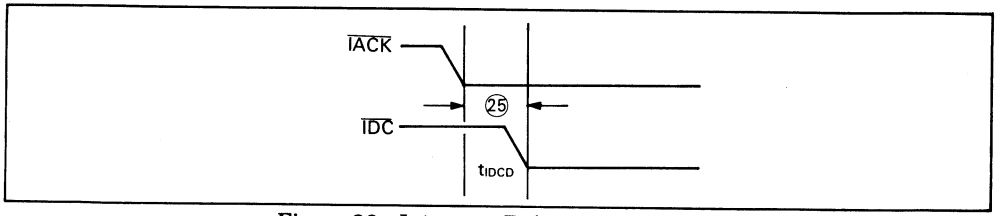


Figure 29. Interrupt Daisy Chain Timing

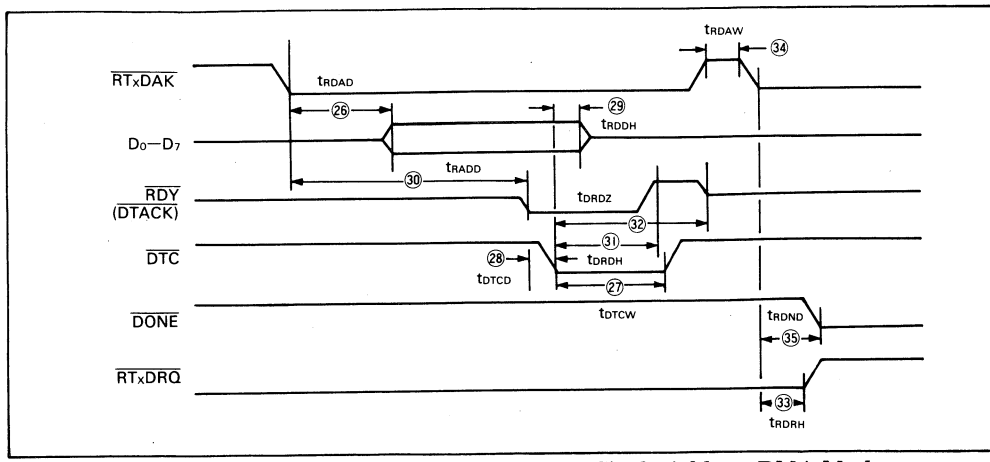


Figure 30. DMA Receiver Read Timing — Single Address DMA Mode

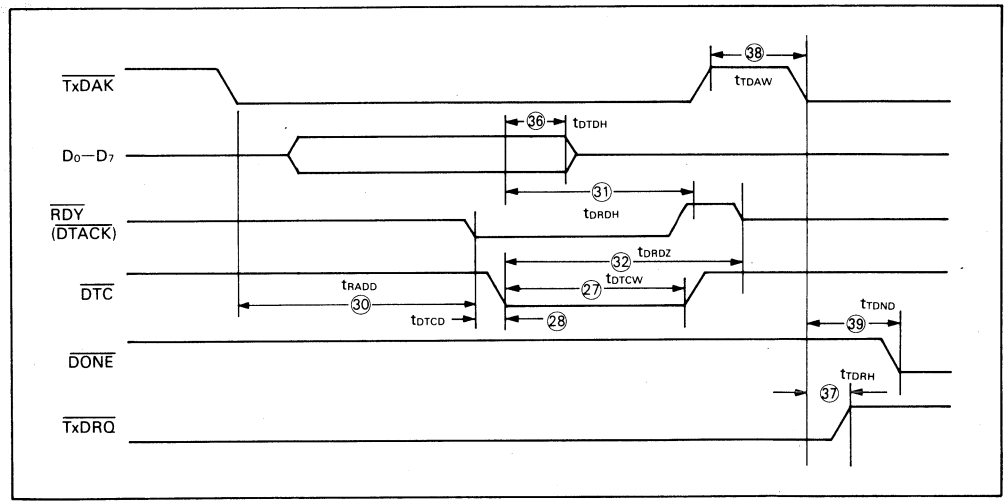


Figure 31. DMA Transmit Write Timing — Single Address DMA Mode

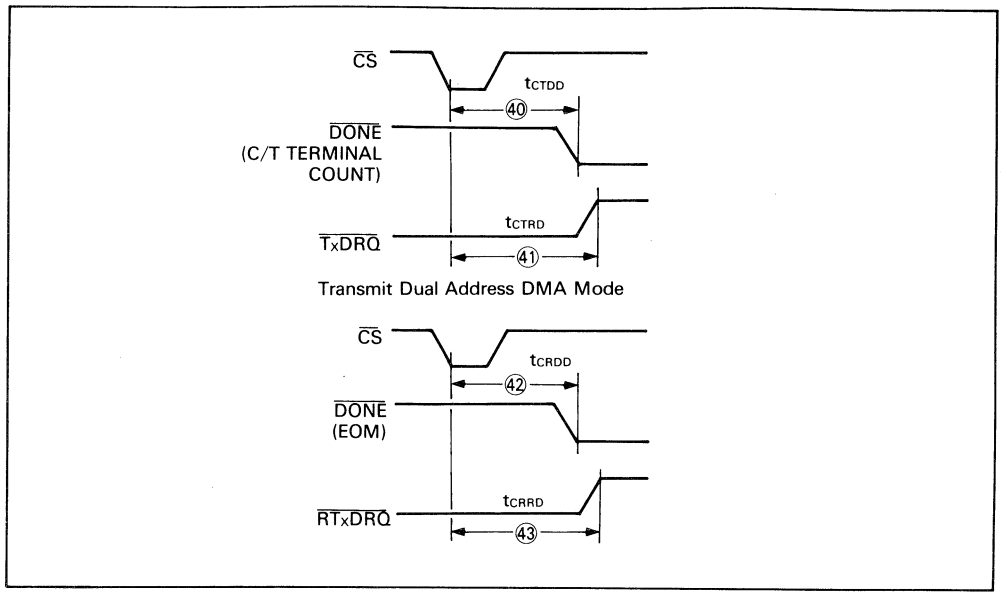


Figure 32. Dual Address DMA Mode Timing

Opto Devices

LASER DIOES

	Packages										
Chips	**A**	**AC**	**C**	**E**	**G**	**FG**	**B**	**P**	**SP**	**BF**	**DL**
HL7801				HL7801E	HL7801G*						
HL7802				HL7802E	HL7802G						
HLP1000	HLP1400		HLP1600	HL8311E			HLP1500				
HL1221	HL1221A	HL1221AC	HL1221C				HL1221B				
HL1321/ HLP5400	HLP5400	HL1321AC	HLP5600			HL1321FG	HLP5500	HL1321P	HL1321SP	HL1321BF	HL1321DL
HL1322	HL1322A	HL1322AC									
HL1341	HL1341A	HL1341AC				HL1341FG				HL1341BF	HL1341DL
HL1521	HL1521A	HL1521AC									
HL1541	HL1541A	HL1541AC				HL1541FG				HL1541BF	HL1541DL

* HL7801G package dimensions are different from those of other G-type products.

INFRARED EMITTING DIODES

	Packages					
Chips	**R**	**RG**	**SG**	**ML**	**SL**	**F**
HLP30	HLP20R —HLP60R	HLP20RG —HLP60RG				
HE8403	HE8403R		HE8403SG	HE8403ML		HE8402F
HE8801			HE8801			
HE8807			HE8807SG		HE8807SL	
HE8811			HE8811			
HE1301	HE1301R		HE1301SG	HE1301ML		
HE1302				HE1302ML		

PHOTODIODES

	Packages		
Chips	**QG**	**TG**	**CX**
HR8101	HR8101		
HR8102		HR8102	
HR8202		HR8202TG	
HR1101		HR1101	
HR1102		HR1102	HR1102CX
HR1103		HR1103TG	HR1103CX
HR1104		HR1104TG	HR1104CX
HR1105		HR1105TG	

HL7801E

GaAlAs LD

Description

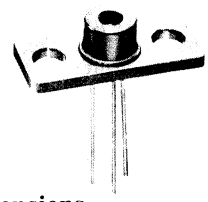
HL7801E is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

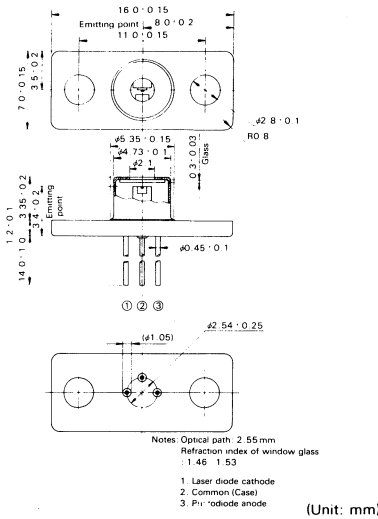
A screw-on type package facilitates the adjustment of optical components. Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 760–800 nm
- Built-in photodiode for monitoring laser output
- Low astigmatism: As = 2 μm typ.
- Small beam ellipticity:
  $\theta_{//}$ = 15 deg., $\theta_{\perp}$ = 30 deg. typ.
- Single longitudinal mode

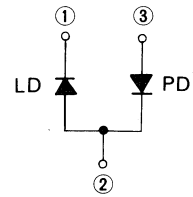


Package Dimensions



E-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	90	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.13	0.25		mW/mA	$\frac{3(mW)}{I\,(4\,mW) - I\,(1\,mW)}$
Lasing wavelength	λ_p	760	780	800	nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$	10	15	20	deg.	P_O = 3 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	30	40	deg.	P_O = 3 mW
Monitor current	I_S	0.1	0.3		mA	P_O = 3 mW

HL7801G

GaAlAs LD

Description

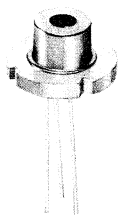
HL7801G is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

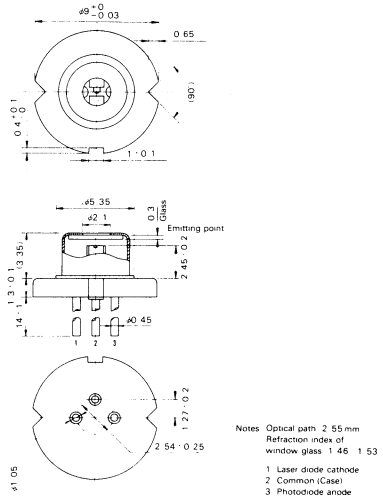
Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 760–800 nm
- Built-in photodiode for monitoring laser output
- Low astigmatism: As = 2 μm typ.
- Small beam ellipticity:
  $\theta_{//}$ = 15 deg., $\theta_{\perp}$ = 30 deg. typ.
- Single longitudinal mode



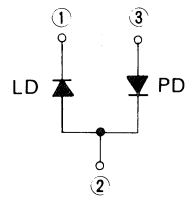
Package Dimensions



(Unit: mm)

G-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	90	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.13	0.25		mW/mA	$\frac{3(mW)}{I(4\ mW) - I(1\ mW)}$
Lasing wavelength	λ_p	760	780	800	nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$	10	15	20	deg.	P_O = 3 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	30	40	deg.	P_O = 3 mW
Monitor current	I_S	0.1	0.3		mA	P_O = 3 mW

HL7802E

GaAlAs LD

Description

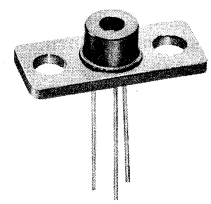
HL7802E is a high-power 0.78 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

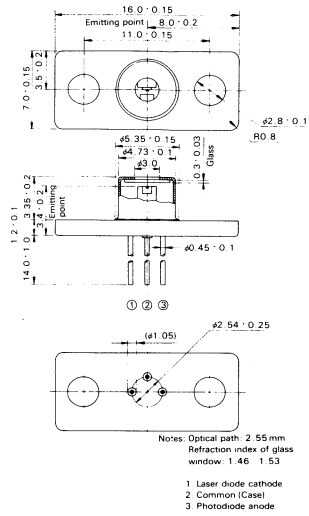
A screw-on type package facilitates the adjustment of optical components. Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 770–800 nm
- Built-in photodiode for monitoring laser output
- Single longitudinal mode



Package Dimensions



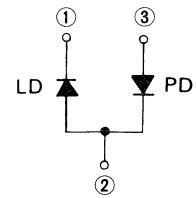
Notes: Optical path: 2.55 mm
Refraction index of glass window: 1.46 1.53

1. Laser diode cathode
2. Common (Case)
3. Photodiode anode

(Unit: mm)

E-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	10	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	90	mA	
Optical output power	P_O	10			mW	Kink free
Slope efficiency	η	0.13	0.25		mW/mA	$\frac{6(mW)}{I(8\ mW) - I(2\ mW)}$
Lasing wavelength	λ_p	770	785	800	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$	6	11	16	deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	30	40	deg.	P_O = 10 mW
Monitor current	I_S	0.35			mA	$V_{R(PD)}$ = 5 V, P_O = 10 mW

HL7802G

GaAlAs LD

Description

HL7802G is a high-power 0.78 μm GaAlAs laser diode with double heterojunction structure.

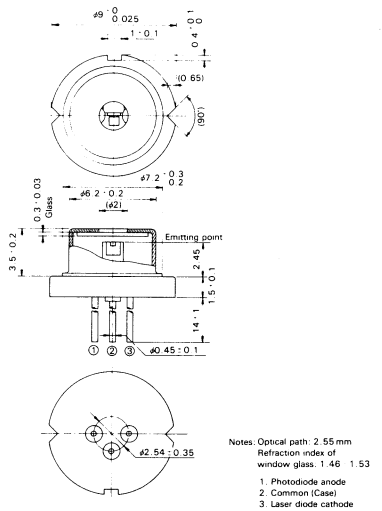
It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 770–800 nm
- Built-in photodiode for monitoring laser output
- Single longitudinal mode

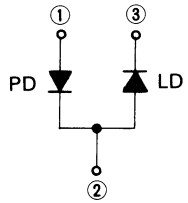
Package Dimensions



(Unit: mm)

G-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	10	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	90	mA	
Optical output power	P_O	10			mW	Kink free
Slope efficiency	η	0.13	0.25		mW/mA	$\frac{6(mW)}{I(8\ mW) - I(2\ mW)}$
Lasing wavelength	λ_p	770	785	800	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$	6	11	16	deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	30	40	deg.	P_O = 10 mW
Monitor current	I_S	0.35			mA	$V_{R(PD)}$ = 5 V, P_O = 10 mW

HLP1400

GaAlAs LD

Description

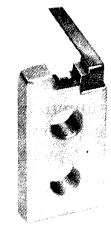
HLP1400 is a 0.8 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in fiberoptic communications, optical disc memories or various other types of optical equipment.

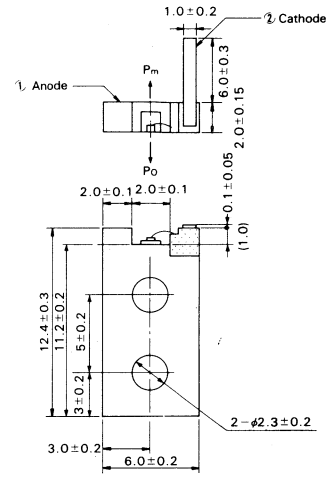
The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Infrared light output: λ_p = 800−850 nm
- 15 mW CW operation at room temperature
- Single longitudinal mode
- Fast pulse response: t_r, t_f ≦ 0.5 ns



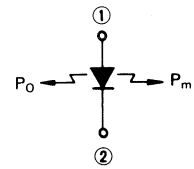
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	15	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	15			mW	Kink free
		4	5		mW	$I_F = I_{th}$ + 25 mA
Monitor power	P_m	2			mW	$I_F = I_{th}$ + 25 mA
Lasing wavelength	λ_p	800	830	850	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$		10		deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$		25		deg.	P_O = 10 mW
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HLP1500

GaAlAs LD

Description

HLP1500 is a 0.8 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in fiberoptic communications equipment.

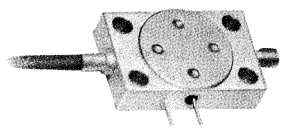
The laser beam is output from the connected optical fiber. Monitoring power is output from the glass rod as optical output power.

—Fiber specifications—

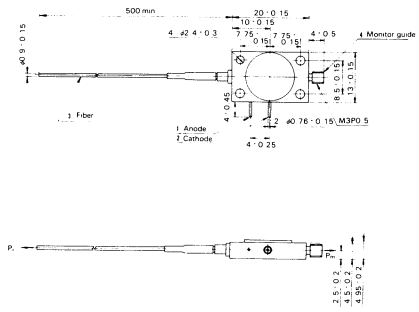
Numerical aperture	: 0.2
Core diameter	: 50 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Refraction index profile	: GI type
Fiber length	: More than 500 mm

Features

- Infrared light output: λ_p = 800–850 nm
- 6 mW CW operation at room temperature
- Single longitudinal mode
- Fast pulse response: t_r, t_f ≦ 0.5 ns



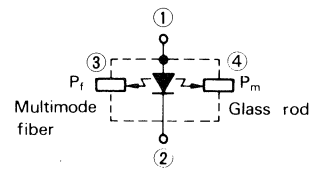
Package Dimensions



B-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	6	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Fiber optical output power	P_f	6			mW	Kink free
		2	3		mW	$I_F = I_{th}$ + 25 mA
Monitor power	P_m	0.5			mW	$I_F = I_{th}$ + 25 mA
Lasing wavelength	λ_p	800	830	850	nm	P_f = 4 mW
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HLP1600

GaAlAs LD

Description

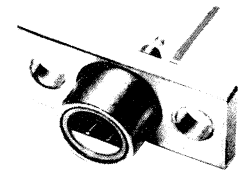
HLP1600 is a 0.8 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in fiberoptic communications, optical disc memories or various other types of optical equipment.

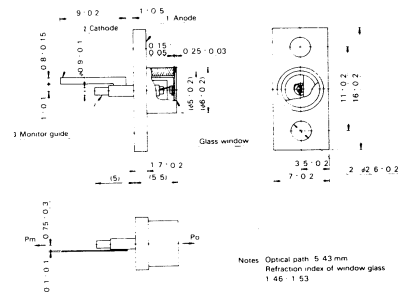
Monitoring power is output from the glass rod as optical output power.

Features

- Infrared light output: λ_p = 800−850 nm
- 15 mW CW operation at room temperature
- Single longitudinal mode
- Fast pulse response: t_r, t_f ≦ 0.5 ns



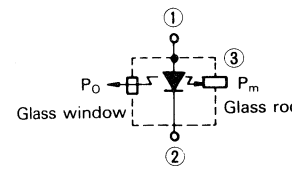
Package Dimensions



C-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	15	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	15			mW	Kink free
		4	5		mW	$I_F = I_{th} + 25$ mA
Monitor power	P_m	0.2			mW	$I_F = I_{th} + 25$ mA
Lasing wavelength	λ_p	800	830	850	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$		10		deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$		25		deg.	P_O = 10 mW
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1221A

InGaAsP LD

Description

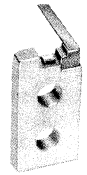
HL1221A is a 1.2 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in fiberoptic communications and various other types of optical equipment.

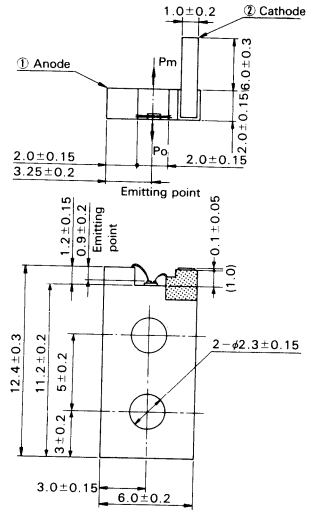
The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1170–1230 nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns



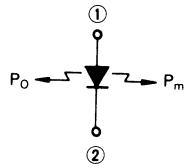
Package Dimensions



A-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	0 to +60	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1170	1200	1230	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1221AC

InGaAsP LD

Description

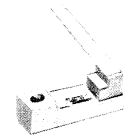
HL1221AC is a 1.2 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in fiberoptic communications and various other types of optical equipment.

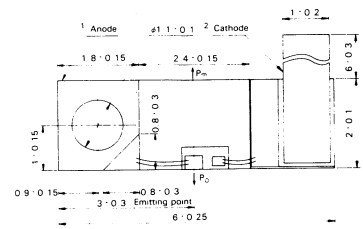
The package is compact to facilitate module assembly.

Features

- Long wavelength light output:
  $\lambda_p = 1170-1230$ nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns



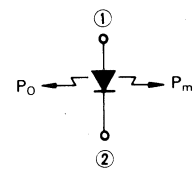
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25$°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	0 to +60	°C

Optical and Electrical Characteristics ($T_C = 25$°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1170	1200	1230	nm	$P_O = 3$ mW
Spectral width	$\Delta\lambda$		2		nm	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1221B

InGaAsP LD

Description

HL1221B is a 1.2 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in fiberoptic communications equipment.

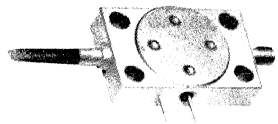
The laser beam is output from the connected optical fiber. Monitoring power is output from the glass rod as optical output power.

−Fiber specifications−

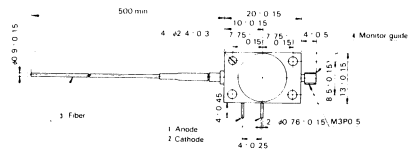
Numerical aperture	: 0.2
Core diameter	: 50 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Refraction index profile	: GI type
Fiber length	: More than 500 mm

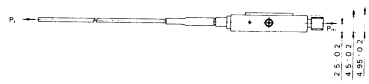
Features

- Long wavelength light output: λ_p = 1170−1230 nm
- 1.2 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns



Package Dimensions





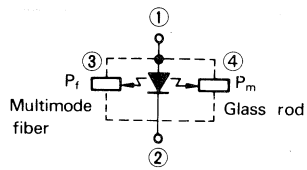
B-type

(Unit: mm)

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	−40 to +60	°C

Internal Circuit



Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Fiber optical output power	P_f	1.2			mW	Kink free
		0.4	0.7		mW	$I_F = I_{th}$ + 20 mA
Monitor power	P_m	0.05			mW	$I_F = I_{th}$ + 20 mA
Lasing wavelength	λ_p	1170	1200	1230	nm	P_f = 0.5 mW
Spectral width	$\Delta\lambda$		2		nm	P_f = 0.5 mW
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HITACHI

HL1221C

InGaAsP LD

Description

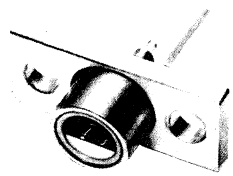
HL1221C is a 1.2 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in fiberoptic communications and various other types of optical equipment.

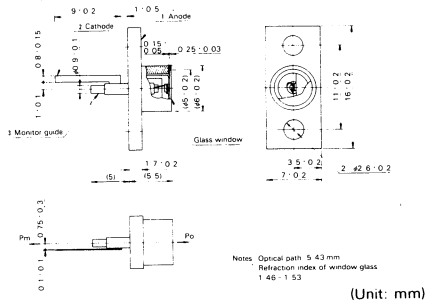
Monitoring power is output from the glass rod as optical output power.

Features

- Long wavelength light output: λ_p = 1170–1230 nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns



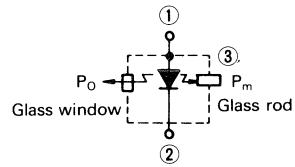
Package Dimensions



(Unit: mm)

C-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	−40 to +60	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1170	1200	1230	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HLP5400

InGaAsP LD

Description

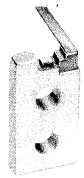
HLP5400 is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

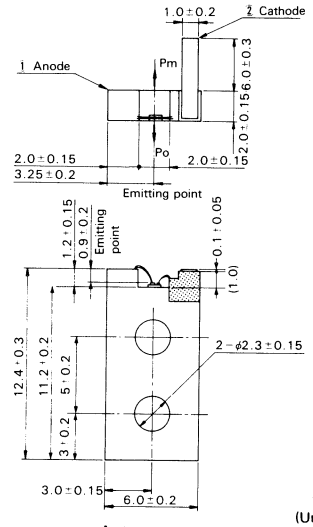
The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1270–1330 nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns



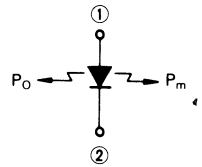
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	0 to +60	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th}$ + 20 mA
Monitor power	P_m	1			mW	$I_F = I_{th}$ + 20 mA
Lasing wavelength	λ_p	1270	1300	1330	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_\perp$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HLP5500

InGaAsP LD

Description

HLP5500 is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

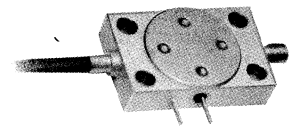
The laser beam is output from the connected optical fiber. Monitoring power is output from the glass rod as optical output power.

—Fiber specifications—

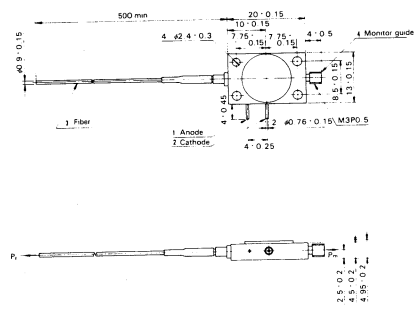
Numerical aperture	: 0.2
Core diameter	: 50 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Refraction index profile	: GI type
Fiber length	: More than 500 mm

Features

- Long wavelength light output: λ_p = 1270–1330 nm
- 1.2 mW CW operation at room temperature
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns



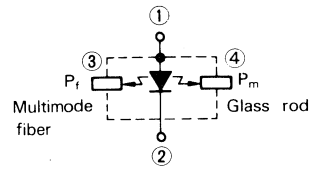
Package Dimensions



(Unit: mm)

B-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	−40 to +60	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Fiber optical output power	P_f	1.2			mW	Kink free
		0.4	0.7		mW	$I_F = I_{th}$ + 20 mA
Monitor power	P_m	0.05			mW	$I_F = I_{th}$ + 20 mA
Lasing wavelength	λ_p	1270	1300	1330	nm	P_f = 0.5 mW
Spectral width	$\Delta\lambda$		2		nm	P_f = 0.5 mW
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HLP5600

InGaAsP LD

Description

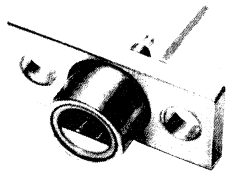
HLP5600 is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

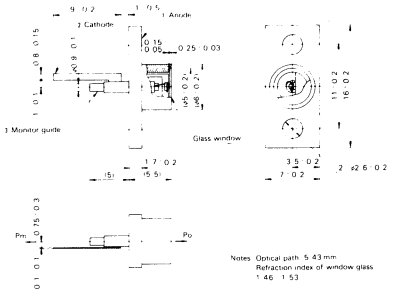
Monitoring power is output from the glass rod as optical output power.

Features

- Long wavelength light output: $\lambda_p = 1270-1330$ nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns



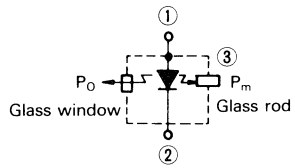
Package Dimensions



(Unit: mm)

C-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25°C$)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	−40 to +60	°C

Optical and Electrical Characteristics ($T_C = 25°C$)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1270	1300	1330	nm	$P_O = 3$ mW
Spectral width	$\Delta\lambda$		2		nm	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1321AC

InGaAsP LD

Description

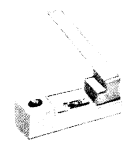
HL1321AC is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

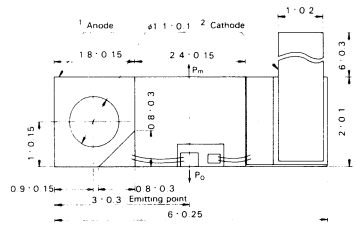
The package is compact to facilitate module assembly.

Features

- Long wavelength light output: λ_p = 1270–1330 nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns



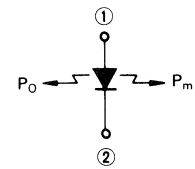
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1.0			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1270	1300	1330	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1321FG

—Under development—
InGaAsP LD

Description

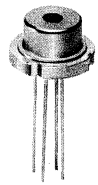
HL1321FG is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

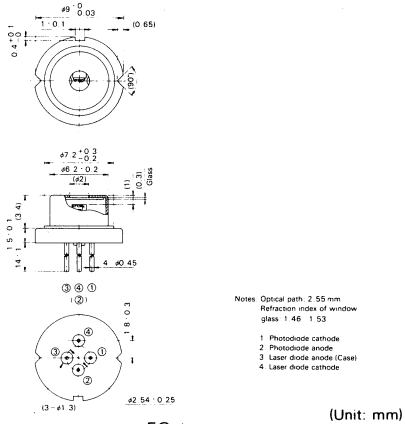
The laser beam is output through the glass window in the package cap. Monitoring current is output from a built-in photodiode.

Features

- Long wavelength light output: λ_p = 1290 – 1330 nm
- 5 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Fast pulse response: t_r, t_f ≦ 0.5 ns



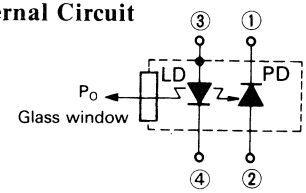
Package Dimensions



FG-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	100			μA	$V_{R(PD)}$ = 5 V, P_O = 3 mW
Photodiode capacitance	C_t		15	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r			0.5	ns	P_O = 3 mW, $I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f			0.5	ns	P_O = 3 mW, $I_{bias} = I_{th}$, 90 to 10%

HITACHI

HL1321P

InGaAsP LD

Description

HL1321P is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

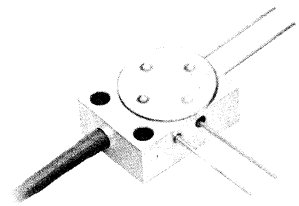
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

The laser beam is output from the connected multimode fiber. Monitoring current is output from a built-in photodiode.

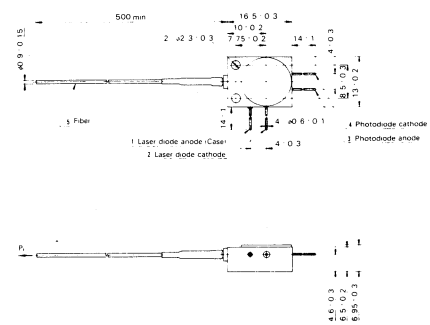
–Fiber specifications–	
Numerical aperture	: 0.2
Core diameter	: 50 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Refraction index profile	: GI type
Fiber length	: More than 500 mm

Features

- Long wavelength light output: λ_p = 1270–1330 nm
- 1.2 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns
- Built-in photodiode for monitoring laser output



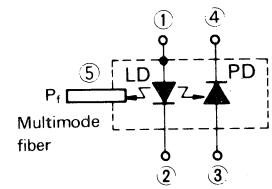
Package Dimensions



(Unit: mm)

P-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2.0	V
Photodiode reverse voltage	$V_{R(PD)}$	20	V
Photodiode forward current	$I_{F(PD)}$	1.0	mA
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	−40 to +60	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.2			mW	Kink free
		0.7			mW	$I_F = I_{th}$ + 20 mA
Lasing wavelength	λ_p	1270	1300	1330	nm	P_f = 0.5 mW
Spectral width	$\Delta\lambda$		2		nm	P_f = 0.5 mW
Photodiode dark current	I_{DARK}			150	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	70			μA	$V_{R(PD)}$ = 5 V, P_f = 1.0 mW
Photodiode capacitance	C_t		3.0	4.0	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1321SP

InGaAsP LD

Description

HL1321SP is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

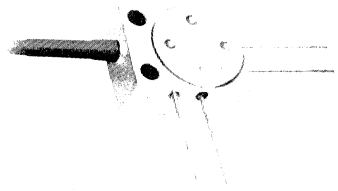
The laser beam is output from the connected single mode fiber. Monitoring current is output from a built-in photodiode.

—Fiber specifications—

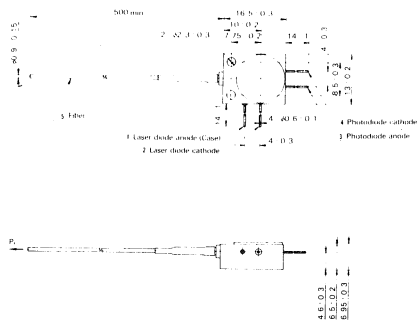
Spot size	: 5 μm
λ_c	: 1.10—1.28 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

Features

- Long wavelength light output: λ_p = 1270—1330 nm
- 1.2 mW CW operation at room temperature
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns
- Built-in photodiode for monitoring laser output



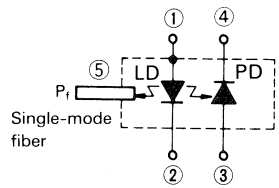
Package Dimensions



(Unit: mm)

SP-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2.0	V
Photodiode reverse voltage	$V_{R(PD)}$	20	V
Photodiode forward current	$I_{F(PD)}$	1.0	mA
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	−40 to +60	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.2			mW	Kink free
		0.6			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1270	1300	1330	nm	P_f = 1.0 mW
Spectral width	$\Delta\lambda$		2		nm	P_f = 0.5 mW
Photodiode dark current	I_{DARK}			150	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	140			μA	$V_{R(PD)}$ = 5 V, P_f = 1.0 mW
Photodiode capacitance	C_t		3.0	4.0	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1321BF

—Preliminary—
InGaAsP LD

Description

HL1321BF is a laser-diode module in a 14-pin butterfly-type package with a built-in thermoelectronic controller and connected single mode fiber.

It is suitable as a light source in high-speed modulated, high-bit-rate, long-distance fiberoptic communications equipment.

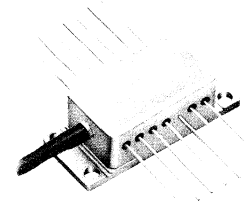
The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

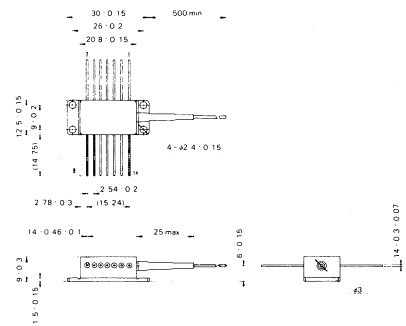
Spot size	: 5 μm
λ_c	: 1.10—1.28 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

Features

- Long wavelength light output: λ_p = 1290—1330 nm
- 1.2 mW CW and pulse operation at room temperature
- High-speed modulation (1.8 Gb/s)
- Stabilized operation with built-in thermoelectronic controller



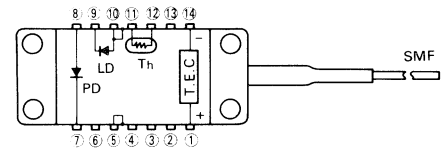
Package Dimensions



(Unit: mm)

BF-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode
② N. C.
③ N. C.
④ N. C.
⑤ Case
⑥ N. C.
⑦ PD cathode
⑧ PD anode
⑨ LD cathode
⑩ LD anode (case)
⑪ Thermistor
⑫ Thermistor
⑬ N. C.
⑭ T. E. C. cathode

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.2			mW	Kink free
		0.6			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	$P_f = 1.0$ mW
Spectral width	$\Delta\lambda$		2		nm	$P_f = 1.0$ mW
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)} = 5$ V
Monitor current	I_S	300			μA	$V_{R(PD)} = 5$ V, $P_f = 1.0$ mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)} = 5$ V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	$P_f = 1.0$ mW
Cooler current	I_C			1.4	A	$\Delta T = 40$°C
Cooler voltage	V_C			1.8	V	$\Delta T = 40$°C
Thermistor resistance	R_{TM}		10		kΩ	

HL1321DL

—Preliminary—
InGaAsP LD

Description

HL1321DL is a laser-diode module in a 14-pin dual-in-line type package with a built-in thermoelectronic controller and connected single-mode fiber.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

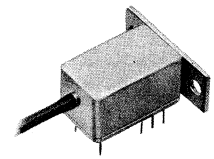
Spot size	: 5 μm
λ_c	: 1.10—1.28 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

Features

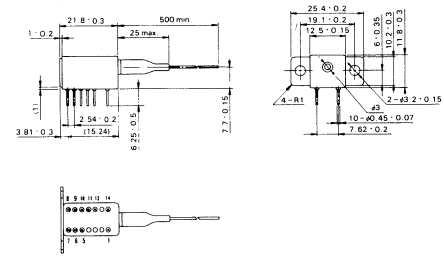
- Long wavelength light output: λ_p = 1290—1330 nm
- 1.2 mW CW and pulse operation at room temperature
- High-speed modulation (800 Mb/s)
- Stabilized operation with built-in thermoelectronic controller

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C



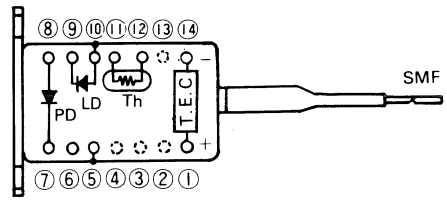
Package Dimensions



(Unit: mm)

DL-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode
② —
③ —
④ —
⑤ Case
⑥ N. C.
⑦ PD cathode
⑧ PD anode
⑨ LD cathode
⑩ LD anode (case)
⑪ Thermistor
⑫ Thermistor
⑬ —
⑭ T. E. C. cathode

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.2			mW	Kink free
		0.6			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_f = 1.0 mW
Spectral width	$\Delta\lambda$		2		nm	P_f = 1.0 mW
Rise time	t_r			0.5	ns	P_f = 1.0 mW, $I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f			0.5	ns	P_f = 1.0 mW, $I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	300			μA	$V_{R(PD)}$ = 5 V, P_f = 1.0 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	P_f = 1.0 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

HL1322A

InGaAsP LD

Description

HL1322A is a high-power 1.3 μm InGaAsP laser diode with double heterojunction structure.

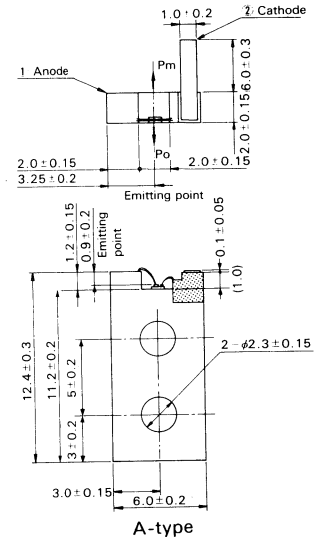
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment. The HL1322A emits higher optical power than HLP5400 and HL1321AC.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: $\lambda_p = 1290-1330$ nm
- 10 mW CW operation at room temperature
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns

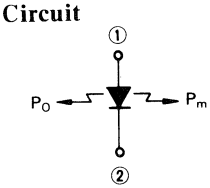
Package Dimensions



A-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings ($T_C = 25°C$)

Items	Symbols	Values	Units
Optical output power	P_O	10	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics ($T_C = 25°C$)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	10			mW	Kink free
		4			mW	$I_F = I_{th} + 40$ mA
Monitor power	P_m	2			mW	$I_F = I_{th} + 40$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	$P_O = 6$ mW
Spectral width	$\Delta\lambda$			5	nm	$P_O = 6$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 6$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 6$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1322AC

InGaAsP LD

Description

HL1322AC is a high-power 1.3 μm InGaAsP laser diode with double heterojunction structure.

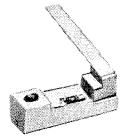
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The HL1322AC emits higher optical power than HLP5400 and HL1321AC.

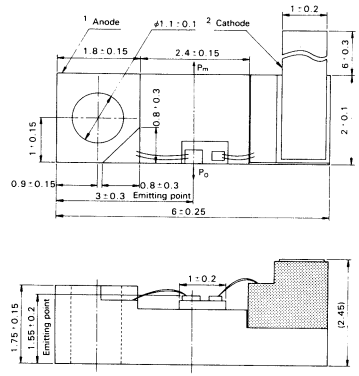
The package is compact to facilitate module assembly.

Features

- Long wavelength light output: λ_p = 1290–1330 nm
- 10 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns



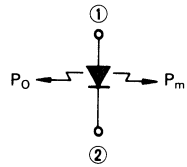
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	10	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	10			mW	Kink free
		4			mW	$I_F = I_{th} + 40$ mA
Monitor power	P_m	2			mW	$I_F = I_{th} + 40$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_O = 6 mW
Spectral width	$\Delta\lambda$			5	nm	P_O = 6 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 6 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_\perp$		40		deg.	P_O = 6 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1341A

—Preliminary—
InGaAsP LD

Description

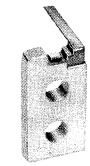
HL1341A is a 1.3 μm InGaAsP distributed-feedback (DFB) laser diode with buried heterostructure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

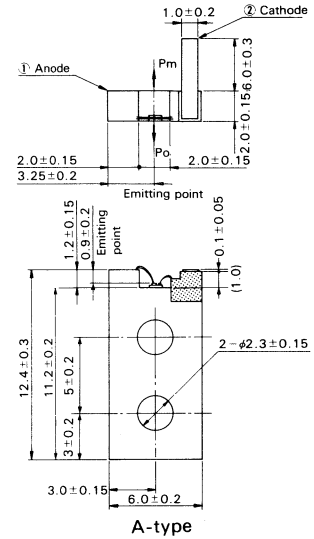
The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: $\lambda_p = 1280 - 1340$ nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns



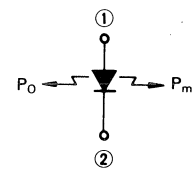
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25°C$)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics ($T_C = 25°C$)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1.0			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1280	1310	1340	nm	$P_O = 3$ mW
Side-mode suppression ratio	S_r		35		dB	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1341AC

—Preliminary—
InGaAsP LD

Description

HL1341AC is a 1.3 μm InGaAsP distributed-feedback (DFB) laser diode with buried heterostructure.

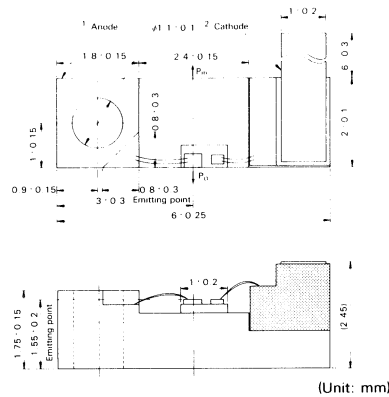
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is compact to facilitate module assembly.

Features

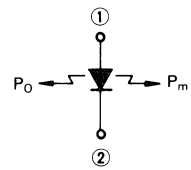
- Long wavelength light output: $\lambda_p = 1280-1340$ nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns

Package Dimensions



AC-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25°C$)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics ($T_C = 25°C$)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1.0			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1280	1310	1340	nm	$P_O = 3$ mW
Side-mode suppression ratio	S_r		35		dB	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_\perp$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1341FG

—Under development—
InGaAsP LD

Description

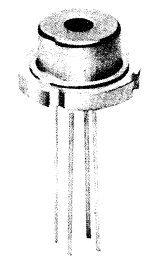
HL1341FG is a 1.3 μm InGaAsP distributed-feedback (DFB) laser diode with buried heterostructure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

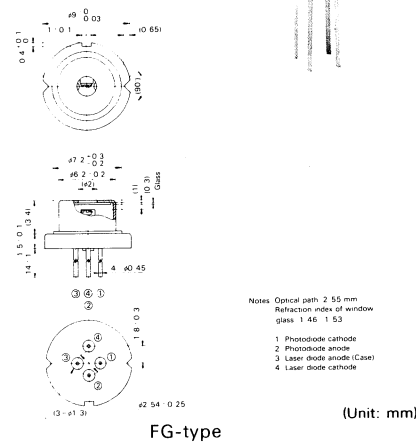
The laser beam is output through the glass window in the package cap. Monitoring current is output from a built-in photodiode.

Features

- Long wavelength light output: λ_p = 1280 – 1340 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode
- Built-in photodiode for monitoring laser output
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns



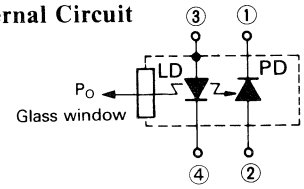
Package Dimensions



(Unit: mm)

FG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1280	1310	1340	nm	P_O = 3 mW
Side-mode suppression ratio	S_r		35		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_\perp$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	100			μA	$V_{R(PD)}$ = 5 V, P_O = 3 mW
Photodiode capacitance	C_t		15	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	

HL1341BF

—Under development—
InGaAsP LD

Description

HL1341BF is a laser-diode module in a 14-pin butterfly-type package with a built-in thermoelectronic controller and connected single-mode fiber.

It is suitable as a light source in high-speed modulated, high-bit-rate, long-distance fiberoptic communications equipment.

The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

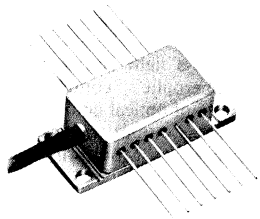
Spot size	: 5 μm
λ_c	: 1.10—1.28 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

Features

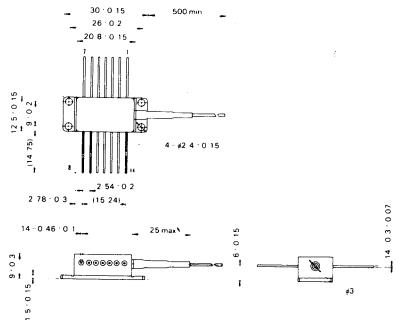
- Long wavelength light output: λ_p = 1280—1340 nm
- 1.2 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode
- High-speed modulation (1.8 Gb/s)
- Stabilized operation with built-in thermoelectronic controller

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	—40 to +80	°C



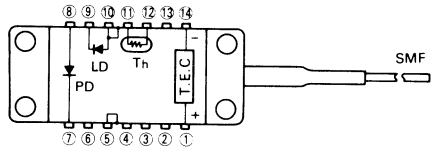
Package Dimensions



(Unit: mm)

BF-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode
② N. C.
③ N. C.
④ N. C.
⑤ Case
⑥ N. C.
⑦ PD cathode
⑧ PD anode
⑨ LD cathode
⑩ LD anode (case)
⑪ Thermistor
⑫ Thermistor
⑬ N. C.
⑭ T. E. C. cathode

HITACHI

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.0			mW	Kink free
		0.3			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1280	1310	1340	nm	P_f = 0.5 mW
Side-mode suppression ratio	S_r		35		dB	P_f = 0.5 mW, CW
Rise time	t_r		0.2		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.3		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	0.3			mA	$V_{R(PD)}$ = 5 V, P_f = 0.5 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	T_C = 60°C, P_f = 0.5 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

HL1341DL

—Under development—
InGaAsP LD

Description

HL1341DL is a laser-diode module in a 14-pin dual-in-line type package with a built-in thermoelectronic controller and connected single-mode fiber.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

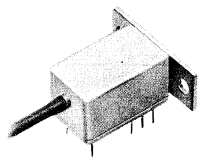
Spot size	: 5 μm
λ_c	: 1.10—1.28 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

Features

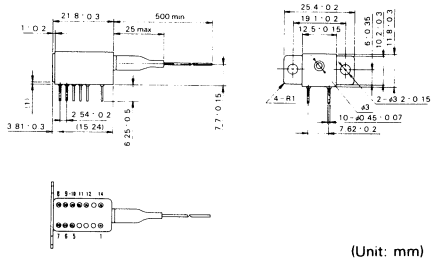
- Long wavelength light output: λ_p = 1280—1340 nm
- 1.2 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode
- High-speed modulation (800 Mb/s)
- Stabilized operation with built-in thermoelectronic controller

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C



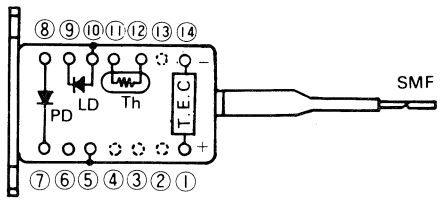
Package Dimensions



(Unit: mm)

DL-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode
② —
③ —
④ —
⑤ Case
⑥ N. C.
⑦ PD cathode
⑧ PD anode
⑨ LD cathode
⑩ LD anode (case)
⑪ Thermistor
⑫ Thermistor
⑬ —
⑭ T. E. C. cathode

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Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.0			mW	Kink free
		0.3			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1280	1310	1340	nm	P_f = 0.5 mW
Side-mode suppression ratio	S_r		35		dB	P_f = 0.5 mW, CW
Rise time	t_r		0.2		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.3		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	0.3			mA	$V_{R(PD)}$ = 5 V, P_f = 0.5 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	T_C = 60°C, P_f = 0.5 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

HL1521A

InGaAsP LD

Description

HL1521A is a 1.55 μm InGaAsP laser diode with double heterojunction structure.

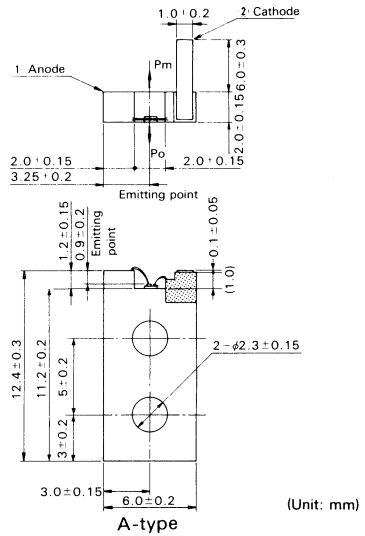
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1530–1570 nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns

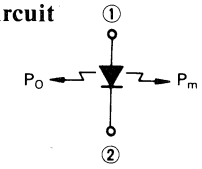
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.0			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.45			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1521AC

InGaAsP LD

Description

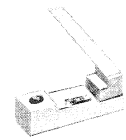
HL1521AC is a 1.55 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

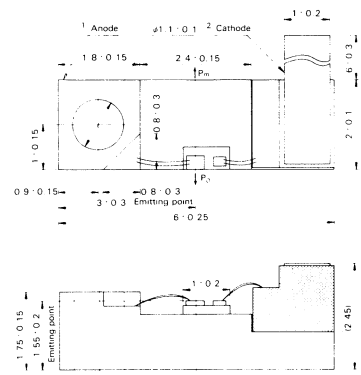
The package is compact to facilitate module assembly.

Features

- Long wavelength light output: $\lambda_p = 1530 - 1570$ nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns



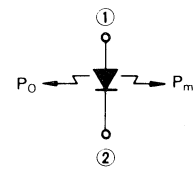
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.0			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1.0			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1541A

—Preliminary—
InGaAsP LD

Description

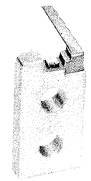
HL1541A is a 1.55 μm InGaAsP distributed-feedback (DFB) laser diode with buried heterostructure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

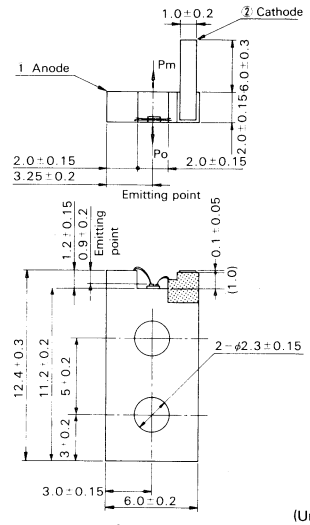
The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: $\lambda_p = 1520-1580$ nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns



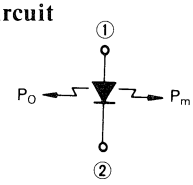
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25$°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics ($T_C = 25$°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1520	1550	1580	nm	$P_O = 3$ mW
Side-mode suppression ratio	S_r		35		dB	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

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HL1541AC

—Preliminary—
InGaAsP LD

Description

HL1541AC is a 1.55 μm InGaAsP distributed-feedback (DFB) laser diode with buried hetero-structure.

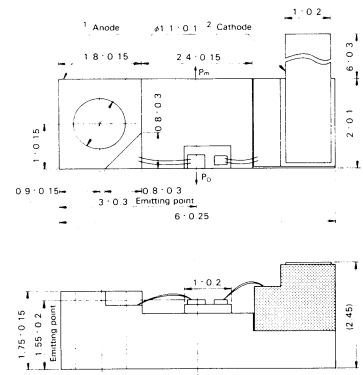
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is compact to facilitate module assembly.

Features

- Long wavelength light output: λ_p = 1520–1580 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns

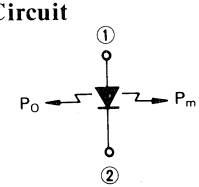
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1520	1550	1580	nm	P_O = 3 mW
Side-mode suppression ratio	S_r		35		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

HL1541FG

—Under development—
InGaAsP LD

Description

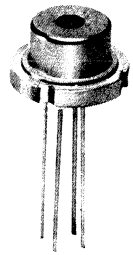
HL1541FG is a 1.55 μm InGaAsP distributed-feedback (DFB) laser diode with buried heterostructure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

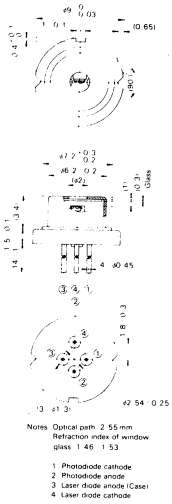
The laser beam is output through the glass window in the package. Monitoring current is output from a built-in photodiode.

Features

- Long wavelength light output:
  $\lambda_p = 1520 - 1580$ nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode
- Built-in photodiode for monitoring laser output
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns



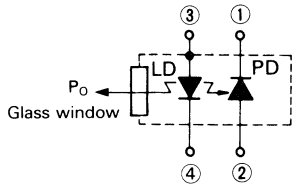
Package Dimensions



FG-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings ($T_C = 25$°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics ($T_C = 25°C$)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1520	1550	1580	nm	$P_O = 3$ mW
Side-mode suppression ratio	S_r		35		dB	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)} = 5$ V
Monitor current	I_S	100			μA	$V_{R(PD)} = 5$ V, $P_O = 3$ mW
Photodiode capacitance	C_t		15	20	pF	$V_{R(PD)} = 5$ V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	

HL1541BF

—Under development—
InGaAsP LD

Description

HL1541BF is a laser-diode module in a 14-pin butterfly-type package with a built-in thermoelectronic controller and connected single mode fiber.

It is suitable as a light source in high-speed modulated, high-bit-rate, long-distance fiberoptic communications equipment.

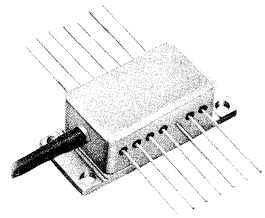
The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

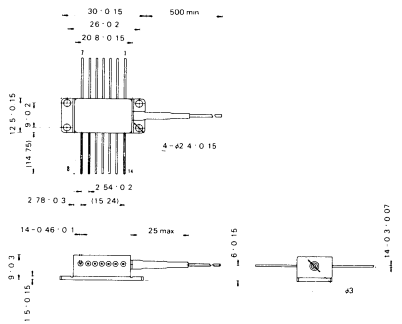
Spot size	: 5 μm
λ_c	: 1.10—1.28 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

Features

- Long wavelength light output: λ_p = 1520—1580 nm
- 1.2 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode
- High-speed modulation (1.8 Gb/s)
- Stabilized operation with built-in thermoelectronic controller



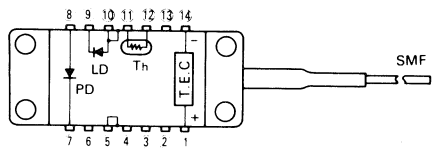
Package Dimensions



(Unit: mm)

BF-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode
② N. C.
③ N. C.
④ N. C.
⑤ Case
⑥ N. C.
⑦ PD cathode
⑧ PD anode
⑨ LD cathode
⑩ LD anode (case)
⑪ Thermistor
⑫ Thermistor
⑬ N. C.
⑭ T. E. C. cathode

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.0			mW	Kink free
		0.3			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1520	1550	1580	nm	P_f = 0.5 mW
Side-mode suppression ratio	S_r		35		dB	P_f = 0.5 mW, CW
Rise time	t_r		0.2		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.3		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	0.3			mA	$V_{R(PD)}$ = 5 V, P_f = 0.5 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	T_C = 60°C, P_f = 0.5 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

HL1541DL

—Under development—
InGaAsP LD

Description

HL1541DL is a laser-diode module in a 14-pin dual-in-line type package with a built-in thermoelectronic controller and connected single mode fiber.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

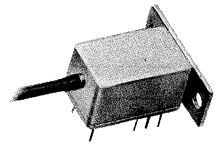
The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

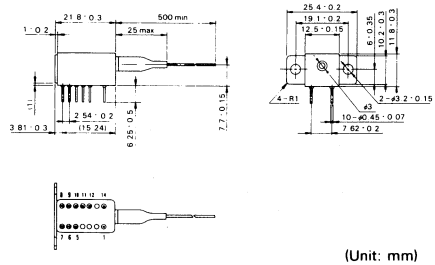
Spot size	: 5 μm
λ_c	: 1.10—1.28 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

Features

- Long wavelength light output: λ_p = 1520—1580 nm
- 1.2 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode
- High-speed modulation (800 Mb/s)
- Stabilized operation with built-in thermoelectronic controller



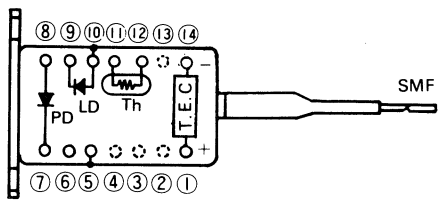
Package Dimensions



(Unit: mm)

DL-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode
② —
③ —
④ —
⑤ Case
⑥ N. C.
⑦ PD cathode
⑧ PD anode
⑨ LD cathode
⑩ LD anode (case)
⑪ Thermistor
⑫ Thermistor
⑬ —
⑭ T. E. C. cathode

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

HITACHI

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.0			mW	Kink free
		0.3			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1520	1550	1580	nm	$P_f = 0.5$ mW
Side-mode suppression ratio	S_r		35		dB	$P_f = 0.5$ mW, CW
Rise time	t_r		0.2		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.3		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)} = 5$ V
Monitor current	I_S	0.3			mA	$V_{R(PD)} = 5$ V, $P_f = 0.5$ mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)} = 5$ V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	$T_C = 60$°C, $P_f = 0.5$ mW
Cooler current	I_C			1.4	A	$\Delta T = 40$°C
Cooler voltage	V_C			1.8	V	$\Delta T = 40$°C
Thermistor resistance	R_{TM}		10		kΩ	

Description

HLP20R, HLP30R, HLP40R, HLP50R and HLP60R are GaAlAs infrared emitting diodes with single heterojunction structure.

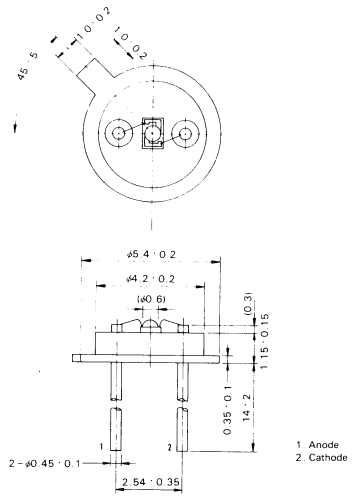
They offer a wide range of wavelength and output power, and are suitable for various types of optical equipment.

The package should be hermetically sealed before mounting on a system.

Features

- High efficiency
- Selection from a wide range of wavelength and output power
- Narrow spectral width

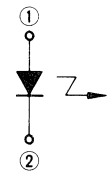
Package Dimensions



(Unit: mm)

R-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	250	mA
		230*	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	600	mW
Operating temperature	T_{opr}	−20 to +40**	°C
Storage temperature	T_{stg}	−40 to +60**	°C

* Value for devices with λ_p from 735 nm to 785 nm.
** Value for conditions without condensation.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O		**		mW	I_F = 200 mA
Peak wavelength	λ_p		**		nm	I_F = 200 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 200 mA
Beam divergence	θ_H		180		deg.	I_F = 200 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 200 mA
			2.0*	2.6*	V	I_F = 200 mA
Reverse current	I_R			30	μA	V_R = 3 V
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		12		ns	I_F = 50 mA
			20*		ns	I_F = 50 mA
Fall time	t_f		12		ns	I_F = 50 mA
			20*		ns	I_F = 50 mA

* Value for devices with λ_p from 735 nm to 785 nm.
** HLP20R-HLP60R are grouped with λ_p and P_O as follows.

	λ_p (nm)			P_O (mW)				
Grades	min.	typ.	max.	15 (min.)	25 (min.)	35 (min.)	45 (min.)	55 (min.)
A	735	760	785	HLP20R	HLP30R	HLP40R		
B	775	800	825		HLP30R	HLP40R	HLP50R	HLP60R
C	815	840	865		HLP30R	HLP40R	HLP50R	HLP60R
D	855	880	905		HLP30R	HLP40R	HLP50R	HLP60R

Description

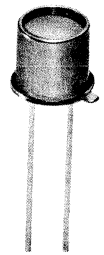
HLP20RG, HLP30RG, HLP40RG, HLP50RG and HLP60RG are GaAlAs infrared emitting diodes with single heterojunction structure.

They offer a wide range of wavelength and output power, and are suitable for various types of optical equipment.

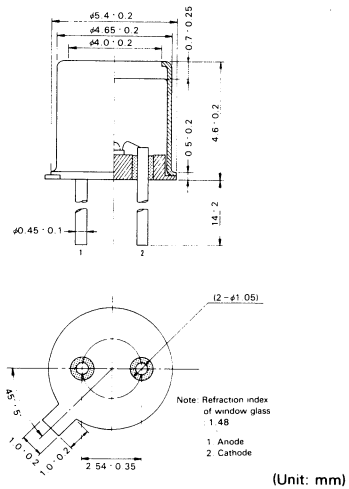
Hermetic sealing of the package achieves high reliability.

Features

- High efficiency
- Selection from a wide range of wavelength and output power
- Narrow spectral width



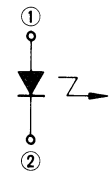
Package Dimensions



(Unit: mm)

RG-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25°C$)

Items	Symbols	Values	Units
Forward current	I_F	250	mA
		230*	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	600	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

* Value for devices with λ_p from 735 nm to 785 nm.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O		**		mW	I_F = 200 mA
Peak wavelength	λ_p		**		nm	I_F = 200 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 200 mA
Beam divergence	θ_H		120		deg.	I_F = 200 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 200 mA
			2.0*	2.6*	V	I_F = 200 mA
Reverse current	I_R			30	μA	V_R = 3 V
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		12		ns	I_F = 50 mA
			20*		ns	I_F = 50 mA
Fall time	t_f		12		ns	I_F = 50 mA
			20*		ns	I_F = 50 mA

* Value for devices with λ_p from 735 nm to 785 nm.
** HLP20RG-HLP60RG are grouped with λ_p and P_O as follows.

	λ_p (nm)			P_O (mW)				
Grades	min.	typ.	max.	7 (min.)	12 (min.)	17 (min.)	22 (min.)	27 (min.)
A	735	760	785	HLP20RG	HLP30RG	HLP40RG		
B	775	800	825		HLP30RG	HLP40RG	HLP50RG	HLP60RG
C	815	840	865		HLP30RG	HLP40RG	HLP50RG	HLP60RG
D	855	880	905		HLP30RG	HLP40RG	HLP50RG	HLP60RG

HE8402F

GaAlAs IRED

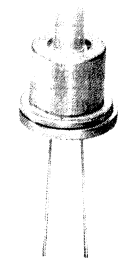
Description

HE8402F is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure, which provides high speed response.

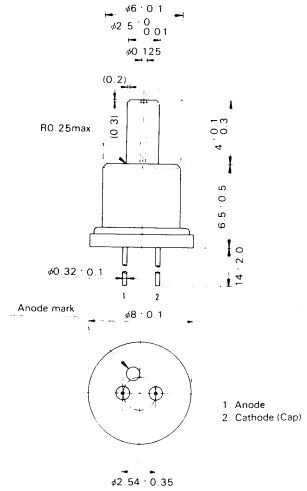
The package can be easily connected to optical fiber, and is suitable as a light source in fiberoptic communications equipment.

Features

- Optical fiber rod (50 μm of core dia., GI) included in ferrule (2.5 mm dia.)
- Ease in fiber coupling
- High frequency response
- Excellent light-current linearity



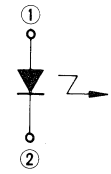
Package Dimensions



(Unit: mm)

F-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	40	60		μW	I_F = 100 mA
Peak wavelength	λ_p	800	840	900	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 100 mA
Forward voltage	V_F			2.5	V	I_F = 100 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

* At GI 50/125 fiber end.

HE8403R

GaAlAs IRED

Description

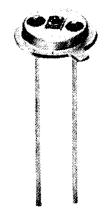
HE8403R is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure, which provides high speed response.

Optical fiber can be close to the chip, achieving high coupling efficiency; suitable as a light source in fiberoptic communications equipment.

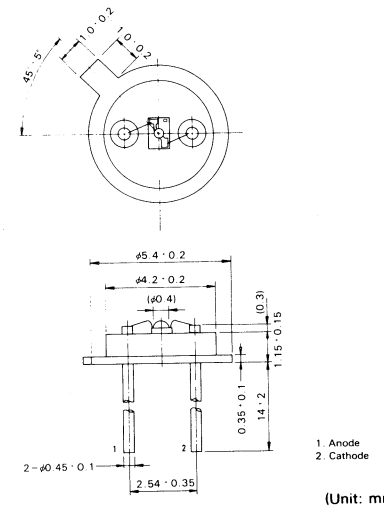
The package should be hermetically sealed before mounting on a system.

Features

- High efficiency and high brightness output
- High frequency response
- Excellent light-current linearity



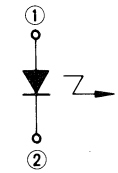
Package Dimensions



(Unit: mm)

R-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +40*	°C
Storage temperature	T_{stg}	−40 to +60*	°C

* Value for conditions without condensation.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	50	80		μW	I_F = 100 mA
Peak wavelength	λ_p	800	840	900	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 100 mA
Forward voltage	V_F			2.5	V	I_F = 100 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

* At GI 50/125 fiber end.

HE8403SG

GaAlAs IRED

Description

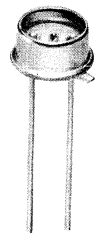
HE8403SG is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure, which provides high speed response.

High coupling efficiency can be realized using a rod lens; suitable as a light source in fiberoptic communications equipment.

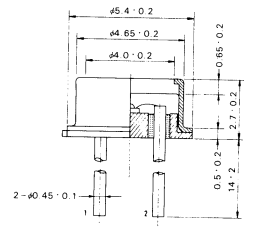
Hermetic sealing of the package achieves high reliability.

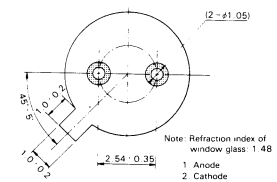
Features

- High efficiency and high brightness output
- High frequency response
- Excellent light-current linearity



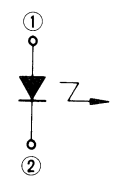
Package Dimensions





SG-type (Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	40	80		µW	I_F = 100 mA
Peak wavelength	λ_p	800	840	900	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 100 mA
Forward voltage	V_F			2.5	V	I_F = 100 mA
Reverse current	I_R			100	µA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

* At GI 50/125 fiber end through rod lens.

HE8403ML

GaAlAs IRED

Description

HE8403ML is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure, which provides high speed response.

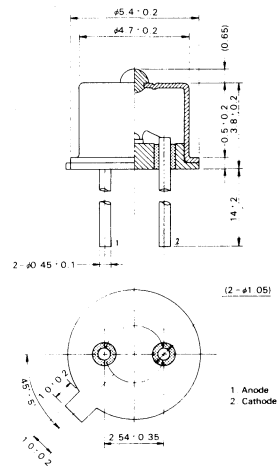
Optical output from the chip is directed to the optical fiber efficiently through the microlens in the cap; suitable as a light source in fiberoptic communications equipment.

Hermetic sealing of the package achieves high reliability.

Features

- High efficiency and high brightness output
- High frequency response
- Excellent light-current linearity

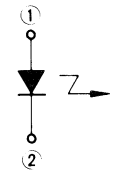
Package Dimensions



(Unit: mm)

ML-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	50	80		μW	I_F = 100 mA
Peak wavelength	λ_p	800	840	900	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 100 mA
Forward voltage	V_F			2.5	V	I_F = 100 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

* At GI 50/125 fiber end.

HE8801

GaAlAs IRED

Description

HE8801 is a 0.8 μm GaAlAs infrared emitting diode with single heterojunction structure.

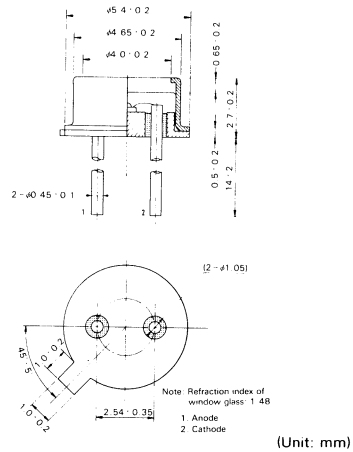
Wide radiant directionality makes it suitable as a light source in various types of optical equipment.

Hermetic sealing of the package achieves high reliability.

Features

- High efficiency and high power output
- Narrow spectral width
- Wide radiant directionality

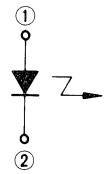
Package Dimensions



(Unit: mm)

SG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	400	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	6	20		mW	I_F = 150 mA
Peak wavelength	λ_p	800	880	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 150 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		12		ns	I_F = 50 mA
Fall time	t_f		12		ns	I_F = 50 mA

HE8807SG

—Preliminary—
GaAlAs IRED

Description

HE8807SG is a 0.8 μm GaAlAs infrared emitting diode with single heterojunction structure.

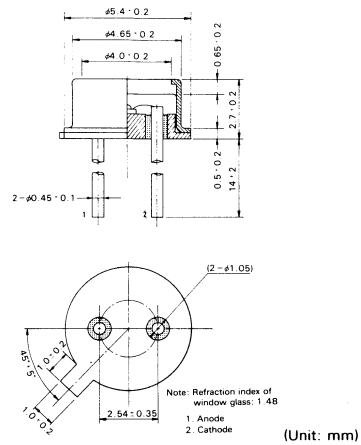
Radiant directionality is narrow and radiant intensity is high; suitable as a light source in encoders and sensors.

Hermetic sealing of the package achieves high reliability.

Features

- High efficiency and high power output
- Narrow spectral width

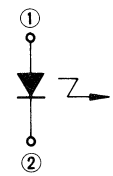
Package Dimensions



(Unit: mm)

SG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	10	20		mW	I_F = 150 mA
Peak wavelength	λ_p	800	880	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 150 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		20		ns	I_F = 50 mA
Fall time	t_f		20		ns	I_F = 50 mA

HE8807SL

—Preliminary—
GaAlAs IRED

Description

HE8807SL is a 0.8 μm GaAlAs infrared emitting diode with single heterojunction structure.

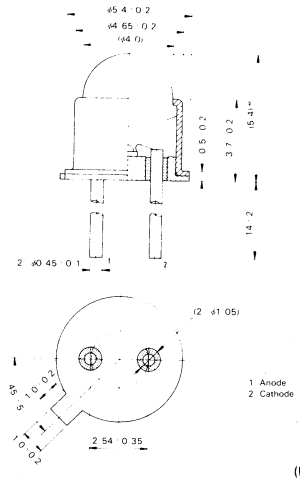
Radiant directionality is narrow and radiant intensity is high; suitable as a light source in encoders and sensors.

The package is hermetically sealed with the cap and lens, achieving high reliability.

Features

- High efficiency and high power output
- Narrow spectral width

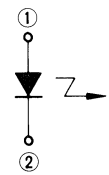
Package Dimensions



(Unit: mm)

SL-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +80	°C
Storage temperature	T_{stg}	−40 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	5	15		mW	I_F = 150 mA
Peak wavelength	λ_p	800	880	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 150 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		20		ns	I_F = 50 mA
Fall time	t_f		20		ns	I_F = 50 mA

HE8811

GaAlAs IRED

Description

HE8811 is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure. High brightness output, high power output and high speed response can be obtained.

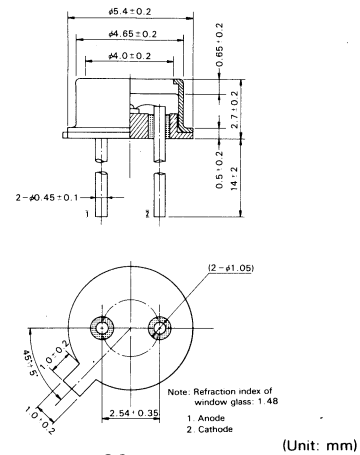
It is suitable as a light source in measuring and beam communications equipment.

Hermetic sealing of the package achieves high reliability.

Features

- High frequency response
- High power output, high efficiency and high brightness output
- No radiant directionality

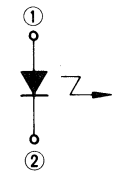
Package Dimensions



(Unit: mm)

SG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	400	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	20	30		mW	I_F = 150 mA
Peak wavelength	λ_p	780	820	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 150 mA
Forward voltage	V_F			2.5	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

HE1301R

InGaAsP IRED

Description

HE1301R is a 1.3 μm InGaAsP infrared emitting diode with double heterojunction structure, which provides high speed response.

It is suitable as a light source in high-speed digital link (up to 200 Mb/s) of fiberoptic communications equipment.

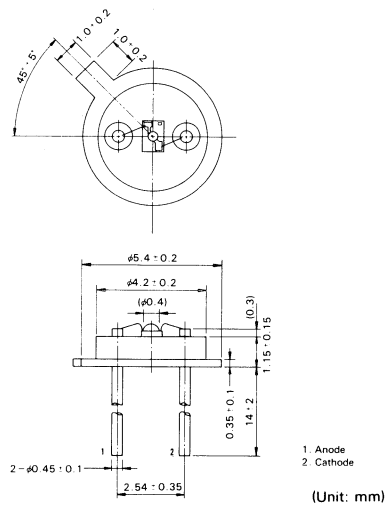
Optical fiber can be close to the chip, achieving high coupling efficiency.

The package should be hermetically sealed before mounting on a system.

Features

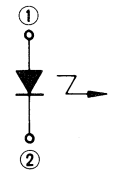
- High power output
- High efficiency and high brightness output
- Fast pulse response

Package Dimensions



R-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	1.0	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +40*	°C
Storage temperature	T_{stg}	−40 to +60*	°C

* Value for conditions without condensation.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	15			μW	I_F = 100 mA
Peak wavelength	λ_p	1260	1300	1340	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		140		nm	I_F = 100 mA
Forward voltage	V_F		1.5	2.0	V	I_F = 100 mA
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		1.5		ns	I_F = 100 mA
Fall time	t_f		4.0		ns	I_F = 100 mA

* At GI 50/125 fiber end.

HE1301SG

InGaAsP IRED

Description

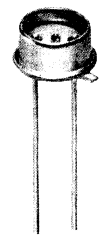
HE1301SG is a 1.3 μm InGaAsP infrared emitting diode with double heterojunction structure, which provides high speed response.

High coupling efficiency can be realized using a rod lens; suitable as a light source in fiberoptic communications equipment.

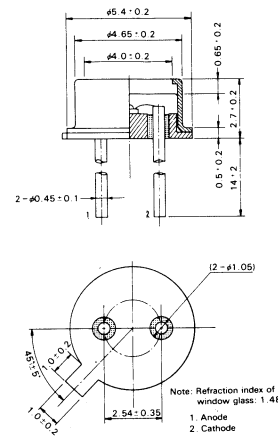
Hermetic sealing of the package achieves high reliability.

Features

- High power output
- High efficiency and high brightness output
- Fast pulse response



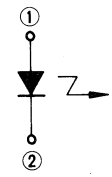
Package Dimensions



(Unit: mm)

SG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	1.0	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	15			µW	I_F = 100 mA
Peak wavelength	λ_p	1260	1300	1340	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		140		nm	I_F = 100 mA
Forward voltage	V_F		1.5	2.0	V	I_F = 100 mA
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		1.5		ns	I_F = 100 mA
Fall time	t_f		4.0		ns	I_F = 100 mA

* At GI 50/125 fiber end.

HE1301ML

InGaAsP IRED

Description

HE1301ML is a 1.3 μm InGaAsP infrared emitting diode with double heterojunction structure, which provides high speed response.

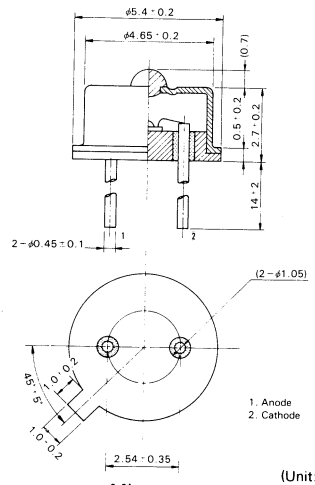
Optical output from the chip is directed to the optical fiber efficiently through the microlens in the cap; suitable as a light source in fiberoptic communications equipment.

Hermetic sealing of the package achieves high reliability.

Features

- High power output
- High efficiency and high brightness output
- Fast pulse response

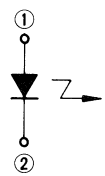
Package Dimensions



ML-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	1.0	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	15			μW	I_F = 100 mA
Peak wavelength	λ_p	1260	1300	1340	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		140		nm	I_F = 100 mA
Forward voltage	V_F		1.5	2.0	V	I_F = 100 mA
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		1.5		ns	I_F = 100 mA
Fall time	t_f		4.0		ns	I_F = 100 mA

* At GI 50/125 fiber end.

HE1302ML

—Preliminary—
InGaAsP IRED

Description

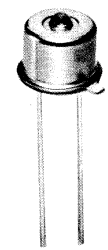
HE1302ML is a high-power 1.3 μm InGaAsP infrared emitting diode with double heterojunction structure, which provides high speed response.

Optical output from the chip is directed to the optical fiber efficiently through the microlens in the cap; suitable as a light source in fiberoptic communications equipment.

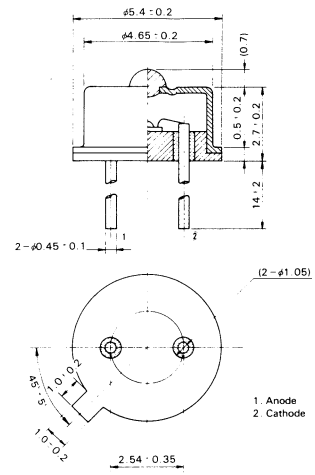
Hermetic sealing of the package achieves high reliability.

Features

- High power output
- High efficiency and high brightness output
- Fast pulse response



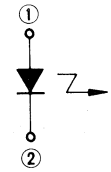
Package Dimensions



(Unit: mm)

ML-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	1.0	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	30			μW	I_F = 100 mA
Peak wavelength	λ_p	1260	1300	1340	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		140		nm	I_F = 100 mA
Forward voltage	V_F		1.5	2.0	V	I_F = 100 mA
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		1.5		ns	I_F = 100 mA
Fall time	t_f		4.0		ns	I_F = 100 mA

* At GI 50/125 fiber end.

HR8101

Si PIN Photodiode

Description

HR8101 is a Si PIN photodiode for detecting 0.6 – 0.9 μm light.

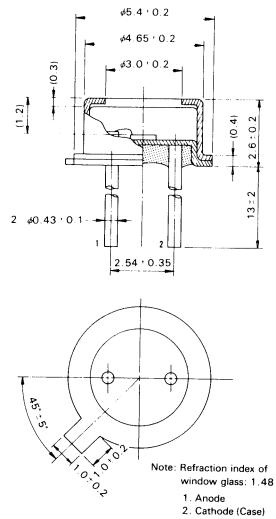
It is suitable as an optical monitor in measuring and fiberoptic communications and various other types of optical equipment.

Hermetic sealing of the package achieves high reliability.

Features

- High speed pulse response: t_r, t_f = 30 ns typ.
- Photodetectable area: 0.8 × 0.8 mm$^{\square}$

Package Dimensions

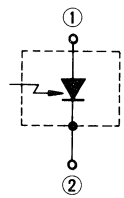


Note: Refraction index of window glass: 1.48
1. Anode
2. Cathode (Case)

(Unit: mm)

QG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	100	V
Forward current	I_F	100	mA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		2	10	nA	V_R = 10 V
Capacitance	C_t		10	15	pF	V_R = 10 V, f = 1 MHz
Sensitivity	S	0.4			mA/mW	V_R = 10 V, λ_p = 830 nm
Rise time	t_r		30		ns	V_R = 10 V, λ_p = 830 nm, R_L = 50 Ω
Fall time	t_f		30		ns	V_R = 10 V, λ_p = 830 nm, R_L = 50 Ω

HITACHI

HR8102

Si PIN Photodiode

Description

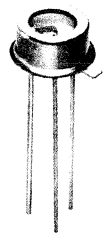
HR8102 is a Si PIN photodiode for detecting 0.6–0.9 μm light.

Its high speed pulse response makes it especially suitable as an optical signal detector in high-bit-rate fiberoptic communications equipment.

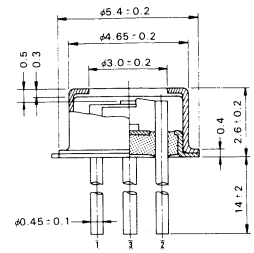
Hermetic sealing of the package achieves high reliability.

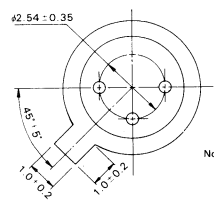
Features

- High sensitivity to wide wavelength range
- High speed pulse response: t_r, t_f = 1 ns typ.
- 5 V of low voltage operation
- Photodetectable area: 300 μm dia.



Package Dimensions





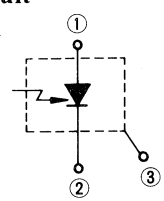
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	100	V
Forward current	I_F	100	mA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		0.5	3	nA	V_R = 10 V
Capacitance	C_t		1.5	3	pF	V_R = 10 V, f = 1 MHz
Sensitivity	S	0.4			mA/mW	V_R = 10 V, λ_p = 830 nm
Rise time	t_r		1.0		ns	V_R = 10 V, λ_p = 830 nm, R_L = 50 Ω
Fall time	t_f		1.0		ns	V_R = 10 V, λ_p = 830 nm, R_L = 50 Ω

HR8202TG

—Preliminary—
Si Avalanche Photodiode

Description

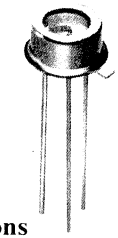
HR8202TG is a Si avalanche photodiode for detecting 0.6–0.9 μm light.

Its high frequency characteristics make it especially suitable as an optical signal detector in analog fiberoptic communications equipment.

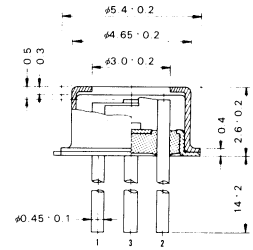
Hermetic sealing of the package achieves high reliability.

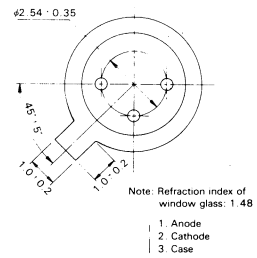
Features

- High quantum efficiency: More than 70%
- High speed response : More than 300 MHz
- Low dark current : Less than 3 nA
- Low operation voltage : Less than 200 V
- Photodetectable area : 300 μm dia.



Package Dimensions

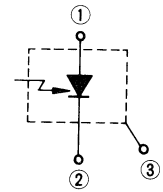




(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	100	mA
Reverse current	I_R	200	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		0.5	3	nA	$V_R = 0.9 \times V_B$
Quantum efficiency	η	70			%	V_R = 150 V, λ_p = 830 nm
Breakdown voltage	V_B	150		200	V	I_{DARK} = 100 μA
Multiplication factor	M	30				$V_R = 0.9 \times V_B$, λ_p = 830 nm
Capacitance	C_t		1.5		pF	V_R = 150 V, f = 1 MHz

HITACHI

HR1101 InGaAsP PIN Photodiode

Description

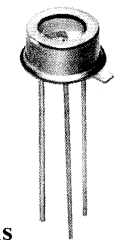
HR1101 is an InGaAsP PIN photodiode for detecting 1.0 – 1.5 μm light.

Its high-speed pulse response makes it especially suitable as a light signal detector in high-bit-rate fiberoptic communications equipment.

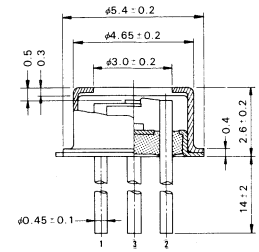
Hermetic sealing of the package achieves high reliability.

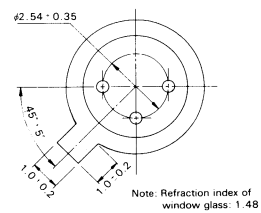
Features

- Fast pulse response : t_r, t_f = 0.5 ns typ.
- High sensitivity : S ≧ 0.45 mA/mW
- Low dark current : I_{DARK} = 7 nA typ.
- Small capacitance : C_t = 2.0 pF typ.
- Photodetectable area : 100 μm dia.



Package Dimensions



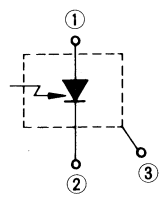


1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		7	200	nA	V_R = 10 V
Capacitance	C_t		2.0	3.0	pF	V_R = 10 V, f = 1 MHz
Sensitivity	S	0.45	0.7		mA/mW	V_R = 10 V, λ_p = 1300 nm P_{in} = 1.0 mW
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		0.5		ns	V_R = 10 V, λ_p = 1300 nm R_L = 50 Ω
Fall time	t_f		0.5		ns	V_R = 10 V, λ_p = 1300 nm R_L = 50 Ω

HR1102 InGaAsP PIN Photodiode

Description

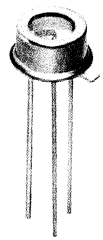
HR1102 is an InGaAsP PIN photodiode for detecting 1.0–1.5 μm light.

It is suitable as an optical monitor in high-bit-rate fiberoptic communications equipment.

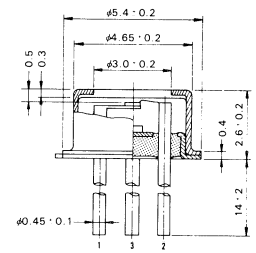
Hermetic sealing of the package achieves high reliability.

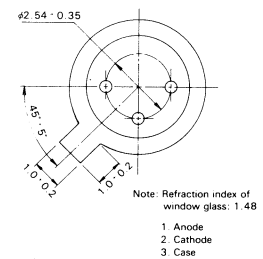
Features

- High sensitivity : S ≧ 0.45 mA/mW
- Low dark current : I_{DARK} = 20 nA typ.
- Photodetectable area : 300 μm dia.



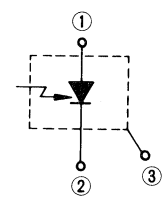
Package Dimensions





TG-type (Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	15	V
Forward current	I_F	1.0	mA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		20	500	nA	V_R = 10 V
Capacitance	C_t		9	15	pF	V_R = 10 V, f = 1 MHz
Sensitivity	S	0.45	0.7		mA/mW	V_R = 10 V, λ_p = 1300 nm P_{in} = 1.0 mW
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		1.2		ns	V_R = 10 V, λ_p = 1300 nm R_L = 50 Ω
Fall time	t_f		1.2		ns	V_R = 10 V, λ_p = 1300 nm R_L = 50 Ω

HR1102CX

InGaAsP PIN Photodiode

Description

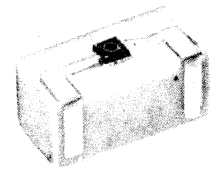
HR1102CX is an InGaAsP PIN photodiode for detecting 1.0–1.5 μm light.

It is suitable as an optical monitor in high-bit-rate fiberoptic communications equipment.

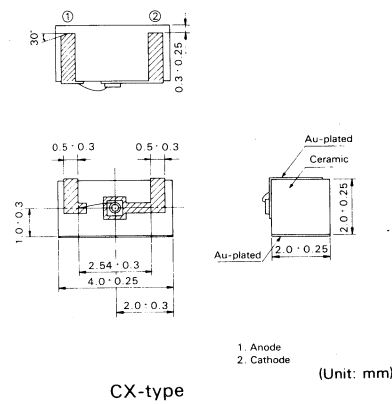
The package is compact for ease in module assembly.

Features

- High sensitivity : S ≧ 0.6 mA/mW
- Low dark current : I_{DARK} = 20 nA typ.
- Photodetectable area : 300 μm dia.



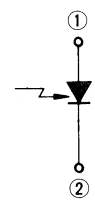
Package Dimensions



(Unit: mm)

CX-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	15	V
Forward current	I_F	1.0	mA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−40 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		20	100	nA	V_R = 10 V
Capacitance	C_t		10		pF	V_R = 10 V, f = 1 MHz
Sensitivity	S	0.6	0.7		mA/mW	V_R = 10 V, λ_p = 1300 nm P_{in} = 1.0 mW
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		1.2		ns	V_R = 10 V, λ_p = 1300 nm R_L = 50 Ω
Fall time	t_f		1.2		ns	V_R = 10 V, λ_p = 1300 nm R_L = 50 Ω

HR1103TG

—Preliminary—
InGaAs PIN Photodiode

Description

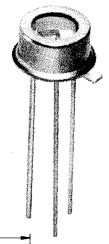
HR1103TG is an InGaAs PIN photodiode for detecting 1.0 – 1.65 μm light.

Its high speed pulse response makes it suitable as an optical signal detector in high-bit-rate fiber-optic communications equipment.

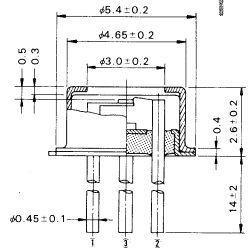
Hermetic sealing of the package achieves high reliability.

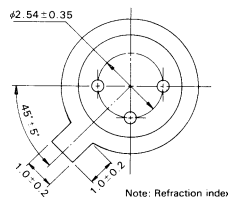
Features

- Fast pulse response : t_r, t_f = 0.5 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 1 nA typ.
- Small capacitance : C_t = 1.0 pF typ.
- Photodetectable area : 100 μm dia.



Package Dimensions





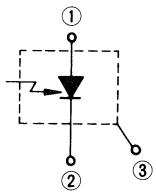
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		1	20	nA	V_R = 5 V
Capacitance	C_t		1.0	1.5	pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

HITACHI

HR1103CX

—Preliminary—
InGaAs PIN Photodiode

Description

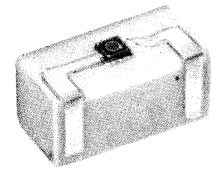
HR1103CX is an InGaAs PIN photodiode for detecting 1.0—1.65 μm light.

Its high speed pulse response makes it suitable as an optical signal detector in high-bit-rate fiber-optic communications equipment.

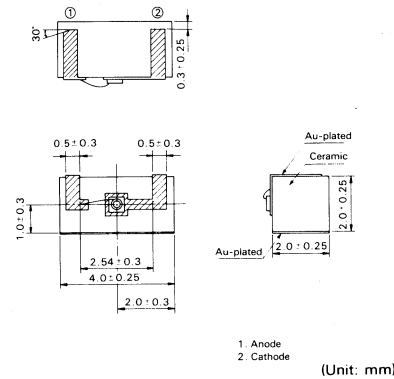
The package is compact for ease in module assembly.

Features

- Fast pulse response : t_r, t_f = 0.5 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 1 nA typ.
- Small capacitance : C_t = 1.2 pF typ.
- Photodetectable area : 100 μm dia.



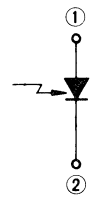
Package Dimensions



(Unit: mm)

CX-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−40 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		1	50	nA	V_R = 5 V
Capacitance	C_t		1.2	2.0	pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

HR1104TG

—Preliminary—
InGaAs PIN Photodiode

Description

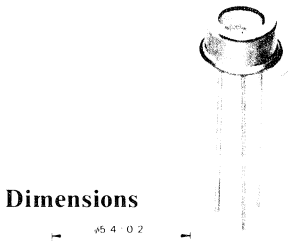
HR1104TG is an InGaAs PIN photodiode for detecting 1.0—1.65 μm light.

It is suitable as an optical monitor in high-bit-rate fiberoptic communications equipment.

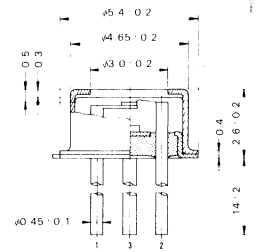
Hermetic sealing of the package achieves high reliability.

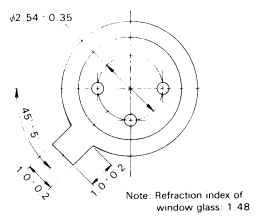
Features

- Fast pulse response : t_r, t_f = 1.0 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 5 nA typ.
- Small capacitance : C_t = 5 pF typ.
- Photodetectable area : 300 μm dia.



Package Dimensions





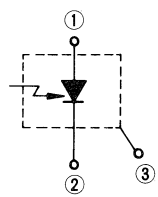
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		5	100	nA	V_R = 5 V
Capacitance	C_t		5	10	pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		1.0		ns	V_R = 5 V, λ_p = 1300 nm R_L = 50 Ω
Fall time	t_f		1.0		ns	V_R = 5 V, λ_p = 1300 nm R_L = 50 Ω

HITACHI

HR1104CX

—Preliminary—

InGaAs PIN Photodiode

Description

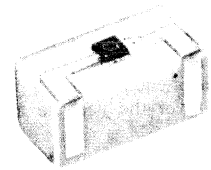
HR1104CX is an InGaAs PIN photodiode for detecting 1.0—1.65 μm light.

It is suitable as an optical monitor in high-bit-rate fiberoptic communications equipment.

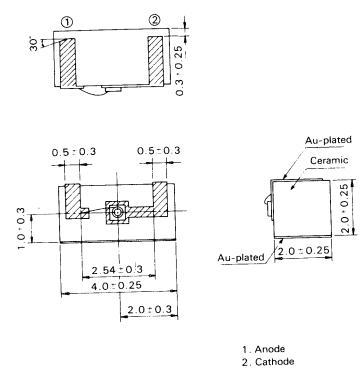
The package is compact for ease in module assembly.

Features

- Fast pulse response : t_r, t_f = 1.0 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 5 nA typ.
- Small capacitance : C_t = 6 pF typ.
- Photodetectable area : 300 μm dia.



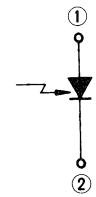
Package Dimensions



(Unit: mm)

CX-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−40 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		5	100	nA	V_R = 5 V
Capacitance	C_t		6		pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		1.0		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		1.0		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

HR1105TG

—Under development—
InGaAs PIN Photodiode

Description

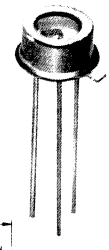
HR1105TG is an InGaAs PIN photodiode for detecting 1.0–1.65 μm light.

Its high speed pulse response makes it suitable as an optical signal detector in high-bit-rate fiber-optic communications equipment.

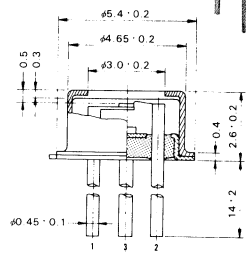
Hermetic sealing of the package achieves high reliability.

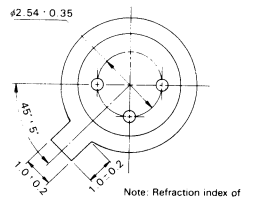
Features

- Fast pulse response : t_r, t_f = 0.5 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 1 nA typ.
- Small capacitance : C_t = 0.8 pF typ.
- Photodetectable area : 80 μm dia.



Package Dimensions





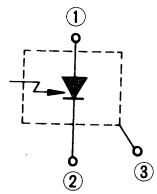
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

Optical and Electrical Characteristics (T_C = 25°C)

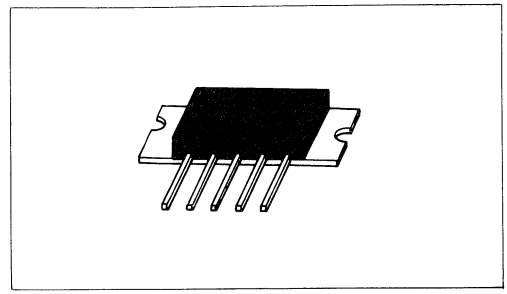
Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		1.0	10	nA	V_R = 5 V
Capacitance	C_t		0.8	1.2	pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

HITACHI

High Frequency Transistors

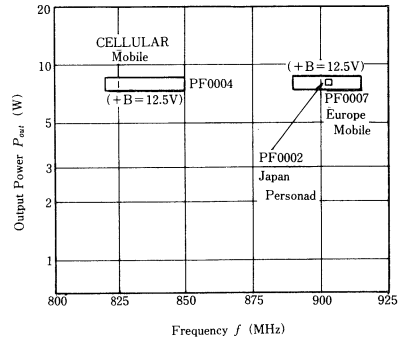
HIGH FREQUENCY POWER MOS FET AMPLIFIER

1. FEATURES AND LINE UP



■FEATURES

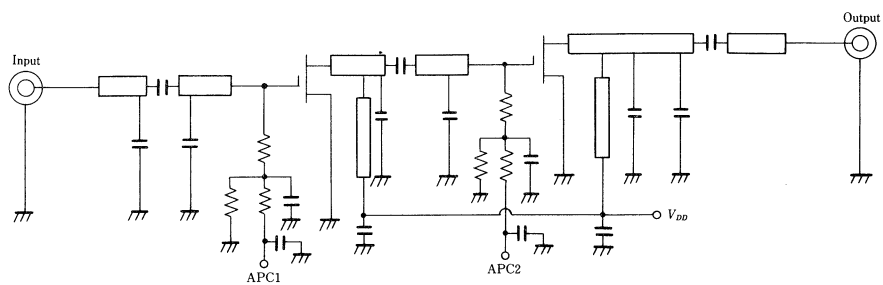
i) Input and output impedance matching circuit built in.
ii) Easy automatic power control (APC) and less control current.
I_{APC} = ±300 μA max. at V_{APC} = ±8V
iii) Wide operating voltage range from 6 to 16V, and capable to cover both portable and mobile units.
iv) Stable at load change.



■LINE UP

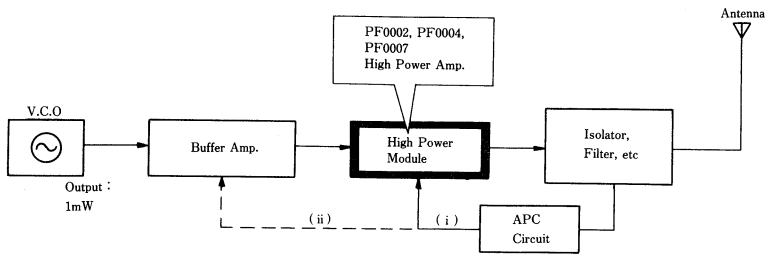
Type No.	Outline	Structure	Features	Remarks
PF0002	PFPAK	Si Power MOS FET MODULE	2 Stage Amplifier for Personal Radios in Japan Pout = 8W Typ. (Pin = 100 mW)	f = 903 to 905 MHz
PF0004	PFPAK	Si Power MOS FET MODULE	2 Stage Amplifier for Cellular mobile radios Pout = 8W Typ. (Pin = 100 mW)	f = 820 to 850 MHz
PF0007	PFPAK	Si Power MOS FET MODULE	2 Stage Amplifier for European mobile radios Pout = 8W Typ. (Pin = 100 mW)	f = 890 to 915 MHz

2. INTERNAL EQUIVALENT CIRCUIT



3. APPLICATION EXAMPLE TO TRANSMITTER OF MOBILE RADIO

3.1. BLOCK DIAGRAM OF TRANSMITTER



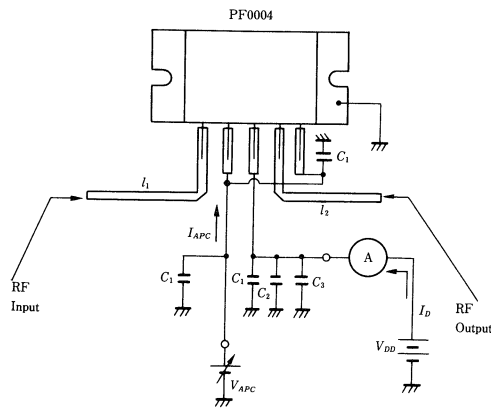
3.2. AUTOMATIC POWER CONTROL (APC)

MOS FET is the voltage controlled device. Therefore, the APC current (I_{APC}) of MOS FET Amp. is required only a few hundred μA, which is one thousandth of Bipolar Transistor Amp. (please refer to Fig. 1 and 2).

To obtain more than 30 dB output power reduction, there are two methodes as follows;

i) To have APC power supply which has both plus and minus polarity. (Please refer to Fig. 3).

ii) If you want to have only plus polarity power supply for APC, the APC should be applied to the buffer amp. as shown in dotted line of block diagrams in item 3-1. This means that output power of the amplifier can be zero watt as the input power of the amplifier becomes lower (in other words, making the output power of the buffer stage lower) as shown in Fig. 4.



■APC Current vs. Output Power

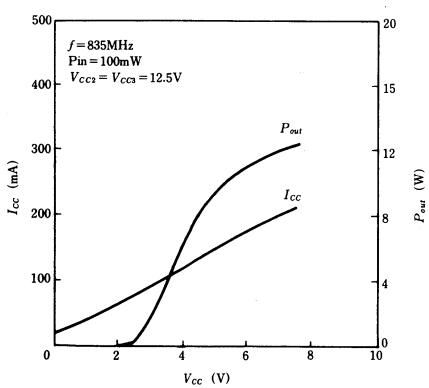


Fig. 1. Bipolar Transistor Amplifier

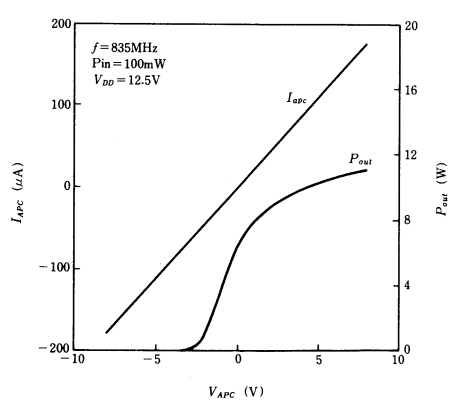


Fig. 2. Power MOS FET Amplifier

■APC Characteristics of Power MOS FET Amplifier

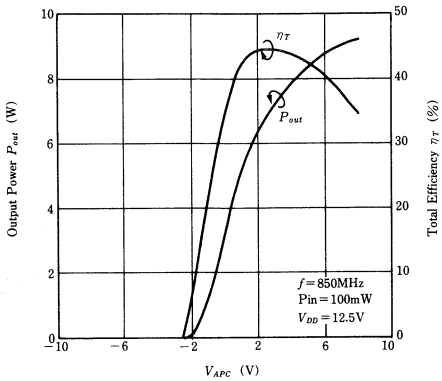


Fig. 3. In the case of plus and minus power supply (fixed input power of 100 mW)

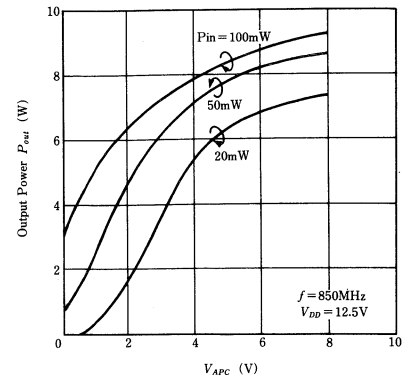


Fig. 4. In the case of only plus power supply (variable input power)

3.3. TEMPERATURE CHARACTERISTICS

Drain current and output power of MOS FET becomes lower as the ambient temperature becomes higher due to the negative temperature coefficient. Therefore, it has wide margin against local current concentration and thermal runaway.

Fig. 5 shows characteristics of output power vs. case temperature. The output power of PF0004 has approximately from –0.23 to –0.26 %/°C.

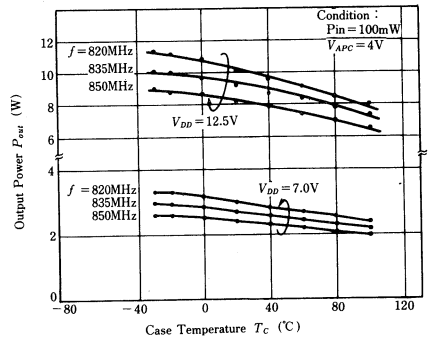
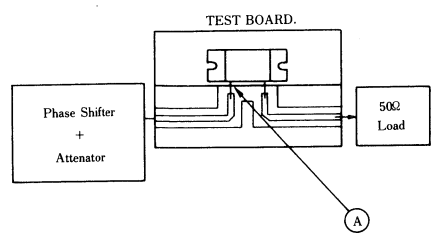


Fig. 5. Output power vs. case temperature (PF0004)

3.4. PARASTIC OSCILLATION

The signal source impedance connected to input and output terminal of the amplifier is usually 50 ohms. However, these impedances vary depending upon the connected condition to buffer amplifier and output circuit condition. Especially, the connected condition to the buffer amplifier causes possibility of oscillation. Therefore, the condition in the actual units should be confirmed well.

As an example, area of oscillation and its oscillation spectrum of PF0004 are shown in Fig. 6. In this case, the wire connection is shown in the right figure, and the input terminal condition of the amplifier is varied by phase shifter and attenuator. The oscillation can be prevented if the impedance looking from point A to the buffer amplifier is located within the shadowed area of Fig. 7.



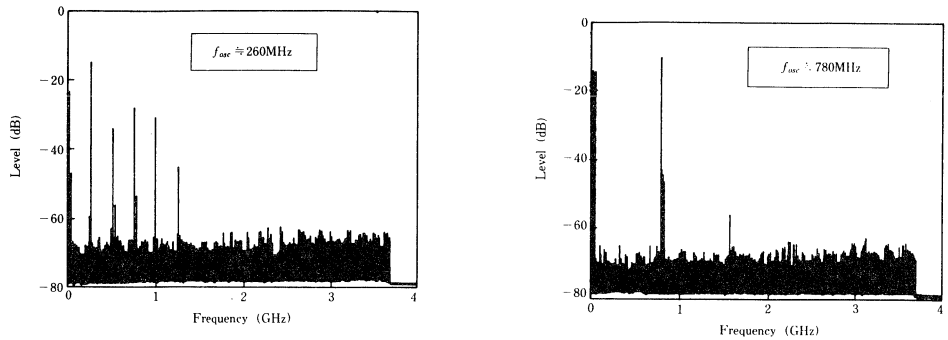


Fig. 6. Example of oscillation spectrum at varying signal source impedance

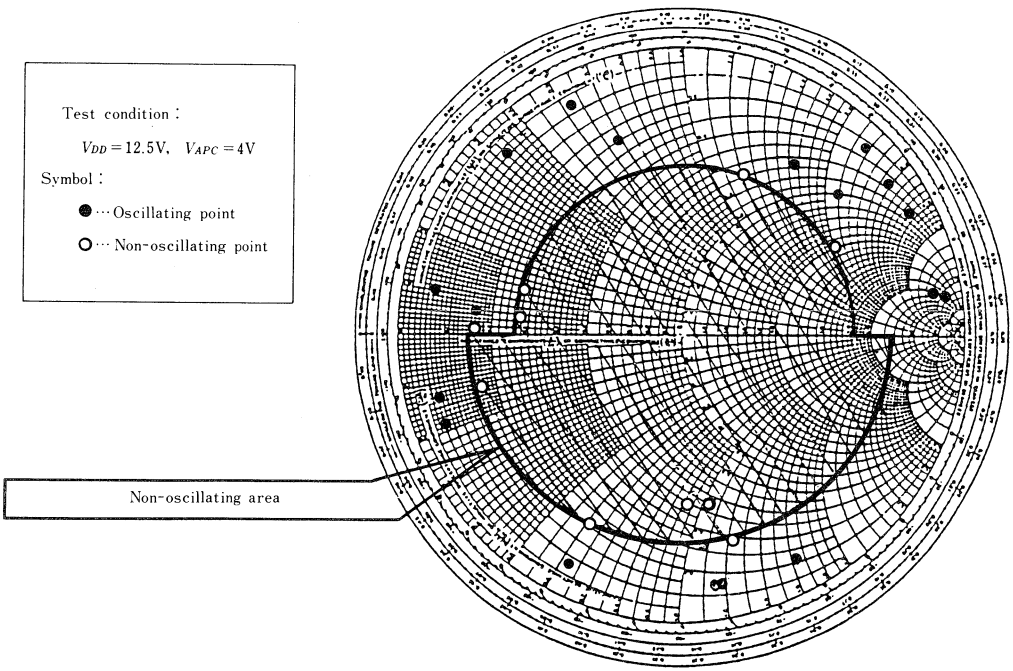


Fig. 7. Non-oscillating area of input signal source impedance

3.5. Others:

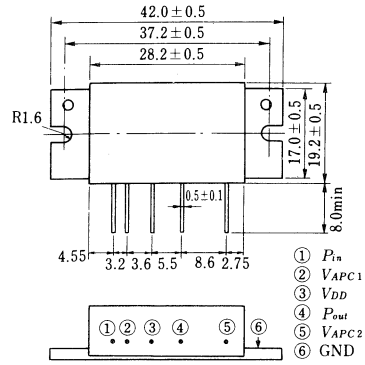
About the reliability and the precautions of handling and mounting, please refer the Hitachi transistor data book, Hitachi high frequency transistor application note and Hitachi semiconductor device reliability note.

POWER MOS FET AMPLIFIER

UHF POWER AMPLIFIER

■ FEATURES

- 50Ω Input/Output impedance.
- Simple Automatic power control.
- Superior stability.
- Withstand infinite VSWR.



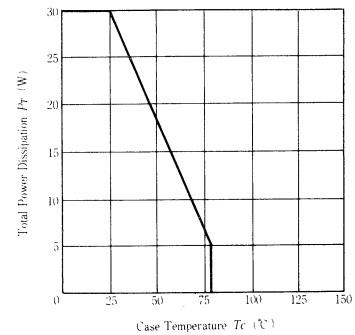
(Unit: mm)

■ ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Item	Symbol	Rating	Unit
DC Supply Voltage	V_{DD}	17	V
Circuit Current	I_{DD}	3.0	A
Power Control Voltage	V_{APC}	±8	V
Total Power Voltage	P_T*	30	W
Operating Case Temperature	$T_{C(op)}$	−30 ~ +80	°C
Storage Temperature	T_{stg}	−40 ~ +100	°C
Maximum Input Power	P_{IN}	250	mW

*Value at T_c=25 °C

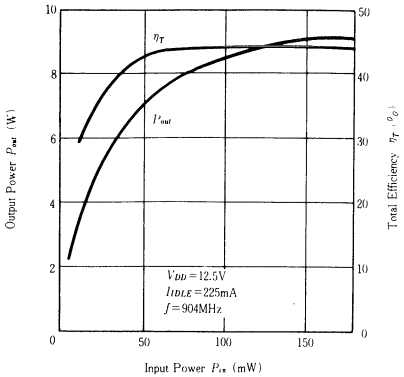
POWER VS. TEMPERATURE DERATING



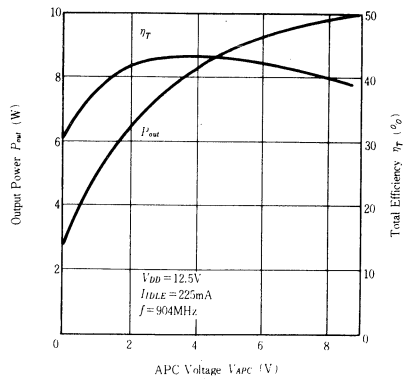
■ ELECTRICAL CHARACTERISTICS (T_a=25 °C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	V_{DD}=15V, V_{APC}=0 Z_{IN}=Z_{OUT}=50Ω	—	—	500	μA
Leakage Current	I_{APC}	V_{APC}=±8V, V_{DD}=0	±100	—	±300	μA
Output Power	P_{OUT}	V_{DD}=12.5V, I_{IDLE}=225mA,	7.0	8.0	—	W
Total Efficiency	η_T	f=903~905MHz,	35	40	—	%
2nd Harmonic Distortion	*2nd H.D.*	P_{IN}=100mW,	—	—	−30	dB
3rd Harmonic Distortion	*3rd H.D.*	Z_{IN}=Z_{OUT}=50Ω	—	—	−30	dB
Input VSWR	$VSWR_{(IN)}$	V_{DD}=12.5V, I_{IDLE}=225mA,	—	1.5	2.5	—
Output VSWR	$VSWR_{(OUT)}$	Z_{IN}=Z_{OUT}=50Ω, f=903~905MHz, P_{IN}=100mV	—	2	—	—

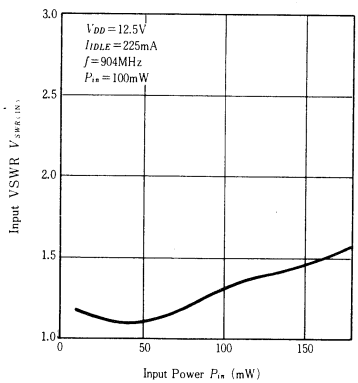
OUTPUT POWER & TOTAL EFFICIENCY VS. INPUT POWER



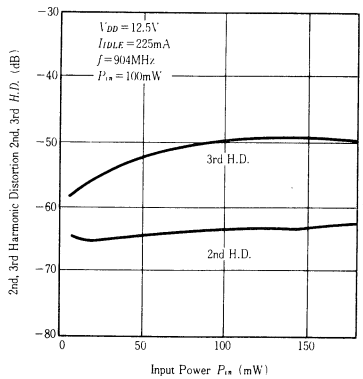
OUTPUT POWER & TOTAL EFFICIENCY VS. APC VOLTAGE



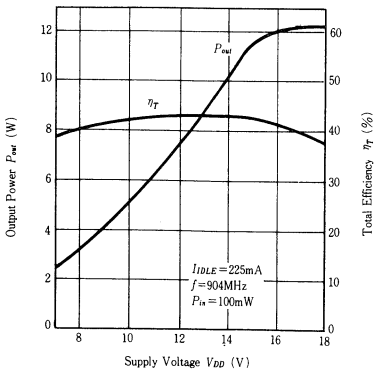
INPUT VSWR VS. INPUT POWER



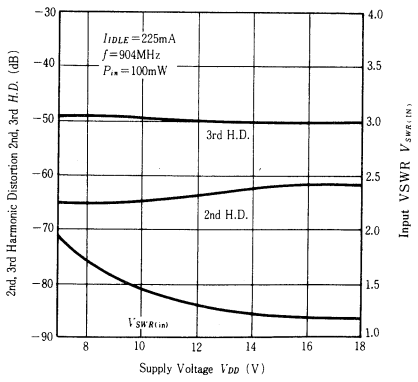
2nd, 3rd HARMONIC DISTORTION VS. INPUT POWER



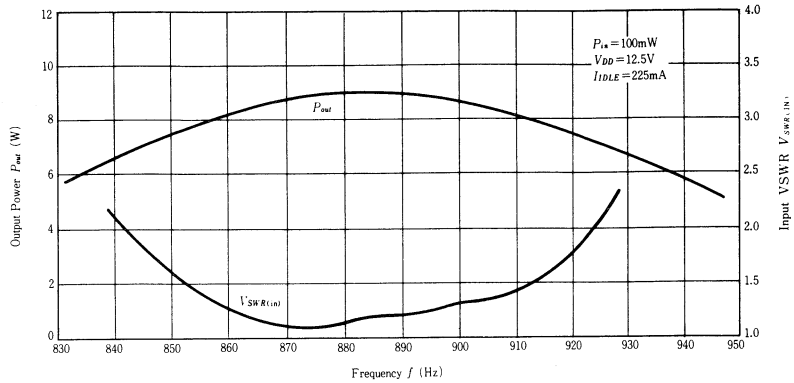
OUTPUT POWER & TOTAL EFFICIENCY VS. SUPPLY VOLTAGE



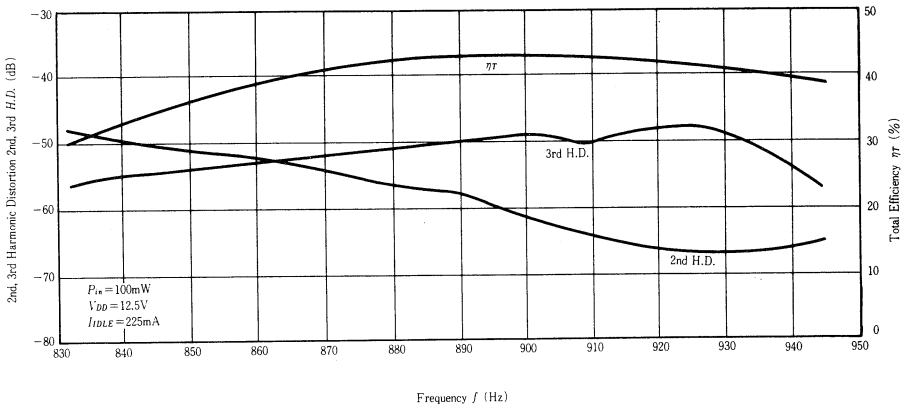
2nd, 3rd HARMONIC DISTORTION AND INPUT VSWR VS. SUPPLY POWER



OUTPUT POWER AND INPUT VSWR VS. FREQUENCY

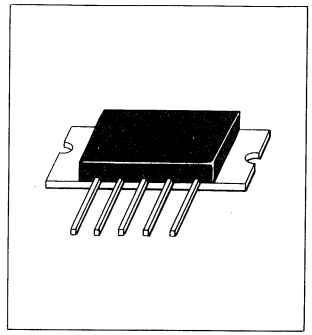


2nd, 3rd HARMONIC DISTORTION VS. TOTAL EFFICIENCY VS. FREQUENCY



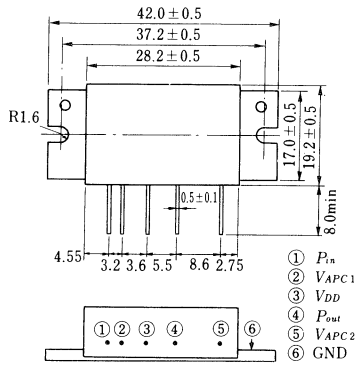
PF0004 — Preliminary

MOS FET POWER AMPLIFIER
UHF POWER AMPLIFIER



■FEATURES

- Included input and output matching circuit.
- Easy to control output power and less A.P.C control current.
  I_{APC} = ±300 μA at V_{APC} = ±8V
- Wide operation voltage.
  V_{DD} = 6 to 16V
- Superior to stability at load mismatching.



(Unit: mm)

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

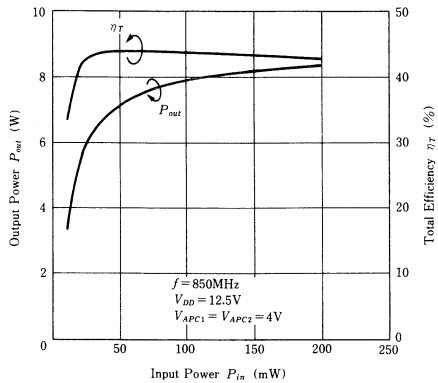
Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	17	V
Maximum Circuit Current	I_D	3.0	A
APC Voltage	V_{APC}	±8	V
Maximum Input Power	*Pin*	200	mW
Operating Maximum Case Temperature	$T_{C(op)}$	–40 to +100	°C
Storage Temperature	*Tstg*	–45 to +125	°C

■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

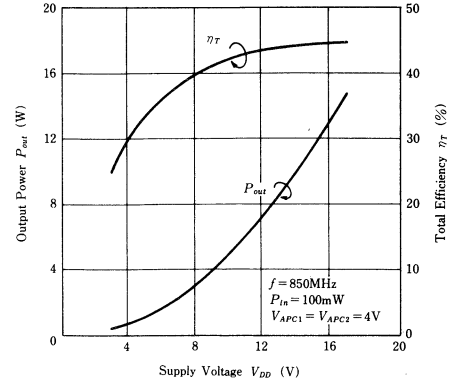
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	V_{DD} = 17V, V_{APC1} = V_{APC2} = 0	–	–	500	μA
Output Power	*Pout(1)*	*f* = 820 to 850 MHz, *Pin* = 100 mW, V_{DD} = 12.5V, V_{APC1} = V_{APC2} = 4V, *Zin* = *Zout* = 50Ω	7.0	8.0	–	W
Total Efficiency	$\eta_T(1)$		35	40	–	%
2nd Harmonic Distortion	*2nd H.D.*		–30	–50	–	dB
3rd Harmonic Distortion	*3rd H.D.*		–30	–50	–	dB
Input VSWR	*VSWR(in)*		–	1.5	3.0	–
Output VSWR	*VSWR(out)*		–	1.5	–	–
Output Power	*Pout(2)*	*f* = 820 to 850 MHz, *Pin* = 100 mW, V_{DD} = 7.2V, V_{APC1} = V_{APC2} = 4V, *Zin* = *Zout* = 50Ω	1.8	–	–	W
Total Efficiency	$\eta_T(2)$		30	–	–	%

HITACHI

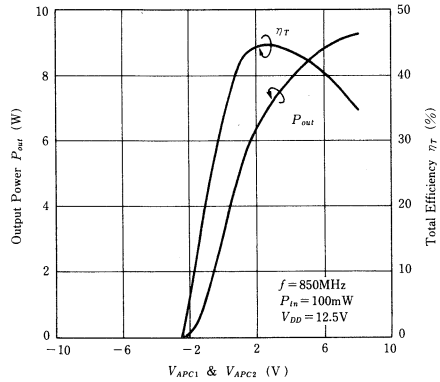
Pout, η_T, vs. Input Power



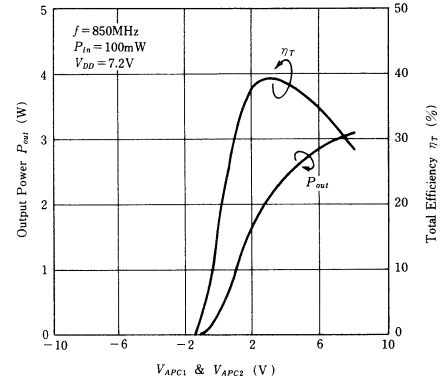
Pout, η_T vs. Supply Voltage



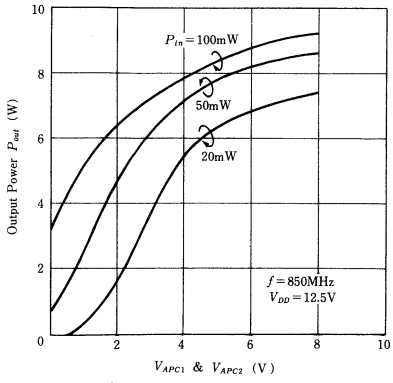
Pout, η_T vs. V_{APC} (1)



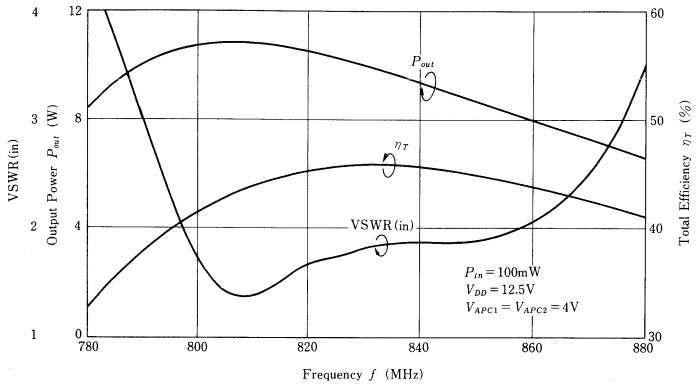
Pout, η_T vs. V_{APC} (2)



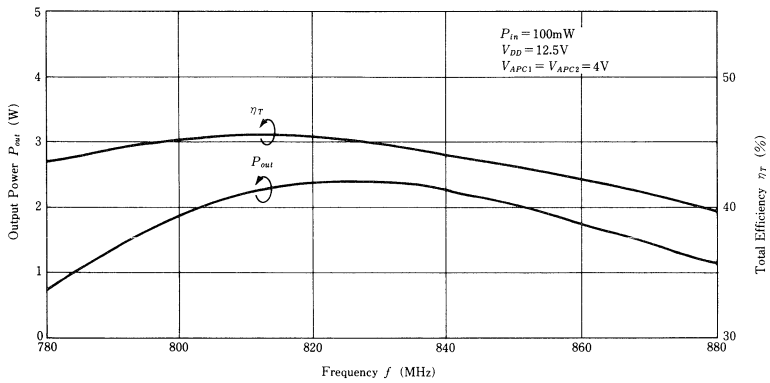
Pout vs V_{APC}



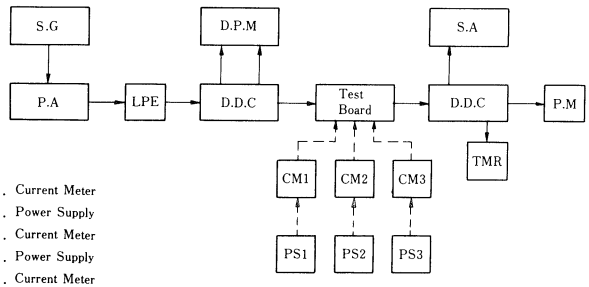
Pout, η_T, VSWR(in) vs. Frequency



Pout, η_T, vs. Frequency



■MEASUREMENT BLOCK DIAGRAM

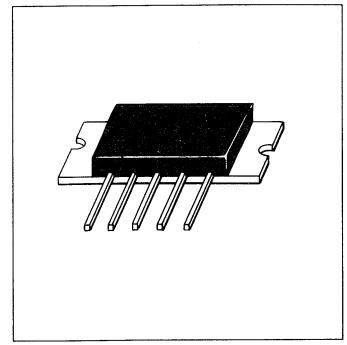


CM1 . . . Current Meter
PS1 . . . Power Supply
CM2 . . . Current Meter
PS2 . . . Power Supply
CM3 . . . Current Meter
PS3 . . . Power Supply

S.G . . . Signal Generator
P.A . . . Power Amplifier
DDC . . . Dual Directional Coupler
DPM . . . Dual Channel Power Meter
S.A . . . Spectrum Analyzer
P.M . . . Power Meter
TMR . . . Terminator (50Ω)

PF0007 — Preliminary

MDS FET POWER AMPLIFIER
UHF POWER AMPLIFIER

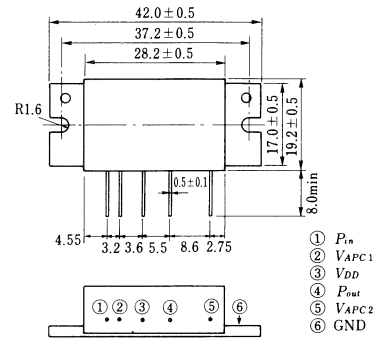


■FEATURES

- Included input and output matching circuit.
- Easy to control output power and less A.P.C control current.
  I_{APC} = ±300 μA at V_{APC} = ±8V
- Wide operation voltage.
  V_{DD} = 6 to 16V
- Superior to stability at load mismatching.

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	17	V
Maximum Circuit Current	I_D	3.0	A
APC Voltage	V_{APC}	±8	V
Maximum Input Power	Pin	200	mW
Operating Maximum Case Temperature	$TC_{(op)}$	−40 to +100	°C
Storage Temperature	$Tstg$	−45 to +125	°C

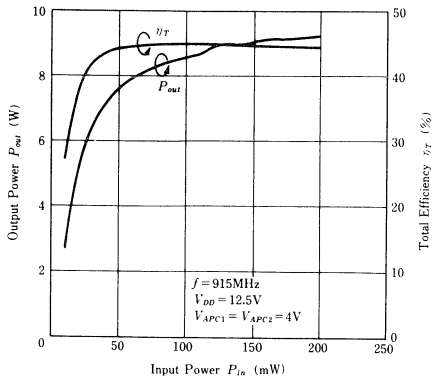


(Unit: mm)

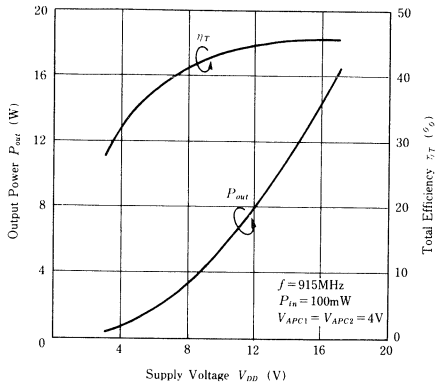
■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	V_{DD} = 17V, V_{APC1} = V_{APC2} = 0	–	–	500	μA
Output Power	$Pout(1)$	f = 890 to 915 MHz Pin = 100 mW, V_{DD} = 12.5V, V_{APC1} = V_{APC2} = 4V, Zin = $Zout$ = 50Ω	7.0	8.0	–	W
Total Efficiency	$\eta T(1)$		35	40	–	%
2nd Harmonic Distortion	$2nd\ H.D.$		−30	−50	–	dB
3rd Harmonic Distortion	$3rd\ H.D.$		−30	−50	–	dB
Input VSWR	$VSWR(in)$		–	1.5	3.0	–
Output VSWR	$VSWR(out)$		–	1.5	–	–
Output Power	$Pout(2)$	f = 890 to 915 MHz, Pin = 100 mW, V_{DD} = 7.2V, V_{APC1} = $V_{APC\,2}$ = 4V, Zin = $Zout$ = 50Ω	1.8	–	–	W
Total Efficiency	$\eta T(2)$		30	–	–	%

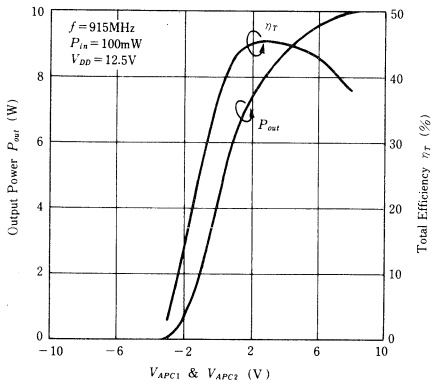
Pout, η_T, vs. Input Power



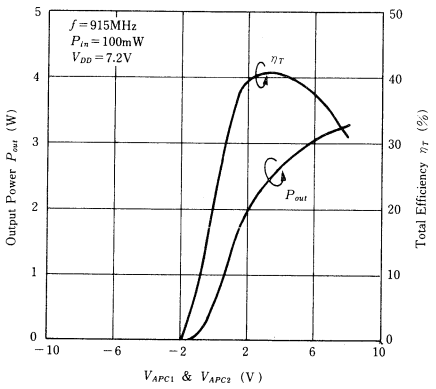
Pout, η_T vs. Supply Voltage



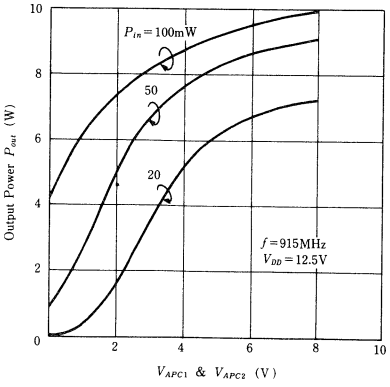
Pout, η_T vs. V_{APC} (1)



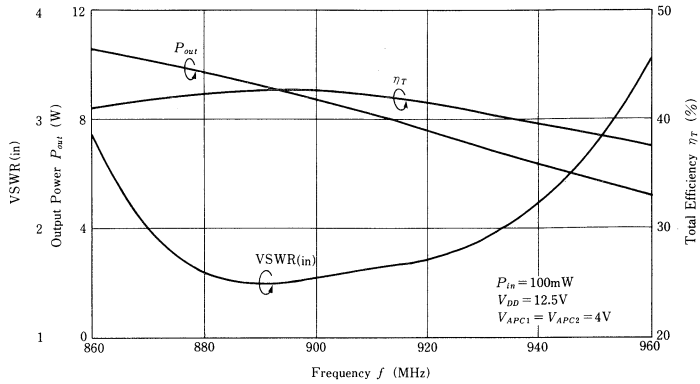
Pout, η_T vs. V_{APC} (2)



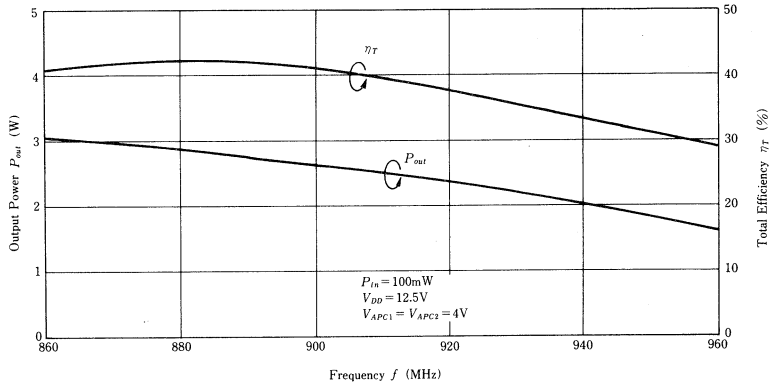
Pout vs. V_{APC}



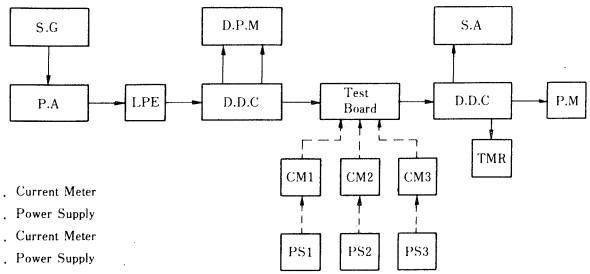
Pout, η_T, VSWR(in) vs. Frequency



Pout, η_T, vs. Frequency



■MEASUREMENT BLOCK DIAGRAM



CM1 . . . Current Meter
PS1 . . . Power Supply
CM2 . . . Current Meter
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CM3 . . . Current Meter
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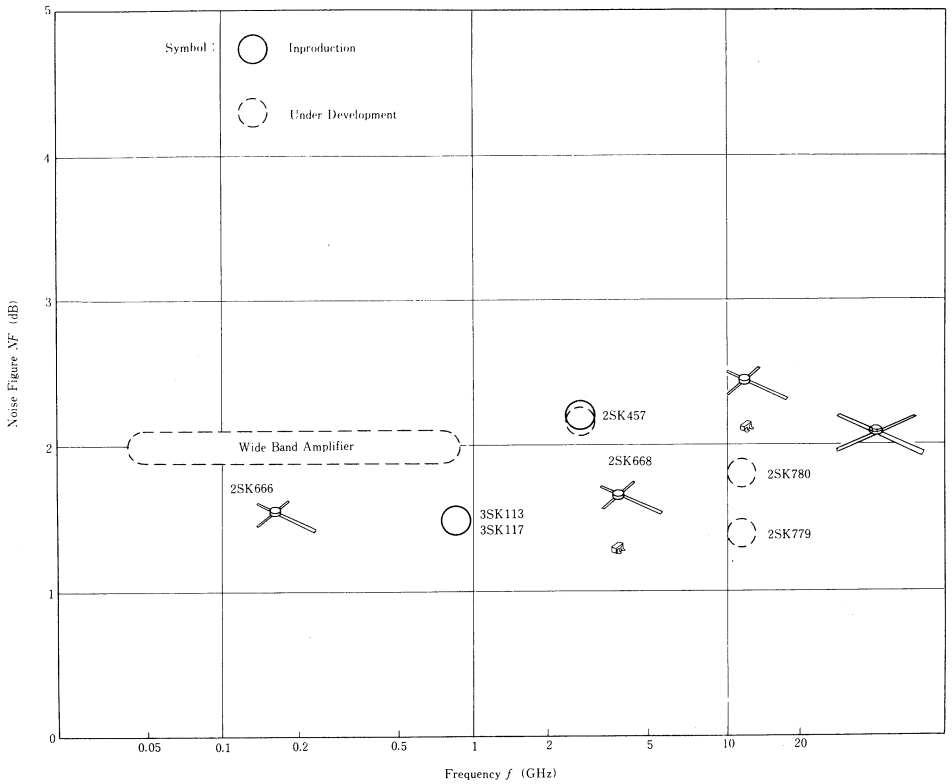
S.G . . . Signal Generator
P.A . . . Power Amplifier
DDC . . . Dual Directional Coupler
DPM . . . Dual Channel Power Meter
S.A . . . Spectrum Analyzer
P.M . . . Power Meter
TMR . . . Terminator (50Ω)

ULTRA HIGH FREQUENCY GaAsFET

LINE UP



FEATURES

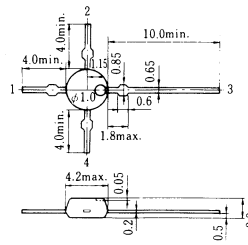
- Low Noise . . . . . NF = 1.8 dB at f = 12 GHz (HS6601)
- Wide Variation of Devices . . . . UHF Band (4 types)
  SHF Band (4 types)

2SK457 — Preliminary

GaAs N-channel MES FET
SHF CONVERTER RF AMPLIFIER

■FEATURES

- Low Noise, High Gain.
  NF = 2.1 dB typ., PG = 10 dB typ. (f = 3 GHz)



1. Source
2. Drain
3. Source
4. Gate

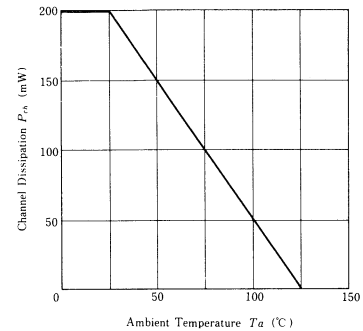
(Unit : mm)

(FPAK)

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	5	V
Gate to Source Voltage	V_{GS}	+0.5 −6.0	V
Drain Current	I_D	100	mA
Channel Dissipation	Pch	200	mW
Channel Temperature	Tch	125	°C
Storage Temperature	$Tstg$	−55 to +125	°C

MAXIMUM CHANNEL DISSIPATION CURVE

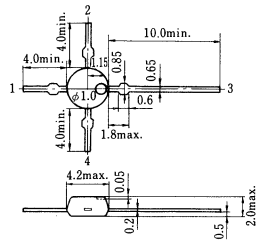


■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Leakage Current	I_{DSX}	V_{DS} = 6V, V_{GS} = −4V	–	–	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = −6V, V_{DS} = 0	–	–	10	μA
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0	20	–	100	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 5V, I_D = 100 μA	–	–	−5	V
Forward Transfer Admittance	$\|yfs\|$	V_{DS} = 5V, I_D = 20 mA, f = 1 kHz	15	35	–	mS
Minimum Noise Figure	NF	V_{DS} = 4V, I_D = 20 mA, f = 3 GHz	–	10	–	dB
Associated Gain	Ga	V_{DS} = 4V, I_D = 20 mA, f = 3 GHz	–	2.1	–	dB

2SK666 — Preliminary

Single Gate GaAs FET
Wide Band Amplifier



1. Gate
2. Source
3. Drain
4. Source

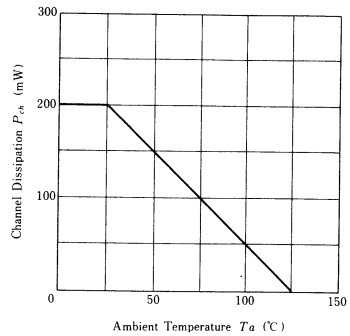
(Unit : mm)

(FPAK)

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	4	V
Gate to Source Voltage	V_{GS}	−3	V
Drain Current	I_D	150	mA
Channel Dissipation	Pch	200	mW
Channel Temperature	Tch	125	°C
Storage Temperature	$Tstg$	−55 to +125	°C

MAXIMUM CHANNEL DISSIPATION CURVE



■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Cutoff Current	I_{DSX}	V_{DS} = 4V, V_{GS} = −1V	–	–	200	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = −3V, V_{DS} = 0	–	–	100	μA
Drain Current	I_{DSS}	V_{DS} = 3V, V_{GS} = 0	20	–	150	mA
Forward Transfer Admittance	$\|yfs\|$	V_{DS} = 3V, I_D = 20 mA, f = 1 kHz	50	100	–	mS
Power Gain	PG	V_{DS} = 3V, I_D = 20 mA f = 50, 900 MHz	6	8	–	dB
Noise Figure	NF		–	2.5	3.5	dB

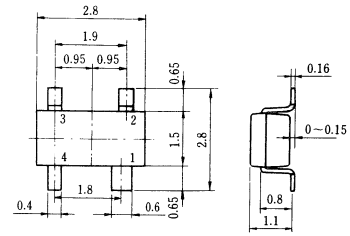
HITACHI

2SK668 — Preliminary

N-Channel GaAs Single Gate MES FET
UHF/SHF Low Noise Amplifier

■FEATURES

- Low Noise, High Gain.
  NF = 2.1 dB typ., PG = 10 dB typ. (f = 3 GHz)



1. Source
2. Drain
3. Source
4. Gate

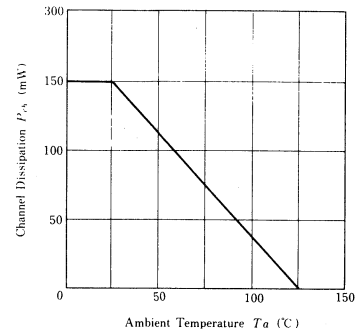
(Dimensions in mm)

(MPAK-4)

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	6	V
Gate to Source Voltage	V_{GS}	+0.5 −6.0	V
Drain Current	I_D	100	mA
Channel Dissipation	Pch	150	mW
Channel Temperature	Tch	125	°C
Storage Temperature	$Tstg$	−55 to +125	°C

MAXIMUM CHANNEL DISSIPATION CURVE



■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

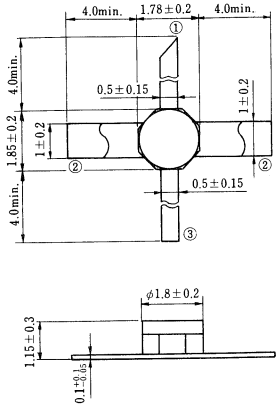
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DSX}	V_{DS} = 6V, V_{GS} = −4V	–	–	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = −6V, V_{DS} = 0	–	–	10	μA
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0	20	–	100	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 5V, I_D = 100 μA	–	–	−5	V
Forward Transfer Admittance	$\|yfs\|$	V_{DS} = 5V, I_D = 20 mA, f = 1 kHz	15	35	–	mS
Power Gain	PG	V_{DS} = 4V, I_D = 20 mA, f = 3 GHz	–	10	–	dB
Noise Figure	NF	V_{DS} = 4V, I_D = 20 mA, f = 3 GHz	–	2.1	–	dB

2SK779 — Under Development

GaAs N-channel MES FET
SHF Converter RF Amplifier

■FEATURES

- Excellent Low Noise Characteristics.
  NF = 1.4 dB (typ.) at f = 12 GHz
- High Associate Gain.
  Ga = 11 dB (typ.) at f = 12 GHz

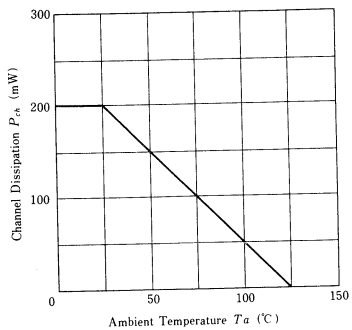


1. Gate
2. Source
3. Drain
(Unit : mm)

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	5	V
Gate to Source Voltage	V_{GS}	−6	V
Drain Current	I_D	120	mA
Channel Dissipation	Pch	200	mW
Channel Temperature	Tch	125	°C
Storage Temperature	$Tstg$	−55 ~ +125	°C

MAXIMUM CHANNEL DISSIPATION CURVE



■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Gate to Source Leakage Current	I_{GSS}	V_{GS} = −3V, V_{DS} = 0	–	–	−10	μA
Drain Current	I_{DSS}	V_{DS} = 3V, V_{GS} = 0	20	–	120	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 3V, I_D = 100 μA	−0.5	–	−3.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 3V, I_D = 10 mA, f = 1 kHz	30	50	–	mS
Minimum Noise Figure	NF	V_{DS} = 3V, I_D = 10 mA f = 12 GHz, (at NF MIN)	–	1.4	–	dB
Associated Gain	Ga		–	11	–	dB

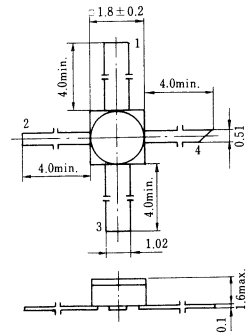
HITACHI

2SK780 — Under Development

GaAs N-channel MES FET
SHF Converter RF Amplifier

■FEATURES

- Excellent Low Noise Characteristics.
  NF = 1.8 dB (typ.) at f = 12 GHz
- High Associate Gain.
  Ga = 10 dB (typ.) at f = 12 GHz



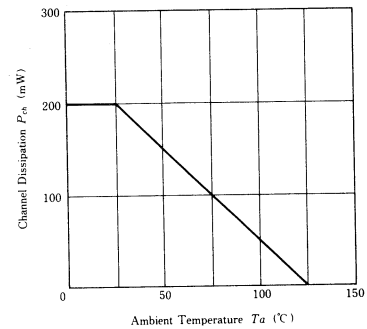
1. Source
2. Drain
3. Source
4. Gate

(Unit : mm)

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	5	V
Gate to Source Voltage	V_{GS}	−6	V
Drain Current	I_D	120	mA
Channel Dissipation	*Pch*	200	mW
Channel Temperature	*Tch*	125	°C
Storage Temperature	*Tstg*	−55 ~ +125	°C

MAXIMUM CHANNEL DISSIPATION CURVE



■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Gate to Source Leakage Current	I_{GSS}	V_{GS} = −3V, V_{DS} = 0	–	–	−10	μA
Drain Current	I_{DSS}	V_{DS} = 3V, V_{GS} = 0	20	–	120	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 3V, I_D = 100 μA	−0.5	–	−3.5	V
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	V_{DS} = 3V, I_D = 10 mA, f = 1 kHz	20	40	–	mS
Minimum Noise Figure	*NF*	V_{DS} = 3V, I_D = 10 mA f = 12 GHz, (at NF MIN)	–	1.8	–	dB
Associated Gain	*Ga*		–	10	–	dB

HIGH FREQUENCY TRANSISTORS FOR WIDE BANDWIDTH AMPLIFIER

■LINE UP

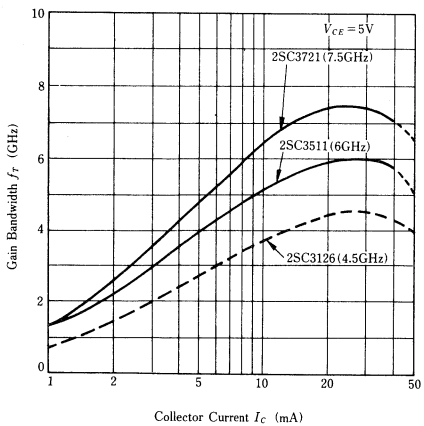
Table 1. High Frequency Transistors for Wide Bandwidth Amplifier

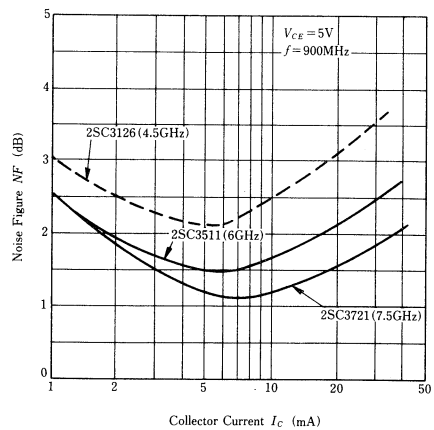
Item / f_T(GHz)	Package Outline				Main Characteristics (typ. value)			
	FPAK	MPAK	TO-92	UPAK	Cob(pF)*1	f_T(GHz)	PG(dB)*2	NF(dB)*2
								
4.4	–	–	2SC3337	–	1.5	4.4	8.6	2.9
4.5	2SC3126	2SC3127	2SC3128 2SC3510	2SC3338	0.9	4.5	10.5	2.2
6.0	2SC3511	2SC3513	2SC3512	–	1.0	6.0	11.0	1.5
7.5	2SC3721	2SC3730	–	–	0.9	7.5	12.5	1.2

*1: f = 1 MHz, *2: f = 900 MHz

■TYPICAL CHARACTERISTICS

- f_T, NF





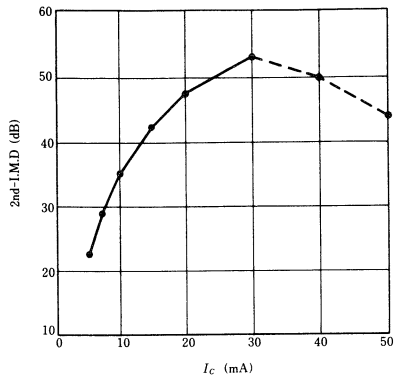
Intermediate Modulation Distortion

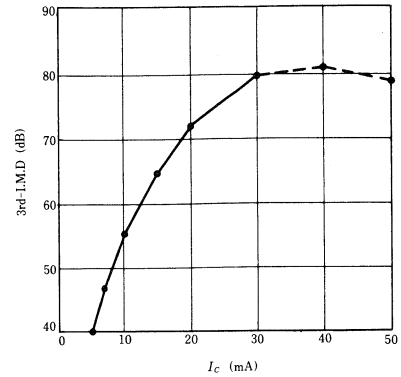
(Unit: dB)

Type No.	Freq.	f_1 = 200 MHz f_2 = 210 MHz		f_1 = 500 MHz, f_2 = 510 MHz		Bias Condition
		410 MHz (2nd I.M.D)	220 MHz (3rd I.M.D)	1010 MHz (2nd I.M.D)	520 MHz (3rd I.M.D)	
2SC3126	FPAK	47.9	79.2	43.6	75.6	V_{CC} = 6V I_C = 30 mA
2SC3511		51.2	79.9	44.7	77.7	
2SC3721		53.2	79.8	47.0	76.6	
2SC3337	TO-92	42.8	70.0	–	–	V_{CC} = 24V I_C = 20 mA
2SC3510		45.7	77.8	–	–	
2SC3512		45.6	79.4	–	–	

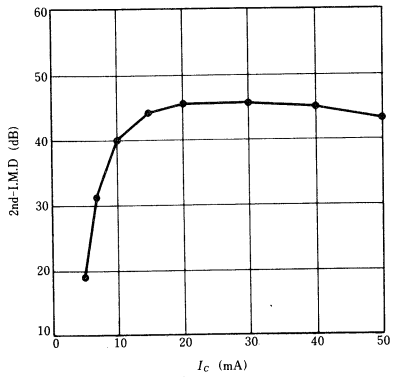
- **IMD vs. IC**

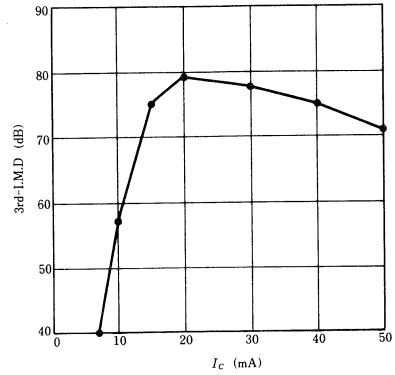
2SC3721





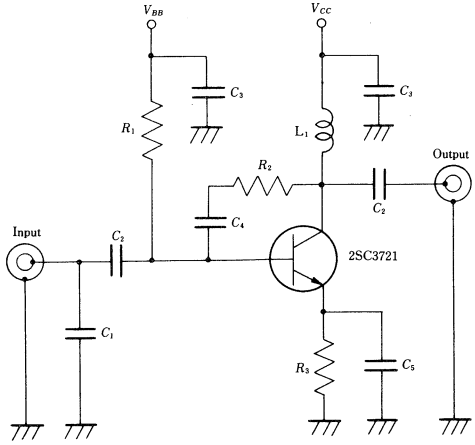
2SC3512



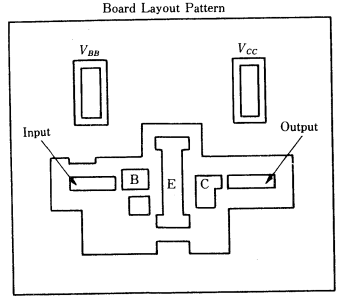


■CIRCUIT EXAMPLE (2SC3721 1-stage Amplifier)

- Equivalent Circuit

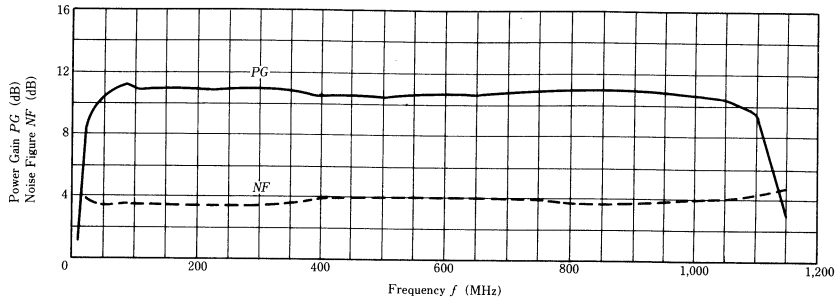


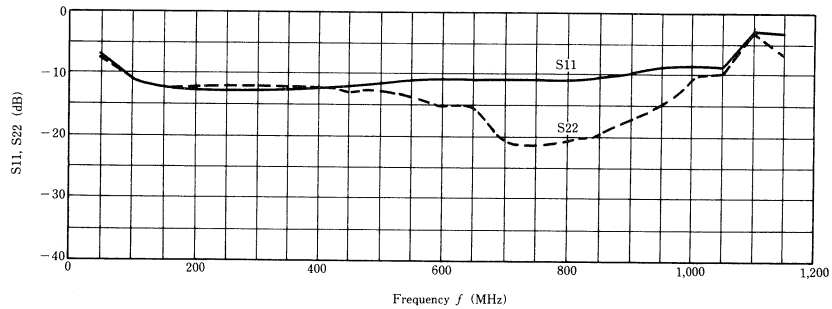
Board Layout Pattern



C_1 : 2pF C_2 : 470pF C_3 : 4,700pF
C_4 : 47pF C_5 : 10pF
R_1 : 30kΩ R_2 : 300Ω R_3 : 11Ω
L_1 : φ0.5mm Cu wire, I.D φ3mm, 14Turn

- Frequency Characteristics





- IMD Characteristics

I.M.D Characteristics (Vcc = 6V, Icc = 24mA, Pin = −10dBm)

Freq. 1 (MHz)	Freq. 2 (MHz)	2nd I.M.D (dB)	3rd I.M.D (dB)	3rd I.M.D (dB)
200	210	53.7 (410 MHz)	72.3 (190 MHz)	73.9 (200 MHz)
500	510	54.4 (1010 MHz)	75.9 (490 MHz)	76.8 (520 MHz)
900	910	50.4 (1810 MHz)	74.2 (890 MHz)	74.8 (920 MHz)

Telecommunications Glossary

■TELECOMMUNICATIONS GLOSSARY

Term	Explanation
A/D (Analog to Digital) Converter	A device which converts analog wave to digital suitable form for digital processing and switching.
ADI (Alternate Digit Inversion)	Used with A law to ensure sufficient 1 → 0/0 → 1 transitions for clock extraction.
A law	Companding/encoding law mainly used in Europe.
Aliasing Noise	A distortion which occurrs if the sampled signal's bandwidth is greater than half the sample rate.
AMI signal (Alternate Mark Inversion)	A pseudo-fernary signal in which successive marks are normally of alternate, + and – polarity but equal in amplitude and in which space is of zero amplitude.
Anti Aliasing Filter	A filter whose input signal bandwidth is limited before sampling to less than half the sampling rate. This is to eliminate Aliasing Noise.
Asynchronous	State in which receive or transmit signal timings occur in the network with the same frequency and phase.
Base-band transmission type	Transmission type which transmits the original forms of signals.
Baud Rate	Unit of modulating speed. One baud shows speed to modulate one element per second. This is not always same as transferred rate bit per second.
BCP (Byte Control Protocol)	A protocol in which sets of byte-wide data control the data link. One of the COP protocols.
Bit Stealing	Signalling in which least significant bit of time slots used for encoded speech are periodically used for switching information.
Blancing Network	A circuit connected bridges or Hybrids which compensate the impedance unmuching to restrain echo.
BOP (Bit Oriented Protocol)	A protocol in which sets of bits control the data link.
Carrier (Signal)	A signal suitable by modulation for an information signal.
CCITT (Comite Consultatif International Telegraphique et Telephonique)	International Telegraph and Telephone Consultative Committee, part of the Internation Telecommunication standard organization.
Channel Bank	PCM multiplexer/demultiplexer equipment. (called usually in North America)
24 Channel Mux	Early PCM multiplex equipment, 7 digit A law, 1 signalling bit with each time slot, transmission rate 1536k bps.
30 Channel Mux	CCITT recommended form PCM multipley equipment. A law, 30 speech channels + 2 signalling channels, transmission rate 2048k bps.
C-message	A frequency weighting which evaluates the noise corresponding to typical subscriber's annoyance in standard telephone service.
C-notched	In C-message, the evaluation for the addition of a notch at 1010 to 1040 Hz.
CODEC	A device which converts an analog (300 Hz to 3.4 kHz) to a digital one, or vice versa.
Companding Law	A logarithmic type of conversion used in compression and expansion.
Compression	Characteristic conversion in which the digitized information is compressed to give digital output for a signals normal dynamic range.
COP (Character Orientel Protocol)	A Protocol in which sets of characters control the data link.

(to be continued)

Term	Explanation
Crosstalk	Interference between transmission paths, caused by a signal traveling to another path.
D/A (Digital to Analog) Converter	A device which converts digital form to analog wave.
Dial pulses	Sequence of pulses as created on a rotary dial telephone set. (cf. DTMF)
DPSK (Differential Phase Shift Keying)	Modulation technique for the transmission of digital information. Carrier is phase modulated to represent different information states.
Drop out	State in which some pulses become undetectable in successive pulses transmitted.
DTMF (Dual Tone Multi Frequency)	Diallling signal in telephony System. It consists of High and Low frequency.
Echo	The phenomena caused by reflected signals in the other direction.
Equalizer	A device in which attenuation varies with frequency and is used for a frequency-dependent transmission line.
Expansion	Back to an original signal from compressed.
FDM (Frequency Division Multiplex)	To obtain several channels over a single path by sharing the frequency band. (cf. TDM)
Frame	A segment of a signal, it is a sequence of time slots each containing a sample in case of TDM.
FSK (Frequency Shift Keying)	A kind of modulation. (cf. DPSK)
Full duplex	Transmission type in both directions simultaneously.
Frequency Specification	A display of a signals constituent frequency components given in terms of frequency versus signal amplitude.
Gain Tracking	Loss deviation (1000 Hz reference commonly) over the range of levels.
Half duplex	Transmission type in one direction at a time over a single channel.
HDLC (High Level Data Link Control)	ISO version of a bit-oriented data link control.
(PCM) Highway	A common path or a set of parallel paths over which signals pass with separation performed time division.
Hookswitch	A switch which detects the state that a handset on telephone whether it operates or not.
Idle Channel Noise	The total signal energy measured at the output when the input is grounded in a device.
Impulse noise	The noise which are much higher than the normal peaks of the circuit noise.
Interpolation Filter	A low path (commonly) Filter which smoothes analog forms from decoder.
ISDN	Integrated Service Digital Network.
Jitter	Short term variations of pulses from their real position in time.
LAN (Local Area Network)	A data only communication between terminals on a private site using a standard interface.

(to be continued)

Term	Explanation
Linear Quantizing	Quantizing in which all the intervals classified are equal.
Mark	Presence of a signal. Equivalent to a binary 1 signal state.
Master Clock	A clock which operates a system.
Master Frame	A set of some frames defined.
Modem	A device which modulates or demodulates signals.
Non-Linear Quantizing	Quantizing in which the intervals classified are not all equal.
0 TLP (Zero Transmission Level Point)	An arbitrary point to which all relative level at other points in the system are referred
PABX	Private Automatic Branch Exchange.
Packet-Switching	To transport and switch data in packet form.
PCM (Pulse Code Modulation)	A process in which an analog signal is sampled, quantized and converted to a digital signal.
Protocol	A formal set of conventions or rules governing format, timing, and error control to facilitate message exchanges between two communicating processors.
P/S (parallel to serial) Converter	A device which converts a group of digit, all of which are presented simultaneously, into a corresponding seauence of serial.
Psophmetric-weighted	A frequency weight which is similar to C-message. (Used commonly for European telephony system standard).
Quantizing	To be classified an instant swing value got by sampling.
Sampling	To get instant swing values of (continuous) analog wave at equal time intervals.
Sampling rate	The number of samples per unit time.
SDLC (Synchronous Data Link Control)	IBM computer networking protocol associated with BOP.
S & H (Sample and Hold)	To sample (see sampling) and to hold each instant swing values as a pulse of constant time width.
Signalling	The transmission of switching information between stations.
SLIC (Subscriber Line Interface Circuit)	The circuit which performs the interface between local loop and digital switching System.
Space	Absence of a signal. Equvalent to a binary 0 signal state.
Space Division switch	Multiport switch in which ports are interconnected by use of different physical paths.
S/P (Serial to Parallel) converter	A device which converts a sequence of signal into a corresponding group of digits (i.e. parallel data).
Speech Network	Speech Circuit which divides a single transmission channel into double.
STS switch (Space-Time-Space)	Large switch consisting of a time switch block between two space switch blocks.

Term	Explanation
Synchronization	State in which receive or transmit signal timings occur in the network with the same frequency and phase.
T1 Carrier System	PCM multiplex equipment using μ law, 24 channels. Signalling being performed by bit stealing.
T.D.M. (Time Division Multiplex)	Several information channels are time shared over a single channel and allocated each information by an assigned time slot.
Teletex	Intelligent text communication service which will gradually replace telex.
Teletext	Broad casting service of text on Television reception.
Telex	A message service enabling its subscribers to dial.
Time Division Mux Switch	Multiport switch in which all ports have same physical path because of TDM.
Time Slot	A digital character created by each sampling in PCM.
Tone ringer	A device which converts the ringing signal received from the station into voice frequency as ringing bell.
Trunk	A transmission area between two switching systems.
TST switch (Time Space Time)	Large switch consisting of a space block between two time switch blocks.
White noise	Random noise whose constant energy per unit bandwidth is independent of the frequency at the band.
X.21	A CCITT standard that defines the interface between public data network (DCE) and user terminating equipment (DTE).
X.25	A CCITT standard that defines the interface between a packet-switched public data network and packet-mode user device.
X.75	A CCITT standard between international communication. Using X.25.
μ law	Companding/encoding law used in North America and Japan.

■UNIT

Unit	Explanation
dB	Decibel-unit of measure of relative power level. $dB = 10\log_{10} P_1/P_2$
dBm	The transmission level which is referenced to a specified impedance value. 0 dBm = 1 mW
dBmp	Unit of dBm measurements made with a psophometrically weighted filter. $dBmp = 10\log_{10} pWp - 90$ $= dBm - 87.5$ (Under consideration of flat noise in 300 ~ 3400 Hz)
dBmO	dBm measurement referenced to a point of zero transmission level.
dBmOP	Relative power psophometrically weighted which is referenced to a point of zero transmission level.
dBr	The relative power level referenced to a point of zero transmission level. dBm = dBmO + dBr
dBrn	Unit of noise measurement on telephone lines. Reference noise is 1 pW (–90 dBm). OdBrn = 90 dBm
dBrnc	dBrn measurements used a C-message weighting filter.
dBrncO	dBrnc measurements referenced to a point of zero transmission level.

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